7.1. Introduction.

Recent studies on GaAs, doped with Sb have shown that the material contains an electron trap whose origin is directly related to Sb. The trap has so far been observed in bulk crystals grown by liquid encapsulated Czochralski (LEC) technique [7.1,7.2] and in epitaxial layers grown by metalorganic vapor phase epitaxy (MOVPE) [7.3,7.4]. The properties of this center have been investigated quite extensively. An activation energy of 0.47eV was obtained from Hall effect studies [7.1]. The trap was found to be a donor and its presence reduced the resistivity of the sample below the semiinsulating limit. It was suggested that the trap was related to a $Sb_{Ga}$ defect. The origin was convincingly identified later as the isolated $Sb_{Ga}$ heteroantisite with the help of electron paramagnetic resonance (EPR) [7.5] and photo-EPR [7.6] techniques. It was shown in these studies that the first charge state (0/+ donor level) of the defect was located at about $E_c - 0.5eV$. Since a group V atom was sitting at a group III site, it was expected that $Sb_{Ga}$ would be a double donor. The contention was confirmed by photocapacitance experiment and the +2+ level was found to be located at $E_c - 0.7eV$.
[7.4]. Finally, both the charge states of the $Sb_{Ga}$ defect were detected by DLTS [7.2]. The activation energies of the first and second charge states were found to be 0.54eV and 0.70eV respectively.

Interestingly, no $Sb_{Ga}$-related electron trap has so far been reported in LPE-grown GaAs:Sb materials. The possible reason may be that in both LEC and MOVPE techniques, growth is done under arsenic-rich conditions. Such growth conditions favor the formation of Ga-vacancies which, in turn, may support the generation of $Sb_{Ga}$ defects. LPE, on the other hand, is a process where growth is done under Ga-rich conditions and the grown material contains relatively smaller number of Ga-vacancies. Hence there is very little likelihood of $Sb_{Ga}$ defects to be present in LPE-grown GaAs:Sb. The same argument is usually put forward to explain the absence of $As_{Ga}$-related EL2 defect in LPE GaAs. From the analysis of photocapacitance data on heavily Sb-doped LPE GaAs we got an indirect evidence for the existence of an electron trap (vide Chapter 6) whose activation energy is similar to that of the $Sb_{Ga}$-related electron trap. However, we could not detect it directly from the experimental data obtained, possibly due to its very low density relative to that of hole traps.

In an earlier experiment [7.7], an electron trap with properties similar to that of the well-known trap EL2 was created in molecular beam epitaxial (MBE) GaAs by high temperature annealing under $Si_{3/4}$ cap. This result was explained by assuming
the out-diffusion of Ga atoms from the layer material to the Si$_3$N$_4$ cap, with the subsequent formation of As$_{Ga}$ defects at the vacant Ga sites which are believed to be the source of EL2. Similar results were obtained by other workers on furnace-annealed [7.8] and on rapid thermal annealed (RTA) [7.9] MBE GaAs and the phenomenon was ascribed to the high thermal stress at the semiconductor-dielectric interface during thermal annealing. The Ga out-diffusion model has been recently confirmed by Katayama et al. [7.10] by their RTA experiments on SiO$_2$-coated bulk GaAs wafers and they indicate that interfacial thermal stress actually enhances the out-diffusion of Ga. This technique of artificially increasing Ga vacancies was tried by us on our LPE-grown GaAs:Sb layers to see if it increased any possible Sb$_{Ga}$ electron trap in the material, which would be detectable by experimental techniques. The details of this work and the results are being described in this chapter.

7.2. Annealing and test device fabrication.

Each test sample was cut into two pieces and one of the pieces was subjected to an anneal at 800°C for 1 hour under ultrapure hydrogen flow in the LPE furnace with the sample placed into one of the wells of the graphite boat with a graphite cover on top. Thermal decomposition of the layer surface during annealing was reduced by using GaAs proximity caps. No change in
the carrier concentration or the type was noticed in the material after annealing.

Schottky-barrier diodes were fabricated on the cleaned surface of the layer by evaporating semi-transparent gold dots of diameter 0.5mm in a Varian electron beam system under a vacuum of \(10^{-8}\) Torr. Gold evaporation was made on both the unannealed and the annealed samples in the same run. Alloyed In-Sn ohmic contacts were formed in the proximity of the gold dots.

7.3. Deep level transient spectroscopy (DLTS) measurements.

7.3.1. Principles of DLTS.

The DLTS technique was introduced by Lang in 1974 [7.11], and is one of the most popular and powerful methods to characterize deep level traps. The principles of this technique are intimately related to the capture and emission processes involving such traps, which are discussed briefly below. A detailed account of the same may be found in Refs. [7.12, 7.13].

The dynamic electronic behavior of a deep state in a semiconductor is controlled by four processes, namely emission and capture of both electrons and holes. A capture process is characterized by a capture cross section, \(\sigma\) which is the effective area posed by a center to capture one carrier from a flux of carriers of a particular type. If \(N_T\) is the total concentration of a deep center, and at any time \(n_T\), is the density
of centers occupied by electrons, the number of electrons captured by the unoccupied centers per unit volume per unit time is given by

$$\frac{\Delta n_T}{\Delta t} = \sigma_n \langle v_{th} \rangle n (N_T - n_T)$$

(7.1)

where \(\langle v_{th} \rangle\) is the rms thermal velocity of electrons (in this case only), and \(n\) is the density of free electrons. Then the electron capture rate per unoccupied state is defined as

$$c_n = \sigma_n \langle v_{th} \rangle n$$

(7.2a)

The hole capture rate may be similarly defined as

$$c_\rho = \sigma_\rho \langle v_{th} \rangle \rho$$

(7.2b)

On the other hand, an emission process is represented by a carrier emission rate, \(e\) which is the number of carriers escaping from a type of occupied center per unit time. In thermal equilibrium, the capture and emission processes balance each other such that for electrons and holes we have

$$e_n n_T = c_n (N_T - n_T)$$

(7.3a)

and

$$e_\rho (N_T - n_T) = c_\rho n_T$$

(7.3b)
In thermal equilibrium, the occupancy of a trap is, therefore, given by

\[ \frac{n_T}{N_T} = \frac{c_n}{(e_n + c_n)} = \frac{e_p}{(e_p + c_p)} \]  

(7.4)

In thermal equilibrium the occupancy is also defined by the Fermi-Dirac distribution function [7.14]. For a deep state at energy \( E_T \) with degeneracy \( g_0 \) when empty of electrons, and \( g_1 \) when occupied by one electron, and in a system with Fermi level at \( E_F \), the occupancy at temperature \( T \) is

\[ \frac{n_T}{N_T} = \left\{ 1 + \left( \frac{g_0}{g_1} \right) \exp \left( \frac{(E_T - E_F) - kT}{kT} \right) \right\}^{-1} \]  

(7.5)

where \( k \) is Boltzmann constant. Thus, combination of Eqns. (7.4) and (7.5) yields the following relation between emission and capture rates for electrons:

\[ \frac{e_n}{c_n} = \left( \frac{g_0}{g_1} \right) \exp \left( \frac{(E_T - E_F) - kT}{kT} \right) . \]  

(7.6a)

The corresponding relation for holes is

\[ \frac{e_p}{c_p} = \left( \frac{g_0}{g_1} \right) \exp \left( \frac{(E_F - E_T) - kT}{kT} \right) . \]  

(7.6b)

For a non-degenerate semiconductor, the free electron and hole concentrations are given respectively by
\[ n = N_c \exp \left( -\frac{E_c - E_F}{kT} \right) \quad \text{(7.7a)} \]

and,
\[ \rho = N_v \exp \left( -\frac{E_F - E_v}{kT} \right) \quad \text{(7.7b)} \]

where \( N_c \) (\( N_v \)) is the effective density of states in the conduction (valence) band, and \( E_c \) (\( E_v \)) is the band-edge energy of the conduction (valence) band. The mean thermal velocity of charge carriers is given by
\[ \langle v_{th} \rangle = (3kT / m^*)^{1/2} \quad \text{(7.8)} \]

where \( m^* \) is the relevant band-edge effective mass. In order to find the temperature dependence of emission rates it is also necessary to consider the temperature dependence of carrier capture cross section \( \sigma \), which is expressed as
\[ \sigma(T) = \sigma_\infty \exp \left( -\frac{\Delta E_c}{kT} \right) \quad \text{(7.9)} \]

Finally, combining Eqns. (7.8)-(7.9), the emission rates of electrons and holes are found to be
\[ e_{n(p)}(T) = A_{n(p)} T^2 \sigma_{n(p)\infty} \exp \left( -\frac{\Delta E_{n(p)}}{kT} \right) \quad \text{(7.10)} \]

where the subscript \( n, p \) indicate electron, and hole respectively, the constant \( A_{n(p)} \) is the product of all the
prefactors of exponentials in the equations involved, and $\Delta E_{n(p)}$ is the activation energy of the trap.

In the DLTS experiment emissions are observed from initially filled majority or minority carrier trap levels in the depletion region of a Schottky-barrier or a junction diode. Usually, the variation of high frequency depletion capacitance of the test diode is monitored as the DLTS signal. For a simple analysis, it is assumed that the junction is abrupt, trap concentration in the material is uniform, traps are filled in, and emissions take place from the entire depletion layer. Then, under a constant applied reverse bias $V$, the capacitance transient in presence of a donor-like majority carrier trap in an n-type material becomes

$$C(t) = C(\infty) \left[1 - n_{iT}(t)/(N_B + N_T)\right]^{1/2}$$

(7.11)

where $n_{iT}(t)$ is the density of deep traps occupied by electrons at time $t$, and the final steady state capacitance $C(\infty)$ is given by

$$C(\infty) = A \left[\frac{1}{2} q \varepsilon_s (N_B + N_T)\right]^{1/2} \left(V + V_{bi}\right)^{-1/2}$$

(7.12)

where $A$ is the diode area, $q$ is the electronic charge, $\varepsilon_s$ is the permittivity of the material, $N_B$ is the shallow background donor density, $N_T$ is the deep trap density, and $V_{bi}$ is the built-in potential.

The time dependence of the electron occupancy, $n_{iT}(t)$ of a trap can be obtained from the rate equation.
\[
\frac{dn_T}{dt} = a(N_T + n_T^-) - bn_T^- \tag{7.13}
\]

where \( a = (c_n + e_n^-) \) is the net rate of gain of electrons, and \( b = (e_n^- + c_p) \) is the net rate of loss of electrons. If \( n_T^- = n_T(0) \) when \( t=0 \), then the general solution of Eqn. (7.13) is

\[
n_T^-(t) = n_T^- + \left[ n_T^- - n_T(0) \right] \exp(-t/\tau) \tag{7.14}
\]

where \( n_T^- \) is the steady state occupancy of the trap, given by

\[
n_T^- = aN_p/(a+b) \tag{7.15}
\]

and, emission time constant \( \tau \) is expressed as

\[
\tau = (a+b) = e_n^- + c_n + e_p^- + c_p^- \tag{7.16}
\]

The values of \( a \), and \( b \) are further simplified, depending on the nature of a trap, and the host material. For electron traps \( e_n^- \gg e_p^- \) while for hole traps \( e_p^- \gg e_n^- \). Again, in an n-type material Fermi level \( E_F \) is above deep trap levels \( E_T^- \). So, from Eqns. (7.6a) and (7.6b) \( c_n^- \gg e_n^- \) and \( e_p^- \gg c_p^- \), where \( c_n^- \approx 0 \). Similarly, in a p-type material \( c_p^- \gg e_p^- \) and \( e_n^- \gg c_n^- \), where \( c_p^- \approx 0 \). Thus for an electron trap in an n-type material, electron emission and capture processes dominate such that \( a = c_n^- \), and \( b = e_n^- \), and it is called a majority carrier trap. On the other hand, a hole trap in a p-type material becomes a majority carrier trap with \( a = e_p^- \), and \( b = c_p^- \).
Further, an electron trap in a p-type material is designated as a minority carrier trap having \( a = e_p \) and \( b = e_n + c_p \), and a hole trap in an n-type material is also called a minority carrier trap having \( a = e_n \) and \( b = e_p + c_n \).

From the above considerations, the capacitance transient (vide Eqn. (7.11)) of a Schottky-barrier diode fabricated on an n-type semiconductor containing an electron trap takes the form

\[
C(t) = C(\infty) \left[ 1 - \frac{N_T}{2N_B} \exp \left( -\varepsilon_n t \right) \right]
\]

(7.17)

where it has been assumed that \( N_i \ll N_B \). Eqn. (7.17) forms the basis of the DLTS experiments on majority carrier electron traps. In the derivation of the above formula it has been assumed that trap emissions occur from the entire depletion region of the diode. However, an exact analysis shows [7.13] that traps located between \( x_2 \) and \( x_1 \) only emit to contribute to the DLTS signal. Consequently, the expression for the DLTS signal gets modified to

\[
C(t) = C(\infty) \left[ 1 - \frac{N_T}{2N_B} \left( \frac{x_1^2 - x_2^2}{x_d^2} \right) \exp \left( -\varepsilon_n t \right) \right].
\]

(7.18)

In the above expression, \( 0 < x < x_2 \) is the region where the electron trap level \( E_T \) is above the steady-state Fermi level \( E_F \) and electron traps are never filled. On the other hand, for \( x_1 < x < x_d \), \( E_T \) is below the electron quasi-Fermi level \( E_{F_n} \) (assuming, electrons are the majority carriers) and electron traps never
emit during the experiment. The parameter $x_d$ is the depletion edge under applied reverse bias. It can be shown [7.3] that $x_1 = x_d - \lambda$, and $x_2 = x_0 - \lambda$ where $x_0$ is the depletion edge in the absence of any applied reverse bias. The transition distance, $\lambda$ may be calculated from the expression,

$$\lambda = \left[ \frac{2\varepsilon_s}{q^2N_B} (E_F - E_T) \right]^{1/2}$$

(7.19)

where the Fermi level, $E_F$ has to be interpreted properly and other symbols have their usual meanings.

The DLTS signal at a constant temperature, $T$ is defined as

$$S(T) = C(t_2) - C(t_1)$$

(7.20)

where $t_1$ and $t_2$ are sampling times, and the capacitance terms on the right hand side are obtained from either Eqn.(7.17) or (7.18). During a temperature scan, the peak of the DLTS signal occurs at a temperature $T_m$ when

$$e^{-t_m(T_m)} = \tau_m = (t_2 - t_1) / \ln(t_2 / t_1).$$

(7.21)

Further, the DLTS signal at $T_m$ is given by

$$S_m = \Delta C_0 \left\{ \exp\left[ -\frac{\ln\beta}{\beta - 1} \right] - \exp\left[ -\frac{\beta \ln\beta}{\beta - 1} \right] \right\}$$

(7.22)

where $\beta = t_2 / t_1$ and $\Delta C_0$ is defined as
\[ \Delta C_0 = \frac{N_T}{2N_B}CC(\omega) \]  \hspace{1cm} (7.23a)

if Eqn. (7.17) is used to construct the DLTS signal, or as

\[ \Delta C_0 = \frac{N_T}{2N_B} \frac{x_1^2 - x_2^2}{x_d^2} C(\omega) \]  \hspace{1cm} (7.23b)

if Eqn. (7.18) is used instead. Thus, the detection of a DLTS peak allows one to calculate the value of emission rate \( e_n \) at temperature \( T_m \) from the experimental parameters, \( t_1 \) and \( t_2 \). This is done for a number of pairs of \( t_1 \) and \( t_2 \) by performing several temperature scans to construct the Arrhenius plot of \( T_m^2 \) vs. \( 10^3/T_m \). It may be seen from Eqn. (7.10) that the slope of the Arrhenius plot which is a straight line, gives the activation energy, \( \Delta E_n \) and its intercept with the \( T_m^2 \)-axis gives the apparent capture cross-section, \( \sigma_{n\alpha} \) of the electron trap. In order to estimate the deep trap density \( N_T \), prior knowledge of shallow background impurity concentration, \( N_B \), and steady state high frequency depletion capacitance \( CC(\omega) \) is required. Eqn. (7.22) is then used to calculate \( \Delta C_0 \) from experimental values of \( S_m \) and \( \beta \), which is substituted either in Eqn. (7.23a) or in (7.23b) to find \( N_T \).
7.3.2. The DLTS system and experiment.

The DLTS system used in this work is shown by a block diagram in Fig. 7.1. A HP4280A capacitance meter was used for biasing the sample and its measuring high frequency capacitance at 1 MHz. The test device which was a gold Schottky-barrier diode, was mounted on the cold finger of an APD Cryogenics Displex closed cycle helium cryogenic system. Temperature scan of the device was made in the range 100-300K. For measurements above 300K, the device was mounted on a separate jig, provided with a heater and a thermocouple. Instead of using a box-car averager, and a chart recorder combination to construct and record the DLTS signal, the experiment was controlled by a HP 9000/236 computer. A HP-BASIC Program (DLTS), listed in Appendix A, was developed for the purpose. Isothermal capacitance transients at different temperatures were recorded in the computer. Before taking a transient, the test diode was held at a constant reverse bias (ranging between 1-3V) for about 200ms to bring it to equilibrium. Then the applied bias was removed for about 500ms to fill the electron traps. Finally, a constant reverse bias (ranging between 1-3V, depending on the sample) was applied for the trap emissions to occur and the capacitance transient was sampled at the smallest interval allowed by the C-meter. For a resolution of $10^{-3}$pF and $10^{-2}$pF, the smallest sampling intervals were 50ms and 20ms respectively. The DLTS signals $S(T)$ were later
Fig. 7.1. Block diagram of the DLTS system used.
computed for different specified rate windows and the DLTS spectra were plotted by a HP7475A digital plotter.

7.3.3 Results.

Fig. 7.2 shows the deep level spectra for a GaAs:Sb layer with an Sb concentration of $6 \times 10^{18}$ cm$^{-3}$, taken before and after annealing. The spectrum for the as-grown sample shows a sharp peak at around 175K corresponding to the presence of an electron trap A. A second weak and broad peak is observed at about 265K which may be due to another electron trap B. The concentrations of traps A and B before annealing are $1.7 \times 10^{13}$ cm$^{-3}$ and $4 \times 10^{12}$ cm$^{-3}$ respectively. After annealing, the height of peak A is reduced and it merges into a broad DLTS spectrum in which the most prominent feature is the peak due to trap B. Correspondingly, the concentration of trap A becomes $4 \times 10^{12}$ cm$^{-3}$ and that of trap B becomes $1.2 \times 10^{13}$ cm$^{-3}$. We repeated the experiment with a layer having higher Sb-doping of $2 \times 10^{19}$ cm$^{-3}$. The DLTS trace for the as-grown sample, as is seen from Fig. 7.3, is quite broad with a single peak due to trap A. There is also a weak shoulder at about 260K, which may again be due to trap B. As in the case of the moderately doped material, annealing reduced the concentration of trap A from $1.8 \times 10^{13}$ cm$^{-3}$ to $1.2 \times 10^{13}$ cm$^{-3}$ whereas that of trap B is enhanced from $6 \times 10^{12}$ cm$^{-3}$ to $1.7 \times 10^{13}$ cm$^{-3}$. Arrhenius plots for traps A and B were constructed by careful analysis of the capacitance transients and are presented in Fig. 7.4. Activation
Fig. 7.2. DLTS plot of electron traps in as-grown and annealed LPE GaAs layers with moderate Sb doping.

LPE GaAs: Sb  
[Sb] = 6 \times 10^{18} \text{ cm}^{-3}  
DLTS PLOT  
t_2/t_1 = 50 \text{ms}/10 \text{ms}  

$C(t_2) - C(t_1)$ [$10^2 \text{PF}$]  

TEMPERATURE [K]  

--- Before anneal  
--- After anneal
Fig. 7.3. DLTS plot of electron traps in as-grown and annealed LPE GaAs layers with high Sb doping.
Fig. 7.4. Arrhenius plots of electron traps in LPE GaAs:Sb.

LPE GaAs:Sb

$T^2 (K^2 S)$

$10^3 / T \ K^{-1}$

$10^4$

$10^3$

$2 \times 10^2$

$10^3 / T \ K^{-1}$

$E_T = 0.54 \text{ eV}$

$\sigma = 7.6 \times 10^{-14} \text{ cm}^2$

$T_{\text{c}} (K S)$

Trap B

Trap A

$E_T = 0.40 \text{ eV}$

$\sigma = 1.1 \times 10^{-12} \text{ cm}^2$
Fig. 7.5. Steady state photocapacitance spectra of the samples whose DLTS data are shown in Fig. 7.2.
Fig. 7.6. Steady state photocapacitance spectra of the samples whose DLTS data are shown in Fig. 7.3.
at about 0.9eV. This capacitance rise is attributed to the complementary transitions from the same hole traps. For the annealed sample, however, there is an additional increase of capacitance at about 0.75eV, indicating emission from an electron trap with a photoionization energy of the same value. Similar behavior of the photocapacitance data is observed more prominently in Fig. 7.6 for the layer with higher Sb-doping.

7.5. Discussion.

From the signature of the electron trap \( A \) in Fig. 7.4, we can identify it with the electron trap \( E_{B6} \) or \( E_3 \), previously found in electron-irradiated LPE GaAs [7.10]. However, there is no previous report regarding the existence of this trap in as-grown LPE GaAs. Origin of the trap is believed to be due to defects or complexes arising out of crystallographic disorders existing in the material, which explains the reduction of the density of the same upon annealing.

Electron trap \( B \) shows two distinctly observable properties. First, the concentration of this trap is increased with that of Sb in both the unannealed and annealed materials, which is clearly seen from Table 7.1. This implies that the trap is directly related to Sb dopants in GaAs:Sb. Secondly, annealing of the material at high temperatures increases the concentration of trap \( B \). The measured signature of trap \( B \) and its relation with Sb
Table 7.1
Concentration of electron traps in LPE GaAs:Sb layers.

<table>
<thead>
<tr>
<th>Sb doping density (cm(^{-3}))</th>
<th>Concentration of trap A (cm(^{-3})) Before anneal</th>
<th>Concentration of trap A (cm(^{-3})) After anneal</th>
<th>Concentration of trap B (cm(^{-3})) Before anneal</th>
<th>Concentration of trap B (cm(^{-3})) After anneal</th>
</tr>
</thead>
<tbody>
<tr>
<td>6\times 10^{18}</td>
<td>1.7\times 10^{13}</td>
<td>9\times 10^{12}</td>
<td>4\times 10^{12}</td>
<td>1.2\times 10^{13}</td>
</tr>
<tr>
<td>2\times 10^{19}</td>
<td>1.8\times 10^{13}</td>
<td>1.2\times 10^{13}</td>
<td>6\times 10^{12}</td>
<td>1.7\times 10^{13}</td>
</tr>
</tbody>
</table>
concentration in the material suggest that it is the same as the Sb$_{Ga}$-related electron trap obtained previously in MOVPE-grown GaAs:Sb [7.3]. Formation of this defect is not, in general, favored in LPE GaAs, grown under Ga-rich conditions. This is consistent with the observed low density of trap B in our samples, prior to annealing. However, if there is any out-diffusion of Ga upon high-temperature annealing, the concentration of this trap should increase as a consequence of generation of more Sb$_{Ga}$ defects. This we actually observe from our data in Figs. 7.2 and 7.3. However, simultaneous generation of EL2 is not observed in our experiments since Sb has much higher affinity towards Ga-vacancies [7.5] and forms Sb$_{Ga}$ defects at the expense of As$_{Ga}$. Further, from the experimental results of Wada and Inoue [7.17], we may note that the loss of As near the surface of GaAs during annealing decreases the concentration of EL2.

The photocapacitance spectra of the annealed samples in Fig. 7.5 and 7.6 indicate the presence of an electron trap with a photoionization threshold near 0.75eV. We may note from previous reports that the Sb$_{Ga}$ electron trap is a double donor with a second charge state energy of 0.7eV [7.2,7.4]. We can, therefore, attribute the 0.75eV threshold, obtained from the photocapacitance experiments, to the +2+ transition of trap B. However, this transition is not being observed in the as-grown samples, suggesting that the density of trap B in such materials is actually low.
Finally, it should be mentioned that we did not use any encapsulant over our GaAs layers during annealing. We believe that in this case, out-diffused Ga atoms piled up near the surface.

7.6. Conclusions.

From DLTS and photocapacitance experiments we have shown that an electron trap, which is present in low concentrations in as-grown LPE GaAs:Sb materials, can be created in appreciable concentrations using high temperature annealing. Concentration of the trap also follows that of Sb in the material. It is suggested that the electron trap originates from $Sb_{Ga}$ defects whose generation is favored in annealed materials due to Ga out-diffusion.

DLTS results further confirm the existence of a second electron trap in the material with an activation energy of 0.4eV. Concentration of this trap is reduced upon annealing. It is supposed that the trap is related to simple native defects or complexes and is the same as the trap $EB6$ detected previously in electron-irradiated GaAs.
References


