CHAPTER 2

Background and Previous Work
Chapter 2

BACKGROUND AND PREVIOUS WORK

2.1 Introduction

Scaling of CMOS technology is done in order to meet the performance, cost, and power requirements of forthcoming high throughput applications [9]. This has been made possible by steady progress in planar processing technology to manufacture transistors with even smaller dimensions, resulting in an exponential growth in number of transistors on a single chip and, hence, functionality of ICs as per Moore’s law [10]. The electronic industry has remarkably kept pace with this exponential growth for the last four to five decades. This exponential growth of transistors count cannot continue for ever as pointed out by Moore’s himself in 2003 [11]. Therefore, many experts are now claiming that CMOS scaling has reached its limits. There are three factors that limit CMOS scaling:

1) Smaller or minimum dimensions that can be fabricated on a chip
2) Diminishing returns in switching performance of scaled CMOS device
3) Static or off state leakage power.

The primary limitations for CMOS scaling have been associated with the process of lithography i.e. how small a transistor can be fabricated on a chip. Advancement in the technology has demonstrated the use of 193nm wavelength to pattern 45nm transistors [12]. Further advancement has opened up the possibility of using Extreme ultraviolet lithography (also known as EUV or EUVL) as the next generation lithography using an extreme ultraviolet (EUV) wavelength. This is targeted to be used for future technologies below 15nm [13-14], resulting in the exponential rise of the cost of lithographic equipment that will limit the profitability of increased scaling.

Due to CMOS scaling, transistor dimensions are approaching the limits of atom or molecule and clearly, it cannot be less than that limit. This aggressive scaling severely affects the electron and hole mobilities which means that the performance gains from each successive generation is less than the gain from the last generation.
The final and the most significant factor that limits MOS scaling is the static or OFF state power consumption. The sources that contribute to OFF state leakage are: junction leakage, gate induced drain leakage, subthreshold current and gate tunnel currents. They become more and more pronounced as the dimensions are scaled. It was shown in [12] that the leakage currents grow exponentially as gate length is reduced.

As depicted in Figure 2.1, although technology scaling reduces the dynamic power dissipation, there is a marked increase in the subthreshold leakage power which may exceed the active power for future technology nodes around 10nm node [15]. Technology scaling trends, as dictated by Moore’s law, has pushed power consumption to the forefront for circuits having limited power budget. Negligible amount of dynamic power dissipation takes place when CMOS transistor is not switching at higher technology nodes. Nevertheless, static power dissipation increases appreciably which is primarily due to the flow of leakage current under subthreshold condition. Therefore, some special class of applications, which are bound by ULP budget, can be accomplished by operating circuits in the subthreshold region. This chapter briefly reviews the sources of power consumption at the nanometer scale with respect to the subthreshold region. It then also focuses on the basics of upcoming devices like TFETs and CNFETs to replace CMOS followed by the review of selected prior art.

Figure 2.1: Normalized dynamic and static power dissipation for \((W/L_g=3)\) device. Data is based on the ITRS [9].
2.2 Sources of Power Consumption in CMOS

Sources of power consumption can be divided into two major types:

1) Dynamic power consumption

2) Static power consumption

The difference between the two is that while the dynamic power is proportional to the activity in the circuit and the switching frequency, whereas the static power is independent of both. The power consumed in any CMOS logic must be reduced for the following two reasons. First it is important to reduce the dissipation of heat to allow a large density of the components to be fabricated on an IC chip. Second one is to conserve energy of the battery operated systems in order to enhance the battery life time. This section briefly reviews dynamic and static power in detail along with different leakage currents.

2.2.1 Dynamic Power Consumption

Dynamic power consumption occurs when internal node (s) of a circuit switches due to changes in the input vector (s). It is caused by two different categories of current: load capacitance \((C_L)\) charging/discharging current and short circuit current. Therefore, it consists of two components namely switching power and short circuit power [16].

1. Switching power

Switching power can be described best with the help of CMOS inverter as shown in Figure 2.2. Assuming the initial input vector to be ‘1’, then the voltage across the load capacitance is ‘0’ as it is fully discharged by the pull-down NMOS. If from this steady state condition, the input vector is changed to ‘0’, then the NMOS stops conducting and PMOS starts conducting, thereby, charging \(C_L\) gradually to \(V_{DD}\). The switching power consumption due to capacitive current is given by [16]:

\[
P_{dyn} = \alpha f C_L V_{DD}^2
\]  

(2.1)

where ‘\(f\)’ is the clock frequency, and ‘\(\alpha\)’ is the activity factor. It is to be noted that, \(C_L\) is the parasitic capacitance of the output node of the inverter. \(C_L\) is composed of three components: drain diffusion capacitance of both the MOSFETs, capacitance of the
connecting wires, and the input capacitance of the fan out gates. The energy drawn from \( V_{DD} \) is totally lost in the complete charging and discharging cycles. Equation (2.1) shows that the power consumption is a quadratic function of \( V_{DD} \) and hence, the most significant reduction in power dissipation is achieved by \( V_{DD} \) reduction technique.

2. **Short-Circuit Power**

During the transition of signal, both pull up and pull down devices conduct simultaneously for a short duration of time which temporarily results in short-circuit path from supply to ground within gate. The simplest static CMOS inverter is shown in Figure 2.2. When NMOS transistor turns ON due to the rising input then the PMOS transistor also continues to conduct current until the input voltage becomes greater than \( V_{DD} - |V_{tp}| \). Hence, a direct current flow from supply to ground, which is called as short-circuit current [17]. The total charge that flows in this period can be found by calculating the area of the triangle [18] as shown in Figure 2.2. Let ‘\( t_r \)’ denotes the time for the input voltage to rise from \( V_{tn} \) to \( V_{DD} - |V_{tp}| \). \( V_{tn} \) and \( V_{tp} \) is the threshold voltage of NMOS and PMOS transistors respectively. Assuming symmetric rise and fall transitions for both input and output of the logic gate, the total short-circuit power consumption due to short circuit current as shown in Figure 2.3 for a single logic gate is defined as [16]:

\[
P_{SC} = \alpha \cdot V_{DD} \cdot I_{peak}
\]

Where ‘\( \alpha \)’ is the switching activity factor, \( I_{peak} \) is the peak current per transistor width.

![Figure 2.2: Schematic of inverter with voltage and current waveforms.](image-url)
Figure 2.3: Short circuit leakage current of inverter at 32 nm technology node.

2.2.2 Static Power Consumption

The static power ($P_{static} = I_{static} \times V_{DD}$) is defined as the power consumption due to constant current from $V_{DD}$ to ground in the absence of any switching activity [16]. Ideally, this static power consumption in a CMOS circuit is zero, as devices in PUN (pull-up network) and PDN (pull-down network) are never switched ON simultaneously in steady state conditions. This type of dissipation is negligible for long channel transistors with high $V_{th}$. Unfortunately, present and future technologies will suffer from high static power, which could even exceed the dynamic contribution in active mode [19]. Shrinking device dimensions causes different sources of leakage current [9]. Different leakage current components contributing to leakage power dissipation through a short channel NMOS transistor are shown in Figure 2.4 [20] and are briefly described here:

Figure 2.4: Leakage current mechanisms in an NMOS transistor.
1. **Reverse bias pn junction current and band to band tunneling leakage current**

Normally in a MOS transistor as shown in Figure 2.4, drain/source to well junction is reverse biased which causes pn junction leakage current. This current is originated because of the minority carrier drift/diffusion near the edge of the depletion region and due to electron-hole pair generation in the depletion region of the reverse biased junction [21-22]. The magnitude of the diode’s leakage current depends on the area of the drain diffusion and the leakage current density, which in turns is determined by the doping concentration. If both n and p regions are heavily doped, band-to-band tunneling (BTBT) dominates the pn-junction leakage [23]. BTBT leakage current flows under high electric field (>10^6 V/cm) across the reverse biased pn junction.

Process technologies are generally well designed to keep this pn junction leakage small relative to the subthreshold current. Since the pn-junction leakage scales with $V_{DD}$ and temperature in a similar fashion as subthreshold current, pn-junction leakage is negligible across the full range of $V_{DD}$ under subthreshold conditions [24].

2. **Subthreshold leakage current**

The origin of subthreshold leakage current is due to the process of diffusion of minority carriers in a non-conducting transistor when $V_{GS} < V_{th}$. Under this condition, the MOS transistor is operated in weak inversion mode [25-26]. Difference of potential between the drain and source creates a flow of minority carriers on the surface of the channel. The subthreshold current is exponentially dependent on $V_{th}$. This is the reason why the low $V_{th}$ characterizing technologies lead to large subthreshold current.

3. **Gate leakage current**

Due to scaling, oxide thickness ($T_{OX}$) is progressively getting thinner. As $T_{OX}$ scales below 3 nm, gate to channel leakage current starts to appear even at low gate voltage. This results in direct tunneling of electrons through the gate oxide as depicted in Figure 2.4. The gate leakage is present in both the OFF state and the ON state of a MOS transistor, which makes it more difficult to control than subthreshold leakage [178-180]. Gate leakage is the sum of two components namely the gate to channel and the gate to source/drain extension overlap current in the ON state. However, in the
OFF state, it is due to the edge direct-tunneling current (EDT). This leakage current increases exponentially with the $T_{OX}$ reduction due to the increasing tunneling probability that depends strongly on the voltage across the oxide. The gate leakage is expressed by the following equation [28]

$$I_{\text{gate}} = W_{\text{eff}} L_{\text{eff}} A \left( \frac{V_{\text{ox}}}{T_{\text{ox}}} \right)^2 \exp \left[ \frac{-B(1-(1-V_{\text{ox}}/\phi_{\text{ox}})^{3/2})}{V_{\text{ox}}/\phi_{\text{ox}}} \right]$$  \hspace{1cm} 2.3

Where,
$$A = \frac{q^3}{16\pi \hbar \phi_{\text{ox}}} \quad \text{and} \quad B = \frac{4\sqrt{2}m\phi_{\text{ox}}^{3/2}}{3\hbar q}$$

‘$V_{\text{ox}}$’ is the potential drop across the thin oxide layer, ‘$\phi_{\text{ox}}$’ is the barrier height for the tunneling particles, ‘$T_{\text{OX}}$’ is the oxide thickness, and ‘A and B’ are physical parameters.

Gate tunneling current has a very strong dependence on the voltage across the gate. Hence, it decreases much more quickly with $V_{\text{GS}}$ and $V_{\text{DD}}$ as compared to the subthreshold current.

4. **Gate-Induced Drain Leakage current**

A high electric field exists in the overlapping zone between gate and drain which leads to the generation of current from the edge of drain and terminates at the body of the transistor. Consider an NMOS transistor, when a low gate potential is applied ($V_G \approx 0\text{V}$), holes accumulate at the surface and create a region which is more heavily p doped than the substrate. If this happens while the drain is connected to a high potential ($V_{DD}$), the depletion layer near the drain becomes narrower. As a result of this, minority carriers are emitted in the drain region underneath the gate and pushed to the substrate due to the vertical electric field as shown in Figure 2.5. Thinner $T_{OX}$ and higher potential between gate and drain enhance the electric field thereby increasing Gate-Induced Drain Leakage (GIDL) [24].

The lower values of $V_{DS}$ for subthreshold operation decreases the electric field across the drain, hence, GIDL current component becomes negligible.
5. **Drain induced barrier lowering (DIBL) and Punchthrough Leakage current**

Due to the proximity of source and drain in short channel devices, the depletion regions at the drain-substrate and source-substrate junctions extend into the channel. As the channel length is reduced for a fixed doping level, the separation between the depletion region boundaries decreases. An increase in the reverse bias across junctions (with increase in $V_{DS}$) also pushes the junctions nearer to each other, resulting in an increase in leakage current. This phenomenon is sometimes referred to as DIBL. This may lead to large flow of current called as punchthrough leakage current.

Though these leakage components are quite significant for strong inversion operation, they tend to become negligible under subthreshold conditions where subthreshold leakage is more pronounced [24]. However, gate leakage dominates subthreshold leakage current at very low temperature as it decreases exponentially with temperature.

In order to try to reduce the power dissipation of CMOS, circuit engineers change their circuits, and device engineers change their devices. The bulk of this thesis is about devices, so it would be appropriate to look into new transistor operating principles which can reduce power dissipation in integrated circuits. As far as CMOS
is concerned, one way to reduce power dissipation is to operate the optimized device in subthreshold region. Based on this optimization and characterization of CMOS, particularly for subthreshold region, we have published a paper which will be covered in chapter 3. The next section briefly discusses about two upcoming devices namely TFETs and CNFETs.

2.3 **Introduction to the Tunnel FET**

Tunnel FETs, also referred to as TFETs are the promising devices to replace the conventional MOSFETs for low power applications because of their quantum tunneling barrier. When the device is turned on, the carriers tunnel through the barrier in order for current to flow from source to drain. When the device is OFF, the presence of barrier keeps the OFF current extremely low which is several orders of magnitude lower as compared to the traditional MOSFET.

2.3.1 **TFET structure and operation**

The tunnel FET is a gated p-i-n device structure that is fully compatible with conventional MOSFET technology. Figure 2.6 shows the device structure utilizing a single gate.

![Figure 2.6: A simple TFET structure with one gate.](image-url)
The regions in the tunnel FETs have been named as source, channel and drain respectively in order to be consistent with current MOS technology. The n(p) type device is turned OFF when the gate is held at 0V and turned ON when the positive (negative) voltage is applied to the gate. Source to drain junction is reverse biased in n(p) type device. The current conduction in TFET is through Band to Band Tunneling (BTBT). In n(p) TFET, electrons(holes) tunnel from source valence(conduction) band to drain conduction(valence) band.

When a Tunnel FET is designed with symmetry between the n- and p-sides (similar doping levels, similar gate alignment, etc.), the device exhibits ambipolar behavior, whereby the transfer characteristics resemble those of a pFET when a negative voltage is applied to the gate, and those of an nFET when a positive voltage is applied to the gate as shown in Figure 2.6.

### 2.3.2 Band-to-Band Tunneling (BTBT)

In TFETs, tunneling of interest is band-to-band tunneling. For band-to-band tunneling to occur, an electron in the valence band of semiconductor tunnels across the band gap to the conduction band without the assistance of traps. Leonid V. Keldysh and Evan O. Kane proposed models for the tunneling probability and the tunneling current (via BTBT) in semiconductors [29-30]. Equation 2.4 gives the tunneling current density for a direct bandgap material [31].
Background and Previous Work

Equation 2.4 can be consolidated to give more common expression for Kane’s equation as:

\[ J_T = AF \cdot e^{-BF} \]  \hspace{1cm} 2.5

where A and B represent material properties for the semiconductor of interest. From equation 2.5, it can be seen that the BTBT generation rate of carriers into the channel is exponentially sensitive to the electric field at the tunneling junction which means that a larger electric field at the tunneling junction produces a larger BTBT current (i.e., a larger \( I_{ON} \)). Therefore, while designing a TFET, one should incorporate a large built-in electric field so as to increase \( I_{ON} \) and thus, the performance of a device for a given power supply. A conventional TFET design utilizes a very steep doping profile in the source in order to realize a large built-in electric field near the BTBT junction. Despite advancements in low energy ion implantation, flash annealing, and \textit{in situ} doping during epitaxial growth, fabrication of very steep doping profiles remains a challenge. Conventional TFET, therefore, has the drawback of having low value of \( I_{ON} \) as compared to traditional MOSFET. Device engineers have come up with different ideas to enhance \( I_{ON} \) by incorporating double gate instead of single, using low band gap material, high \( K \) dielectric material or by using hetrostructures.

2.3.3 Subthreshold Slope of TFET

Subthreshold swing (‘SS’) is a quality measure of a device that determines the relationship between the subthreshold current and the gate voltage. It is defined as the amount of \( V_{GS} \) required to change the subthreshold current by an order of magnitude. A small ‘SS’ is preferred for higher \( I_{ON} \) current for a given \( I_{OFF} \) current value. The inverse subthreshold swing has a lower bound of 2.3 \( kT/q \), or 60 mV/decade [32]. From the definition of inverse ‘SS’, it can be also expressed as follows [32].
The dependence of subthreshold swing on gate voltage is shown in Figure 2.8 [33]. Two important observations can be drawn. First, the subthreshold swing of TFETs is not constant, but rather a function of gate voltage. Secondly, at low gate voltages, it is possible for Tunnel FETs to have a subthreshold swing less than the 60 mV/decade MOSFET limit at room temperature. When the subthreshold swing is calculated as in equation 2.6 the result is [34]:

$$SS = \left( d \left( \log_{10} I_D \right) / dV_{GS} \right)^{-1}$$  \hspace{1cm} 2.6$$

Where, $V_{eff}$ is the bias at the tunnel junction and $F$ is the electric field at the tunnel junction.

$$SS = \log_{10} \left[ \frac{1}{V_{eff}} \frac{d_{eff}}{dV_{GS}} + \frac{F + b}{F^2} \frac{dF}{dV_{GS}} \right]^{-1}$$  \hspace{1cm} 2.7$$

[Figure 2.8: Tunnel FET subthreshold slope dependence on gate voltage for different dielectric constants [33].]

$$b = \frac{4\sqrt{m^*E_g^{3/2}}}{3qh}$$  \hspace{1cm} 2.8$$
From equation 2.7, it should be noted that the subthreshold swing is a function of $V_{GS}$ which is in sharp contrast with conventional MOSFET. This means that the subthreshold region does not appear as a straight line when $I_{DS}$-$V_{GS}$ is plotted on a log-linear scale, and the swing does not have one unique value. Swing is smallest at the lowest $V_{GS}$, and increases as $V_{GS}$ increases. Thus, a steep subthreshold swing allows low power operation of device as power scales as the square of $V_{DD}$. A steep SS device requires less gate voltage for a given $I_{ON}/I_{OFF}$ ratio. Therefore, the research on TFETs seeks to reduce power dissipation while maintaining the performance of a given system.

2.3.4 State-of-the-art of the TFET

The first investigation containing the basic element of tunnel transistor was conducted by Stuetzer in 1952 [35]. He showed the ambipolar nature of the current–voltage $I$–$V$, in the field gating of a lateral Ge p–n junction. Quinn et al. at Brown University [36] were the first to propose the gated p-i-n structure of a Tunnel FET in 1978, and suggested the usefulness of this device for spectroscopy. They proposed the formation of a surface-channel MOS tunnel junction by replacing the n-type source of an n-MOSFET with a highly degenerate p type source. In 1988, Leburton et al. [37] proposed the first vertical TFET with the aim of creating a high-speed transistor in which the gate was used to control the negative differential resistance (NDR). Baba [38] in 1992, fabricated Tunnel FETs which he called Surface Tunnel Transistors, using MBE in III-V materials. In 1994, Reddick and Amaratunga proposed and fabricated the first known Si based BTBT transistor [39]. They were motivated by the desire for devices that would be faster than conventional MOSFETs, as tunneling devices are, and that could be scaled down more easily without running into problems such as punchthrough. Hansch et al. [40] in 2000 proposed and fabricated a Si vertical TFET and noted its potential for low off-current relative to the MOSFET. In 2004, Aydin et al. [41] fabricated Lateral Interband Tunneling Transistors on SOI. These devices used a different TFET structure without an intrinsic region and placing the gate over a p-n junction. They claimed that this would reduce gate capacitance and therefore increase speed. They also claimed that there should be no current saturation for these devices. In 2004, the concept of low subthreshold swing in TFET was reported by wang [42], Bhuwalka [43], and Appenzeller [44]. A subthreshold swing smaller than the 60 mV/dec limit of conventional MOSFETs was reported for the first
time by [44]. [43] proposed a Tunnel FET on silicon with a SiGe delta layer, grown by molecular beam epitaxy “MBE”. The SiGe replaced the silicon delta layer so that the smaller bandgap should have reduced the tunnel barrier width and increased tunneling current in the on-state as well as lowering the subthreshold swing. Boucart et.al [45], showed that length scaling in nanometers dimensions gives much better results as compared to MOSFET. TFET, unlike MOSFET, does not suffer from SCE, DIBL and have much better $I_{ON}/I_{OFF}$ ratio and sub-threshold swing is not limited by temperature. It can, therefore, be much lower than 60mV/dec even at room temperature and will have much lower sub-threshold power consumption, that might be very useful for low power/sub-threshold region applications. The same author in [46] has shown ways to boost up the ON current of silicon TFET, using double gate structures to double the ON current and utilizing high K dielectrics. To further enhance the ON current, Ge material [47] is employed.

We have published an optimized TFET paper which will be covered in chapter 5.

2.4 Introduction to Carbon Nanotube Field Effect Transistor (CNFET)

Carbon Nanotubes field effect transistor (CNFET) is one of the most promising device that could eliminate most of the fundamental limitations of traditional silicon devices. Improved channel transport and high carrier velocity of CNT results in significant improvement in speed over Si MOSFET [48, 49, 50]. They have the potential to minimize the subthreshold slope (i.e., minimize the short channel effects). Initially there was lot of fabrication issues with CNFET technology. However, most of these issues like positioning and alignment of CNTs along with the presence of metallic CNTs have been solved [51, 52]. Moreover, CNFET can be fabricated using the existing CMOS technology infrastructure and it can also be integrated with CMOS on the same chip [53], therefore, most of the fabrication issues have been solved and CNFET holds a bright future and a lot of promise. This section briefly introduces CNFET technology.

2.4.1 Carbon Nanotubes

The carbon nanotube is made by rolling up a sheet of graphite or graphene (a monolayer of $sp^2$ bonded carbon in a honeycomb lattice, which are even stronger than the $sp^3$ bonds in diamond) into a cylinder. This makes atomic electromigration more
difficult which means that carbon nanotubes are an extremely stable structure that avoids damage from high currents [54]. These cylindrical carbon tubes have remarkable electrical properties, which are valuable for nanotechnology, electronics, optics, and other fields of material science and technology. Nanotubes are categorized as single walled CNTs (SWCNTs) and Multi walled CNTs (MWCNTs).

Carbon nanotubes (CNTs) are hollow cylinders of graphene having varying diameter (0.4nm to 4nm) and it provides a single path between source and drain. They can be classified depending upon the direction in which the graphene sheets are rolled up either as semiconducting with distinct band gap or metallic with no band gap. The resulting structure is called single-walled carbon nanotube (SWCNT). If more than one SWCNT of varying diameters are folded concentrically, they form a multi walled CNT (MWCNT). The properties of CNTs such as bandgap, conductivity, diameter etc. are determined by its chirality \((n_1, n_2)\). A SWCNT works as metal if \(n_1 = n_2\) or \(n_1 - n_2 = 3i\), where ‘i’ is an integer. Otherwise, it works as a semiconductor. The relationship between chirality \((Ch)\), CNT diameter \((D_{CNT})\) and threshold voltage \((V_{th})\) is given by:

\[
Ch = a\sqrt{(n_1^2 + n_2^2 + n_1n_2)} \quad 2.9
\]

\[
D_{CNT} = \frac{Ch}{\pi} \quad 2.10
\]

\[
V_{th} \approx \frac{E_g}{2} = \frac{aV_x}{qD_{CNT}\sqrt{3}} \quad 2.11
\]

Where \(E_g\) is the energy gap, \(q = \) electronic charge, \(a = \sqrt{3}d = 2.49\)\(\text{Å}\) is the lattice constant (where \(d = 1.44\) \(\text{Å}\) is the inter-carbon-atom distance) and \(V_x = 3.033eV\) is the carbon \(\pi\)–to–\(\pi\) bond energy in the tight bonding model [55, 56].

The working principle of CNFET is similar to that of conventional MOSFET. The bulk semiconductor channel is replaced by a number of semiconducting carbon nanotubes as shown in Figure 2.9. Since the carriers are now confined to a narrow nanotube, their mobility increases due to quasi 1-D (ballistic) transport.
2.4.2 CNFET Model Overview

A circuit-compatible CNFET model from Stanford University is used for the simulation purpose [49] [57]. It provides improved accuracy by accounting for several practical non-idealities, such as scattering, effects of the doped source/drain extension region, and inter-CNT charge screening effects. In addition, by including a full trans-capacitance network, it does better predictions of the dynamic performance and transient response.
The semiconducting intrinsic CNT, shown in Figure 2.10, under the gate acts as the channel and heavily doped CNT regions outside the gate forms the source/drain extension regions.

The model is organized hierarchically into three levels [58] as shown in Figure 2.9. The first level (L1) describes the intrinsic CNT region that forms the channel under the gate. Several non-idealities, such as near ballistic transport and parasitic components are taken into account here. For a MOS-like n-type CNFET, the hole current is usually negligible as compared to the electron current for semiconducting sub-bands. This is due to heavily doped source/drain extension regions (n-type). The opposite is true for p-type CNFETs.

The second level L2 represents the heavily doped source/drain extension region and takes into account the effects such as elastic scattering, parasitic resistances of the source/drain extension region, parasitic capacitances of the source/drain extension region, and the Schottky barrier resistance of the source/drain metal contacts.

The third level L3 models the effects such as CNT-to-CNT charge screening and the gate-to-neighboring-contact parasitic capacitances. Practical CNFETs must contain multiple CNTs per device in order to achieve sufficient drive current at reasonable speed. Thus, the model allows multiple nanotubes and accounts for the CNT-to-CNT charge screening effect present in this device. In other words, CNTs only experience charge screening from their immediate neighbors.
2.5 Summary

This chapter has successfully introduced the concept of technology scaling that result in faster and smaller transistors to achieve higher performance and higher chip density but static power consumption issues increase significantly. Hence, increased leakage power dissipation becomes a major bottleneck while designing low power circuits for portable application. This chapter also presents an overview of promising emerging devices. It explains the need for alternative technologies like TFETs and CNFETs and also reviews their basic concepts.

The next chapter explores CMOS device optimization to achieve better subthreshold slope and $I_{ON}/I_{OFF}$ ratio to enhance the speed and to reduce the switching energy of subthreshold circuits.