CHAPTER 3

Optimization and Characterization of CMOS for Ultra Low Power Applications
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**OPTIMIZATION AND CHARACTERIZATION OF CMOS FOR ULTRA LOW POWER APPLICATIONS**

In the subthreshold regime, the aggressive voltage scaling holds great challenges and promise for strict energy budget applications. It has been established, however, that high speed superthreshold devices are not suitable for moderate performance subthreshold applications. The selection of threshold voltage ($V_{th}$) and oxide thickness ($T_{OX}$) is much more flexible for subthreshold applications rather than superthreshold one at low voltage levels. It is therefore, necessary to explore and optimize silicon MOSFET’s process and geometry parameters at Nano technological node. This chapter calibrates the process and electrical parameters for n and p type MOS with 35nm physical channel length. Subsequently, the calibrated MOS device for superthreshold application is optimized for better performance under subthreshold conditions using Synopsys Technological Computer Aided Design (TCAD) simulation. The simulated device shows 9.89% enhancement in subthreshold slope and 34% benefit in $I_{ON}/I_{OFF}$ ratio for the same drive current.

3.1 **Introduction**

CMOS technology scaling trends are mostly concentrated on achieving higher speed. Device fabrication process parameters selection for Ultra Low Power (ULP) applications with lower operating voltages and frequencies is still under exploration [10, 59-62]. It has been shown in [61] that subthreshold circuit performances are significantly gained by optimizing the device geometry parameters. For superthreshold circuit applications, process and geometry parameters are largely dictated by different leakage currents and, hence, severely affect its static power dissipation [32, 63-66]. However, due to lower bias supply, gate leakage current, DIBL, and punchthrough effects are almost negligible under subthreshold conditions [24]. Therefore, it seems to some extent that the design constraint for selecting $V_{th}$ and $T_{OX}$ are more flexible in subthreshold region of operation.
scaling of $V_{th}$ for superthreshold devices, is limited by the amount of static leakage, mainly subthreshold leakage current in submicron technology nodes [60, 61]. A high $V_{th}$ device will give notable performance penalty under subthreshold conditions due to lower subthreshold leakage current. Therefore, the choice of $V_{th}$ is a tradeoff between speed and leakage power dissipation in case of superthreshold applications. However, in subthreshold region, lower static leakage power dissipation due to scaled $V_{DD}$ even below $V_{th}$ allows further reduction in $V_{th}$ to enhance the speed of subthreshold devices and circuits.

Gate leakage along with subthreshold leakage is also a major bottleneck in aggressive $T_{OX}$ Scaling in order to obtain better control over the channel for superthreshold devices [60, 61]. $T_{OX}$ generally scales down from 130 nm technology in case of high frequency applications to keep gate leakage minimum due to higher bias [60]. However, it degrades subthreshold slope (SS). In subthreshold regime due to lower $V_{DD}$, $T_{OX}$ reduction will not significantly increase the gate leakage current [24]. Moreover, transistor input capacitance is smaller under subthreshold conditions than the superthreshold region of operation [61]. Therefore, more aggressive $T_{OX}$ scaling is possible to achieve higher speed and lower power consumption under subthreshold regime.

Halo and retrograde doping are generally needed to suppress short channel effects in case of superthreshold devices in submicron technology. These doping wells are used to reduce Drain Induced Barrier Lowering (DIBL) and punch through effects and to control $V_{th}$ of the device independent of its subthreshold slope. However, due to lower bias in subthreshold region, DIBL and punch through effects are not significant at all. Therefore, subthreshold device characteristics are less sensitive to halo and retro doping. This chapter, therefore explores the subthreshold design of MOS device at 45nm technology node with enhanced subthreshold slope and higher current drive capability of the device.

### 3.2 Calibration of MOS Device

As shown in Figure 3.1, $L_g$ and $T_{OX}$ of the device are set as the transistor’s performance parameters [67]. In [68], authors have fabricated the optimized 35nm gate length NMOS device at $V_{DD} = 0.85V$ with 676 $\mu A/\mu m$ drive current capability, subthreshold slope = 86mV/dec., and $I_{OFF} = 100nA/\mu m$. The said device is fully
optimized for short channel effect (SCE) suppression and parasitic resistance reduction.

There is a need to design a superthreshold device with better performance at 45nm technology node. Then it can be optimized to get an optimum subthreshold device. For this purpose, NMOS device is fabricated in [68]. The physical dimensions of a 35nm device are listed in Table 3.1 [68]. The poly-Si thickness is 150 nm, while the distance of S/D contact to gate is 52 nm. Source and drain contactss are treated as ohmic for simulation purpose. The resulting SDE junction depth is 15nm for NMOS and 28nm for PMOS. Lower $T_{OX}$ for PMOS causes more drive current in PMOS comparable to NMOS. Also, lower $T_{OX}$ of PMOS will cause more vertical electric field in channel which further increases the subthreshold drive capabilities in PMOS. Moreover, channel and halo doping are tuned to calibrate our device with the fabricated NMOS device in [68] and its corresponding electrical characteristics are listed in Table 3.2.

To begin with, the simulation project is accurately matched with the process details of real structure by incorporating the physical parameters given in Table 3.1. The calibrated 45nm device structure is obtained as shown in Figure 3.2.

$(I_{DS}-V_{GS})$ and $(I_{DS}-V_{DS})$ characteristics are the primarily set as a target for calibration in device simulation. The calibration begins by adjusting the electrostatic in order to match subthreshold slope, drain current, and $I_{OFF}$. Finally, device measurements are tuned and matched to the calibrated device [68] by doping profiles adjustment in order to obtain the desired $I-V$ characteristics. The flowchart depicting the calibration
process is shown in Figure 3.3 [69]. Tuned mobility parameters are used for process calibration.

![Figure 3.2: Meshed structure of 45 nm NMOS.](image)

The matched calibrated electrical characteristics are obtained through Synopsys TCAD simulation utilizing Sentaurus workbench. The significant figures of merit, thus, extracted from simulation, are then compared with the experimental data given in Table 3.2. This marks the beginning of investigating the effect of physical and process parameters under subthreshold conditions.

<table>
<thead>
<tr>
<th>Device</th>
<th>Gate length (nm)</th>
<th>$T_{ox}$ (nm)</th>
<th>Junction Depth (nm)</th>
<th>Poly silicon thickness (nm)</th>
<th>Spacer thickness (nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>NMOS</td>
<td>35</td>
<td>1-1.2</td>
<td>20</td>
<td>150</td>
<td>52.5</td>
</tr>
<tr>
<td>PMOS</td>
<td>35</td>
<td>0.95</td>
<td>33</td>
<td>150</td>
<td>52.5</td>
</tr>
</tbody>
</table>
Table 3.2: Performance Parameter listing of Simulated Device with experimental one.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>[68]</th>
<th>This work (simulation)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>NMOS</td>
<td>PMOS</td>
</tr>
<tr>
<td>$I_{ON}$ ($\mu$A/$\mu$m)</td>
<td>676</td>
<td>272</td>
</tr>
<tr>
<td>$I_{OFF}$ ($n$A/$\mu$m)</td>
<td>100</td>
<td>100</td>
</tr>
<tr>
<td>SS (mV/dec)</td>
<td>86.1</td>
<td>92.3</td>
</tr>
</tbody>
</table>

Figure 3.3: Flowchart depicting calibration methodology [64].

3.3 Oxide and Channel Length Variations effects under subthreshold Condition

One of the key techniques to enable gate length scaling is to scale $T_{OX}$ [70]. Therefore, $T_{OX}$ scaling has been influential in controlling SCEs as MOS device dimensions get reduced. This improves the control of the gate electrode over the channel. As depicting in Figure 3.4, as $T_{OX}$ scales down, there is a marked increase in gate leakage
current which becomes significant below 65nm technology node. Moreover, gate capacitance also increases significantly with $T_{OX}$ scaling for superthreshold devices and circuits. In order to reduce the gate leakage, a gate dielectric with higher dielectric constant $k$ is introduced below 45 nm [71]. Due to lower supply voltage $V_{DD}$, gate leakage component, however is negligible under subthreshold as compared to superthreshold region of operation.

As shown in [72], the effective gate capacitance $C_g$ of a transistor is largely dominated by intrinsic depletion and parasitic capacitances that are strongly dependent on $T_{OX}$ variations.

![Figure 3.4: $T_{OX}$ scaling and gate leakage versus Intel technology [10].](image)

In power constraint subthreshold design of circuits, devices are normally optimized to enhance the speed [73, 74]. Reduction of capacitances can be achieved by using higher value of $T_{OX}$. This, however results in the reduction of the gate control over the channel. Moreover, it results in higher value of SS. Therefore, for moderate speed applications with little bit loss of energy, remarkable improvement in speed can be achieved. Furthermore, under subthreshold conditions with ($V_{GS} < 0.3$), $T_{OX}$ scaling does not increase gate capacitance $C_g$ significantly contrary to superthreshold region of operation as shown in Figure 8.5. The effective channel length also regulates subthreshold leakage current and $V_{th}$. Hence, this part of the section examines the combine effect of $T_{OX}$ and $L_g$ scaling on the performance of the device. As shown in Figure 3.2, the calibrated NMOS device, is simulated to explore the joint impact of $L_g$ and $T_{OX}$ on the NMOS device characteristics under subthreshold conditions at $V_{DD}$.
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=150mV. Variations in the values of \( L_g \) and \( T_{OX} \) are carried out from 30 nm to 50 nm and 0.6nm to 1.3nm respectively, whereas the values of halo and substrate doping are kept constant at 1.6e+19/cm\(^3\) and 2.2e+18/cm\(^3\), respectively. It can be deduced from Figure 3.6 that with an increase in \( L_g \) and a decrease in \( T_{OX} \), significant reduction in SS is observed. With the increase in \( L_g \) from 35 to 50 nm SS reduces by approximately 6mV/decade for different values of \( T_{OX} \). As seen from Figure 3.7, an increase in channel length has a minimal effect on the gate capacitance. Hence, longer channel length will result in lower power dissipation and better performance due to improved SS. Moreover, reduction in the value of \( T_{OX} \) from 1 to 0.8 nm at \( L_g = 35 \) nm reduces SS by 2.3mV/decade and an increase in \( C_g \) by 12%. Therefore, careful selection of \( T_{OX} \) is required so that the improvement in SS will not be masked by an increase in \( C_g \) and therefore, the power dissipation \((C_gV_{DD}^2f)\). It is obvious from Figure 3.7, that \( T_{OX} \) is having a larger impact on \( C_g \) as compared to \( L_g \). Furthermore, it can be observed that with an increase in \( L_g \), \( I_{ON} \) and \( I_{OFF} \) reduces by 14x and 22x, respectively, at \( T_{OX} = 1 \) nm. Accordingly, \( I_{ON}/I_{OFF} \) ratio increases by 1.36x at \( T_{OX} = 1 \) nm with the corresponding increase in \( L_g \). This also helps in the reduction of power consumption. Optimum value of \( L_g \) can be obtained from Figure 3.8, for better values of SS and \( I_{ON}/I_{OFF} \) ratio for various values of \( T_{OX} \). From the above investigation, it can be deduced that, for energy efficient ULP circuits and systems, larger value of \( L_g \) can be used to reduce the energy consumption due to smaller SS and higher \( I_{ON}/I_{OFF} \) ratio. Nevertheless, for high performance ULP applications, an increase in \( L_g \) will appreciably reduce the drive current and therefore the speed of the operation of the circuit. Hence, larger values of \( L_g \) are not feasible for high performance ULP applications.
Figure 3.5: Gate capacitance variation with $V_{GS}$ for 45 nm NMOS.

Figure 3.6: Subthreshold slope variation with $L_g$ and $T_{OX}$ for 45 nm NMOS.
Figure 3.7: Gate capacitance variation with $L_g$ and $T_{OX}$ for 45 nm NMOS.

Figure 3.8: Subthreshold slope and $I_{ON}/I_{OFF}$ variations with $L_g$ and $T_{OX}$ for 45 nm NMOS.
3.4 Doping Profile Variation Effects under Subthreshold Condition

It has been observed that in scaled superthreshold devices, halo and retrograde doping are used to suppress short channel effects (SCE) like DIBL and punchthrough effect [75]. Nevertheless, in subthreshold region, SCE plays a least significant role as compared to superthreshold region because of lower values of $V_{DD}$ [24]. Therefore, it has now been well established that halo and retrograde doping profiles are less significant under subthreshold regime. Furthermore, low doping profile levels can reduce the junction capacitance significantly. Hence, it is essential to explore the effect of doping profile under subthreshold conditions in nanometer technology nodes.

It can be observed from Figure 3.9 that with the reduction in substrate ($N_{sub}$) and halo doping, there is an appreciable increase in the drain current ($I_{sub}$). The decrease in $N_{sub}$ doping concentration by 50% increases $I_{sub}$ by 3.5x. Moreover, reducing $N_{halo}$ by 4x increases $I_{sub}$ by 2.25x. However, from Figure 3.10, it can be deduced that with the reduction in $N_{sub}$ by 50%, there is an increase in SS by 0.7mV/decade and $I_{OFF}$ by 3.88x. Hence, there is a trade-off involved in boosting the drive current, SS and $I_{OFF}$ on reducing $N_{sub}$ doping concentration. Similar observable trends in performance are observed by varying the halo doping concentration. Figure 3.11 and 3.12 exhibit the drain current ($I_{sub}$) and subthreshold slope (SS) as a function of halo and substrate doping.

![Figure 3.9: Drain current variation with channel doping for different halo dose.](image-url)
Figure 3.10: Subthreshold slope and $I_{OFF}$ variation with channel doping.

Figure 3.11: Drain current variation with halo doping.
Characterization of Device under Subthreshold Condition

This section deals with the subthreshold slope improvement so that power consumption can be reduced [24]. The calibrated device is then fine-tuned at optimum values of $L_g$, $T_{OX}$, $N_{sub}$ and $N_{halo}$ in order to achieve best subthreshold characteristics. Optimized device parameters from Section 3.4 are used to achieve better subthreshold slope under subthreshold conditions. Figure 3.13 shows the comparison of the subthreshold slope as a function of supply voltage for the standard and the optimized device under subthreshold condition.

As depicted in Figure 3.13, the optimized device showed a marked improvement of 9.89% in subthreshold slope over the traditional device operated in subthreshold region. Moreover, as depicted in Table 3.3, $I_{ON}/I_{OFF}$ ratio increases by 34% in case of optimized device for the same drive current. Since the effect of DIBL is very negligible under subthreshold conditions, therefore this work does not taken into account the DIBL effect during device optimization.
3.6 Summary

The device designed particularly for superthreshold region of operation is not worthy for optimum subthreshold region. This chapter proposed new device process parameters in order to improve the subthreshold slope and to enhance the speed of subthreshold devices and circuits. It has successfully presented the optimized device for subthreshold region which results in improvement in both the subthreshold slope and the $I_{ON}/I_{OFF}$ ratio. Therefore, in order to obtain the better device performance characteristics under subthreshold conditions, it is necessary to optimize the process and geometry parameters of Silicon MOSFET at nanometer technology node due to the relaxed constraint for different leakage currents and short channel effects.
The next chapter presents the design and optimization of ultra-low power CMOS based second generation current conveyor (CCII) in the subthreshold region at 32nm technology node. Optimal sizing of transistors for different designs has been done at low supply voltages.