ABSTRACT

For many “Big Data” applications, the limiting factor in performance is often the transportation of large amount of data from hard disks to where it can be processed. In this research work, a system architecture is designed which accelerates the performance of transporting, processing, storing and retrieving data when required at high speed. So, a high speed data transfer is required with high throughput. A very efficient way to achieve the same is the usage of PCIe interface or link that is capable of transferring data at high speed. It has been proven that it is a plug and play for the hosts using it. It requires no additional protocols or data integrity.

The system designed consists of a high density field-programmable gate array (FPGA) based architecture using PCI bus interface for high speed data transfer from the SDRAM for usage of BIG data analytics. The design is incorporated with programmable PCI master core which act as an interface between PCI bus and the internal logic design of FPGA. These days the requirement of memory is increasing day by day so the SDRAM is selected as the memory element for storage of data. A controller is necessary to control the operations of SDRAM. SDRAM controller is designed for high speed communication with PCI Bus that can handle huge amount of data and can be used for various storage related application such as BIG DATA.

In short, the objectives were to choose a proper memory element for storage of Big Data. Just determination of the storage capacity does not fill the need, but rather access to the information from the storage element is likewise important. So, an interface was essential which is equipped for exchanging information at higher data rate. At the point when more number of memory components are available a controller is required to have a control so the stream goes easy. So, a controller was intended to have control over the memory component. In any case, the availability between the memory components and the controller must be set up and this is accomplished by the idea known as Network on Chip.

The design developed is implemented on Xilinx Artix 7 FPGA and coded using Verilog language. Xilinx ISE 14.1 is used as a development environment and Modelsim6.3 is used to work on the functional verification of the design. The chip scope analyzer is also used for the functional verification of the hardware results generated.