CHAPTER 6

CONCLUSION AND FUTURE WORK

CGRA based SoC research is an emerging technique for programmable acceleration of high performance computation intensive processing kernels with word-level arithmetic. It is likely to be a never-ending story as the dynamic partial reconfigurable applications on the one side and the CGRA platform services on the other side. Hence, this chapter provides a concluding summary of the proposed works covered in this thesis and provide the possibilities of future enhancements. This chapter is organized as follows: - Section 6.1 briefly summarizes the thesis and presents the significant contributions and conclusions about each chapter of this thesis. Section 6.2 provides various possibilities to enhance the proposed work in future.

6.1 SIGNIFICANT CONCLUSIONS

Besides providing a novel CGRA design and its implementation space, this thesis introduces several novel mechanisms, algorithms and components. It can directly address the scalability, flexibility, programmability, predictability, a high performance and a low power consumption design methodology for performing real-time embedded applications running on a homogeneous multiprocessor CGRA. This includes dynamic partial reconfiguration management combined with fast and efficient resource allocation schemes, task migration mechanisms and policies, network-on-chip inter-connect communication management mechanism and polices and a quality management component for handling real-time embedded applications. A brief summary and achievements of each chapter is given below.
Chapter 1:
In this chapter, a brief introduction on reconfigurable technologies is presented. It gives more comprehensive idea about the coarse/fine grained reconfigurable architectures and various reconfigurable computing features like flexibility, scalability, power consumption and system performance. Also this chapter discusses about a collection of CGRA and FPGA solutions for run-time task migration and HW/SW co-design issues.

Chapter 2:
In this chapter, a novel homogeneous multi-processor based coarse-grained dynamic and partial reconfigurable system-on-chip architecture (MDPRA) is designed with 4 by 4 array of processing elements with local memory (DRPUs) and a network-on-chip interconnect communication mechanism (DRRUs) for wireless communication applications. This MDPRA platform consists of
(1) A modeling methodology which allows dynamic partial reconfiguration of the homogeneous blocks
(2) A synthesizable IP core dedicated to datapath oriented operations
(3) A customizable coarse-grained elements for accelerating embedded reconfigurable computing applications.
(4) An architecture-aware technology mapper to translate the dataflow graphs into mapped circuits which can be integrated into high-level synthesis tools
(5) A modeling methodology for hardware/software estimation, co-design, co-synthesize and co-verification techniques
(6) A novel dynamic partitioning, sorting and scheduling algorithms
(7) A chained micro-engine code generator to generate assembly codes for software partitions
(8) Dynamically generated arithmetic processors for power and area savings of CGRA
In this chapter, a highly challenging task is to compare the proposed MDPRA system with existing CGRAs because of the variation between design-tools on different reconfigurable architectures may yield entirely different results. Hence, system-level simulation methodology of CGRAs with high abstraction level is presented to build, simulate, evaluate, and tune models of real-time embedded applications. This high abstraction level simulation method improves the design time, increases the simulation speed and enables efficient architectural exploration.

The proposed MDPRA prototype system was simulated with Xilinx ISE system edition software, synthesized with Mentor Graphics’ Precision RTL Plus software and implemented with TSMC 90 nm technology. It consists of about 0.57 million gates with an average power consumption of 1.2 mW/MHz for the evaluated benchmarks. Performance analysis of the proposed MDPRA system with other CGRAs (like RAW, RaPiD, PipeRench and MATRIX) is given in the summarized form.

- MDPRA provides about 2x, 3x, 3x and 2x throughput gains against the RAW, RaPiD, PipeRench and MATRIX implementations, respectively.
- MDPRA consumes 18x, 2x, 4x and 2x less power than RAW, RaPiD, PipeRench and MATRIX implementations, respectively.
- MDPRA provides about 31x, 4x, 6x and 3x high energy efficiency than RAW, RaPiD, PipeRench and MATRIX implementations, respectively.

The results demonstrate that the MDPRA is a promising dynamic reconfigurable, low power and energy efficient platform for signal processing applications. Finally, chapter 2 also serves as a reference for the rest of the thesis.
Chapter 3:

In this chapter a new system-level architectural framework is presented for the multi-objective hypergraph based module partitioning problems to improve the system efficiency and to diminish the fault occurrences in CGRA based SoC systems. It exploits the techniques of module overlapping, temporal partitioning, dynamic partial reconfiguration and genetic algorithm engine. This work creates the virtual empty space when all the breathing spaces are occupied in the reconfigurable components by using swapping process. Here, the Late Acceptance Hill-Climbing Plus (LAHC+) algorithm is used for macro-node swapping process.

In Multi-objective optimization, more than one objective function have to be optimized simultaneously in the presence of trade-offs between two (or) more conflicting objective functions. Hence, it has the (possibly infinite number) Pareto optimal solutions (or) non-dominated solutions. Here, a special computer program acts as a decision maker to provide the Pareto optimal decision, which coincides with the objective function through the feedback process of mapping and refinement stages. The proposed system-level architectural framework uses the temporal partitioning technique to implement the module partitioning process.

The proposed architectural framework is tested on a full-set of ISPD'98 benchmark suite. Experimental results have showed that the proposed scheme is quite efficient than that produced by the hMETIS recursive bisection partitioning method in terms of minimization of cut and maximum degree and also maximization of node gain value. As a result, this SoC framework attains more than ‘14 times’ enhanced speed over the software execution.

The results demonstrate that this proposed system-level architectural framework is most suitable for high-quality SoC-based control-dominated applications.
Chapter 4:

This chapter describes the design and realization of a digital MIMO-OFDM based software defined radio system – a real-time embedded computing application as proof-of-concept implementation and demonstration for previous chapters.

Modern wireless communication systems are progressing towards MIMO-OFDM based cognitive radio (CR) and long-term evolution (LTE) technologies. Cognitive radio system is capable of conscious of its surrounding environment and dynamically adapting it’s internal states to achieve optimal performance by making changes in certain operating parameters like transmit power, carrier frequency and modulation strategy. Hence, the design of cognitive radio is going towards software-defined radio (SDR) platform which is a fully reconfigurable wireless transceiver with dynamic adaptation of communication parameters based on the user demands. It provides high reliable communication and efficient utilization of the radio spectrum. In this thesis, a novel digital MIMO-OFDM transceiver architecture was designed to implement adaptive (or) dynamic multi-standard multi-mode wireless communication systems (i.e. Software Defined Radio) on homogeneous CGRA based System-on-Chip.

The proposed MDPRA/ADRES reconfigurable-SoC based digital MIMO-OFDM transceiver architecture is functioning on the concept of dynamic reconfiguration. It can able to utilize the same software and hardware modules for different logics and algorithms using dynamic partial reconfiguration. Hence, this proposed method can provide greater flexibility to add new features (or) modules, without requiring additional cost of software and hardware. Also, the performance of this transceiver architecture is improved by a new algorithm called the radix-2^5 modified booth encoding (MBE) algorithm for FFT/IFFT unit. In addition, a phase locked loop (PLL) and a real-time controller (RTC) are added to minimize the fault occurrences in signal processing techniques.
Performance of the proposed radix-2\(^5\) modified booth encoding (MBE) algorithm is evaluated through mathematical analysis and computer simulations. It shows that the proposed algorithm improves the performance of digital MIMO-OFDM transceiver architecture with low complexity in dense multipath environments.

The proposed digital MIMO-OFDM transceiver architecture is successfully simulated in MATLAB/SIMULINK environment and effectively implemented on Xilinx Virtex 5 FPGA based MDPRA/ADRES reconfigurable processors. The efficiency and performance of this implementation has been verified in software as well as in hardware. It can able to provide at least two times greater performance than previous works in terms of throughput (about 2.4 Gsample/s for both MDPRA and ADRES), latency (about 2.897ns and 2.941ns for MDPRA and ADRES respectively) and area utilization (about 25k and 27k logic gates for MDPRA and ADRES respectively).

**Chapter 5:**

This chapter combines the MDPRA system (chapter 2), multi-objective module partitioning system (chapter 3) and novel digital MIMO-OFDM transceiver architecture (chapter 4) concepts to provide a proof-of-concept demonstration for a complete software defined radio platform.

This chapter provides a detailed experimental study of coarse-grained reconfigurable system-on-chip based software defined radio on top of the FPGA. The various experimental achievements of the proposed work are listed below.

- This work achieves greater functionality with a simpler hardware design. It can be possible by DPR process to reduce the cost of additional features when not all of the logics are used at all times.
This work uses efficient software management of the reconfigurable hardware against the traditional embedded processor (or) microcontroller based system.

The trade-off between maximization of the resource utilization percentile with higher operational speed and minimization of the dynamic power consumption is handled in proficient way.

The optimization of hardware architecture is greatly achieved by the DPR process of pipelining & parallel processing techniques at run-time of the system.

The circuit and function of the reconfigurable system can be customized in application level and phase level over time.

The proposed coarse-grained reconfigurable system-on-chip based SDR architecture supports dynamic and partial reconfigurable embedded systems. This work deals with BPSK, QPSK, 16-QAM and 64-QAM based SDR wireless communication system. The DPR implementation results show that this dynamic and partial reconfigurable CGRA based SDR provides greater flexibility to add new features (or) modules, without the additional cost of software and hardware using preemption and relocation techniques.

This proposed system has been successfully simulated in the Agilent SystemVue environment and emulated in the MDPRA, MOLEN, MORPHOSYS and ADRES reconfigurable SoC model on top of the Xilinx Virtex 5 FPGA based XUP development board. The efficiency and performance have been verified in software as well as in hardware level. As per the power, area and speed requirements and low circuit-complexity, the MDPRA SoC architecture is a best option for SDR realization compared to MOLEN, MORPHOSYS and ADRES SoC architectures. Also in the aspect of dynamic and partial reconfiguration property, MDPRA SoC architecture is a best choice for SDR realization compared to others.
The results demonstrate that the proposed MDPRA system-level architectural framework with multi-objective module partitioning technique is most suitable for high-quality, control-dominated, low power and energy efficient platform for signal processing (like MIMO-OFDM and software defined radio based wireless communication) applications.

6.2 FUTURE EXPANSION AND SCOPE

This dissertation obviously presents only a small portion of the ever-evolving overall multiprocessor CGRA based SoC architecture puzzle. Here, each chapter approaches with its own set of assumptions and limitations. Most of the producible solutions are validated and still some of the architecture based solutions, application assumptions and limitations require validations. It offers scope for extending the research further and gain more insights. Some of the important such issues are given below.

- The future system-on-chip technology for long term evaluation (LTE) based wireless communication needs a strong run-time partial reconfigurable coarse-grained architecture.
- Though the dynamic generated arithmetic processor (DGAP) unit is automatically generated at run-time based on the functional requirements, it has a fixed processing elements and it does not consider the complete utilization of that DGAP.
- The MDPRA design may be modified to solve the inter-module communication and its routing issues during the partitioning process.
- The system integration module needs further improvement for better performance of the MDPRA based real-time embedded computing applications.
In the Genetic algorithm engine, real-coded chromosome representations may be used to replace the binary-coded symbol to reduce the necessity of external memory storage.

In the system-level exploration, a separate local search engine may be incorporated to increase the processing speed.

In wireless communication, there may be chance of collapse and/or distortion of signals in the digital SoC transceivers. It may be controlled by a real-time fault tolerance functional system.

The symbol timing error estimation and fine frequency estimation processes may be analyzed and improved in the synchronization of the MIMO-OFDM transceiver architecture.

The adaptation of multi-user MIMO technique in SDR realization may improve the overall system performance.

The CGRA based SDR system may be worked along with the wireless open-access research platform (WARP).