CHAPTER 5

HARDWARE IMPLEMENTATION OF TLDCI FED INDUCTION MOTOR WITH DTC-SVM

5.1 INTRODUCTION

This chapter deals with the hardware implementation of three level diode clamped inverter fed induction motor using DTC-SVM control along with the detailed description about various components used in the hardware setup. The closed loop performance analysis of the motor drive is carried out in detail for various load conditions.

5.2 CIRCUIT DESCRIPTION

The block diagram for the closed loop control of TLDCI fed IM using DTC-SVM technique is shown in Figure 5.1. It consists of one optocoupler, voltage and current sensors, speed sensor, frequency to voltage converter (F/V), signal conditioner, protection circuit and DSP processor. The optocoupler is used for isolating the input PWM signals between the FPGA processor and the power circuit of diode clamped inverter. Voltage and current sensors are used to measure the dc link voltage, dc link current and line current of the diode clamped inverter. The Hall Effect sensors are used for sensing the current and voltage. Hall Effect current transducers sense the currents $I_d$, $I_a$, $I_b$, $I_c$ and one hall effect voltage transducer senses the DC link voltage ($V_d$).
Figure 5.1 Block diagram of closed loop control TLDCI fed induction motor with DTC-SVM

The speed sensor is used to measure the speed of the induction motor in terms of frequency of square wave which is fed to a frequency to voltage converter circuit. The signal conditioner circuit is used to convert the current and voltage signals compatible with the protection circuit and the ADC of the DSP processor. The protection circuit is used to provide protection against over voltage, over current and under voltage. The current and voltage obtained from signal conditioners are given to the ADC inputs DSP. The space vector modulation scheme is implemented in DSP processor. The output of a PI controller generates reference torque using speed error as an input. The actual torque and flux are compared with the corresponding reference values in the DSP processor to get the voltage reference $V_{qs}^*$. 
5.2.1 Current Sensor

The current is sensed using LTS 25-NP transducer which is capable of measuring DC, AC and impulse currents with a galvanic isolation. The transducer presents a multi-range configuration designed for nominal currents of 8, 12 and 25 Amps. Multitude of connection options are integrated allowing the users to make direct or differential current measurement. The advantage of the LTS 25-NP is that it is capable of measuring currents with magnitude more than 3 times INPUT values. Thus, the peak currents up to 25.6A, 38.4A and 80 A can be measured for different ranges. The unique features of the LTS 25-NP transducer over the traditional Hall Effect transducer are its miniature size (9.3x22.2x24 mm), intrinsic accuracy of +/-0.2%, an excellent linearity of less than 0.025% and a bandwidth from DC to 200 kHz. The LTS 25-NP with very low temperature drift of 50 ppm/K are supplied with a unipolar power supply of +5V, while still having the capacity to measure both positive and negative currents. In addition, a measuring resistor of 0.5% accuracy has been incorporated which is characterised by a very low temperature drift; this provides the voltage output directly. The output is set at 2.5V at zero primary current with a variation span of 0.625 V at nominal current. Thus the transducer can directly be connected to the 5 Volt inputs of microcontrollers, A/D converters and instrumentation cards. The main features of LTS series are that it offers a closed-loop transducer based on an ASIC as shown in Figure 5.2.
The output voltage is generated across the measuring resistor ($R_{IM}$) which is integrated in the transducer. For a given primary current, the value of the output voltage can be calculated as

$$V_{OUT} = V_{REF} + I_S R_{IM}$$

$$I_S = \frac{I_P}{N_S}$$

$$V_{OUT} = V_{REF} + \frac{I_P}{N_S} R_{IM}$$

The range of the closed loop LTS transducers permits the measurement of nominal currents $I_{PN}$ from a few amperes to several tens of kA, with an accuracy of about 1%. The value of primary-current/output voltage ratio is determined by the resistor $R_{IM}$. The reference point is exactly half the supply voltage. The output voltage as a function of the primary current is represented in Figure 5.3.
Figure 5.3 Output voltage $V_o$ Vs primary current $I_{pm}$

There are three different input voltage ranges via selection pins as 6V, 15V and 25V. The current transducer has excellent precision, good linearity and low temperature drift. The current transducer of LTS 25-NP is shown in Figure 5.4 and its specifications are given in Table 5.1.

Figure 5.4 Current Transducer LTS 25-NP
### Table 5.1 Specifications of LTS25-NP

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Accuracy</td>
<td>±0.2%</td>
</tr>
<tr>
<td>Frequency Bandwidth</td>
<td>DC 100-200Khz</td>
</tr>
<tr>
<td>Input Current Range</td>
<td>±80A</td>
</tr>
<tr>
<td>Maximum cable diameter</td>
<td>3.2mm</td>
</tr>
<tr>
<td>Maximum operating temperature</td>
<td>+85°C</td>
</tr>
<tr>
<td>Minimum operating temperature</td>
<td>-40°C</td>
</tr>
<tr>
<td>Mounting type</td>
<td>PCB</td>
</tr>
<tr>
<td>Overall depth</td>
<td>10mm</td>
</tr>
<tr>
<td>Overall height</td>
<td>24mm</td>
</tr>
<tr>
<td>Overall width</td>
<td>22.2mm</td>
</tr>
<tr>
<td>Sensor type</td>
<td>Closed Hall Effect</td>
</tr>
<tr>
<td>Output Voltage</td>
<td>5V</td>
</tr>
</tbody>
</table>

The PCB diagram of current transducer LTS25-NP used in the hardware is shown in Figure 5.5. To measure the three phase currents ($I_a$, $I_b$, and $I_c$) and dc link current $I_d$, four current transducers are used.

![Figure 5.5 PCB layout for current transducer LTS 25-NP](image-url)
5.2.2 Voltage Transducer

Voltage Transducer is realised by a current transducer assembly with large number of turns. This permits the realization of necessary ampere-turns for the creation of the primary induction with a low primary current, thus consuming minimal power. The circuit current is shunted through a resistance connected in series with the primary winding. This resistance can be external or integrated into the transducer construction. The LV25-P is a Hall Effect closed cycle transducer which works with DC or AC signals up to 500 V as shown in Figure 5.6. It has galvanic isolation between the primary circuit (high voltage) and the secondary one (electronics) and a theoretical conversion factor of 2500:1000. It needs a power supply between ±12 and ±15V. It has an excellent precision and an accurate linearity.

![LV25-P Transducer](image)

**Figure 5.6 Voltage transducer LV25-P**

The voltage sensor needs a resistance in series with the “+HT” terminal to produce a current which should be in the order of 10 mA. Since the phase effective voltage is 230 V, a resistance of 22 kΩ is used in the present work. The sensor output is also a current out of terminal “M” (25 mA) which is converted to a voltage with 100 Ω resistances.
### 5.2.3 Signal Conditioner Circuit

The basic block diagram of signal conditioner circuit is shown in Figure 5.7. The function of the signal conditioner is to collect the current and voltage signals from the respective sensors and to transfer the same as appropriate voltage signals to the protection circuit and the ADC inputs of the DSP processor.

![Block diagram of signal conditioner](image)

*Figure 5.7 Block diagram of signal conditioner*
DC link voltage is sensed using the Hall Effect voltage sensor and the output of that transducer is given to the inverting amplifier. Then, its output is connected to another inverting amplifier where the gain of the amplifier is adjusted using a trim pot. Then the amplified input is compared with the reference voltage via comparator whose output is connected to the hardware protection unit and also to the ADC channels of DSP processor.

DC link current $I_{d}$ is measured and given to the non-inverting amplifier where the offset voltage can be adjusted using the trim pot. Then the gain is adjusted in the second amplifier. The dc current is passed through the active filter and its output is connected to ADC channel of the DSP Processor. The current $I_{dc}$ is compared with a reference value using a comparator and its output passed on to the hardware protection unit.

![Figure 5.8 Circuit diagram of operational amplifier TL084 circuit](figure)

The line current signals are passed through the inverting amplifiers through pin 2 as shown in Figure 5.8. The first one is used for correcting the offset in the input signal and the second amplifier is used for adjusting the gain of the signals. These conditioned currents signals are converted to volts and connected to the ADC inputs of the processor. The op-amp TL084 is high-speed JFET quad operational amplifiers in a monolithic integrated
circuit. The devices have high slew rates, low input bias and offset currents, and low offset voltage temperature coefficient.

### 5.2.4 Protection Circuit

Protection circuit is used to provide protection against over voltage, over current and under voltage. The schematic diagram of protection circuit of IPM based power module is shown in Figure 5.9. The output current and voltage from signal conditioners are the input signals for the master / slave JK Flip flops whose outputs are connected to transistors Q1 and Q2.

![Figure 5.9 Schematic diagram of protection circuit](image)

The output transistor Q1 drives the control inputs of PWM- AND gates. Other inputs of AND gates are connected to PWM outputs of DSP. These outputs of AND gates drive the input of optocoupler. The output signal of optocoupler is fed to the input of the base driver. The optocoupler output is ANDed with Q1 output signal in the ANDP gate to generate interrupt signal PDP-INT for DSP.
5.2.5 OptoCoupler

The function of Optocoupler is to isolate the control circuit from the power circuit. Pulse width modulation signals (PWM 1 to PWM 12) obtained from DSP Processor is passed to the power circuit through protection circuit and optocoupler. The optocoupler schematic diagram is shown in Figure 5.10.

![Figure 5.10 Schematic diagram of optocoupler](image)

The PWM signals obtained from the protection circuit are given as input to the optocoupler and driver circuit. The optocoupler and driver circuit produce gate and source signals which are switching signals to the inverter.
Optocoupler is a component that transfers electrical signals between two isolated circuits by using light. The output of AND gate is connected as input to the pin 2 of photo coupler with the pin 3 connected to ground as shown in Figure 5.11. The pins 8 and 5 are connected to +15volt and ground (F) respectively. The output of the photodiode is connected as an input to the driver circuit to get an output of 15 volt.

![Image of TLP250 optocoupler]

**Figure 5.11 PCB layout of TLP250 optocoupler**

### 5.2.6 Speed Sensor

The enhanced quadrature encoder pulse (eQEP) module is used for direct interface with a linear or rotary incremental encoder to get position, direction, and speed information from a rotating machine. As the encoder disk rotates, the two photo-elements generate signals that are shifted by 90° out of phase from each other. These are commonly called QEPA and QEPB signals. The clockwise direction for most encoders is defined as the QEPA channel going positive before the QEPB channel and vice versa as shown in Figure 5.12

The encoder wheel typically makes one revolution for each rotation of the motor or the wheel may be geared with respect to the motor. Therefore,
the frequency of the digital signals from the QEPA and QEPB vary proportionally with the speed of the motor. For example, a 2000-line encoder directly coupled to a motor running at 5000rpm results in a frequency of 166.6 KHz. The output frequency of either the QEPA or QEPB can determine the speed of the motor.

Figure 5.12 QEP encoder output signal for forward/reverse movement

The HEDM-5605 translates the rotary motion of a shaft into pulse output. As seen in Figure 5.13, these encoders contain a single LED as its light source. The light is collimated into a parallel beam by means of a single lens located directly over the LED. Opposite to the emitter is the integrated detector circuit. This IC consists of multiple sets of photo detectors and the signal processing circuitry necessary to produce the digital waveforms. The code wheel rotates between the emitter and detector, causing the light beam to be interrupted by the pattern of spaces and bars on the code wheel. The photodiodes, which detect these interruptions, are arranged in a pattern that depends on the radius and design of the code wheel. These detectors are also spaced such that a light period on one pair of detectors corresponds to a dark
period on the adjacent pair of detectors. The photodiode outputs are then processed resulting in outputs \( A, \overline{A}, B \) and \( \overline{B} \). The comparators receive these signals and produce the final outputs for channels A and B which are in quadrature. The output signals I and T are compared to get a signal to the index processing circuitry along with the outputs from channels A and B.

![Diagram of QEP (HEDM-5605) block diagram](image)

**Figure 5.13 Block diagram for QEP (HEDM-5605)**

The output of the channel I is an index pulse (PO) which is generated once for each full rotation of the code wheel.

### 5.3 POWER CIRCUIT FOR TLDCI

The power circuit board of TLDCI is shown in Figure 5.14. The PWM pulse for IGBT power circuit obtained from the DSP processor is fed as one of the input signal to the gate CD4081. The current signal \( C_1 \) obtained
from the protection circuit is given to the control input of CD4081. Whenever the current $I_{dc}$ is below 6A, the signal $C_1$ becomes high, and the pulse to the inverter is enabled. If the current is above 6 A then the signal $C_1$ becomes low and pulses are blocked.

Figure 5.14 TLDCI power circuit for phase A of 0.75kW induction motor

The IC CD4081B contains four independent 2-input AND gates. The output of CD4081B drives the photo coupler TLP250. The PWM input generated from the FPGA processor and the current signal $C_1$ generated from the sensor for $I_{dc}$ are the two input signals to the gate which needs a power supply of 5 volt to produce a 5 volt output. The output voltage of photo
coupler is passed through 47ohm resistance in order to have high amplitude during the turn on period of IGBT. An 18V zener diode is provided across the driver circuit to protect the gate when the voltage exceeds 15 volt. A 100 ohm resistance connected in series with diode reduces the voltage during the device turn off. In order to keep the circuit at reset condition a pull down resistance of 47KΩ is connected across the gate circuit. A snubber circuit is connected across the IGBT for $\frac{dv}{dt}$ protection. (R=47KΩ, C=0.1 μF).

5.3.1 Comparator and Flip-flop Circuit

The output voltage obtained from the TL084 op-amp circuit is fed to the comparator circuit to trigger the flip-flop in the protection circuit. The comparator produces an output voltage of 5V (High) which is used as a set input for the JK flip-flop as shown in Figure 5.15.

The CD4027BC dual J-K flip-flops are (CMOS) integrated circuits constructed with N and P-channel enhancement mode transistors. These flip-flops are edge sensitive to the clock input and change state on the positive-going transition of the clock pulses. Set or reset are independent of the clock and is accomplished by a high level on the respective input.

When set bit value becomes 1, Q takes logic 1. When Q is high the LED starts glowing and this indicates the wrong logic sequence. When set value becomes low the reset becomes active producing high Q output. The Q output is given to the control current C₁ to the gate CD4081B in the power circuit.
Figure 5.15 Circuit diagram of comparator and flip flop circuit
5.4 SWITCHING PULSES FOR TLDCI FED INDUCTION MOTOR

The waveforms of switching pulses for phase A of TLDCI using SVM technique are shown in Figure 5.16.

![Switching pulses for phase A using SVPWM technique](image)

Figure 5.16 Switching pulses for phase A using SVPWM technique

DSP processor is used to generate PWM signals for the TLDCI fed induction motor. The processor has total 676 I/O pins with 80 pins used for integrating the peripherals like LED, Switches etc. The balance 110 pins are available to the user. It has on board programmable oscillator from 3MHz to 200 MHZ with ADC and DAC interfaces. The processor has one 8 channel 12-bit ADC and two numbers of 2 channel 14-bit DAC. The AD7266 is a dual, 12 bit, high speed, low power, 8 channel successive approximation type ADC that operates from a single 2.7 V to 5.25 V power supply. The device
contains two ADCs, each preceded by a 3-channel multiplexer, and a low noise, wide bandwidth track-and-hold amplifier that can handle input frequencies in excess of 30 MHz. The 3 channels are used for sensing the line current $I_a$, $I_b$ and $I_c$ of the induction motor. The DAC8802 is a dual, serial input 14-bit current-output DAC which operates from a single 2.7V to 5.5V supply. The device contains double-buffered, serial data interface which offers high speed, 3-wire SPI interface up to 50 MHz and also enables simultaneous multi channel update. The features of the DAC device include separate four multiplying reference inputs, 10MHz reference bandwidth and internal power on reset. DAC has 6 output ports and one of them is used for generating 12 SVPWM signals for TLDCI fed induction motor. The pulse has been generated using XILINX Software. The algorithm for the controller is discussed below.

**Algorithm**

**Step 1:** Read the current $I_a$, $I_b$, $I_c$ and speed from the TLDCI fed Induction motor.

**Step 2:** Estimate the d and q-axis current and dc link voltage.

**Step 3:** Estimate the value of torque and flux

**Step 4:** Get the speed error from the actual speed and set speed of motor

**Step 5:** Multiply the error obtained from step 4 with the calculated value of $K_p$

**Step 6:** Integrate the error obtained from step 4 and then multiply it by $K_i$ value

**Step 7:** Add the values from step 5 and step 6 to get the reference torque.

**Step 8:** Repeat step 4 to step 7 for the PI controllers for flux and Torque to obtain $V^*_{qs}$ and $V^*_{ds}$.

**Step 9:** The d-axis and q-axis voltage are transformed to $V_a$ and $V_B$.

**Step 10:** The $V_a$ and $V_B$ are used for generating SVPWM switching pulses for TLDCI fed induction motor.
5.5 PERFORMANCE ANALYSIS OF TLDCI FED 0.75kW INDUCTION MOTOR WITH DTC-SVM

The induction motor fed from TLDCI fed IM with DTC-SVM control is started under no load. The measured phase and line voltage waveforms are shown in Figures 5.17 and 5.18. The no load current waveform is shown in Figure 5.19.

![Figure 5.17 Phase A voltage of TLDCI under no load](image)

Figure 5.17 Phase A voltage of TLDCI under no load

![Figure 5.18 Line voltage V_{ab}](image)

(a) Line voltage $V_{ab}$

Figure 5.18 (Continued)
Figure 5.18 Line voltages of TLDCI on no-load

(b) Line voltage $V_{bc}$

(c) Line voltage $V_{ca}$
A load of 5Nm is applied at 0.25 seconds and then the load is reduced to 3Nm at 0.4 seconds. The corresponding torque response is shown in Figure 5.20. The torque ripple measured for 5Nm torque is 21.42%.

Figure 5.20 Torque response of 0.75kW IM for changes in load torque $T_L$ at 0.25 sec and 0.45 sec
The Figures 5.21 and 5.22 show the line voltage waveforms and the line current waveforms for a load torque of 3Nm.

(a) Line voltage $V_{ab}$

(b) Line voltage $V_{bc}$

(c) Line voltage $V_{ca}$

Figure 5.21 Line voltages of TLDCI for $T_L=3$Nm
Figure 5.22 Line current waveform of TLDCI for $T_L=3\text{Nm}$

The speed response is shown in Figures 5.23 for a reduction in load torque at $t=0.45$ sec. It is clear from the speed response that the drive maintains the set speed 1500rpm even during load variations. The magnitude of torque ripple is shown in Figure 5.24 for 5Nm load torque. The torque ripple varies between 6.2Nm and 4.3Nm with ripple content about 21.42%.

Figure 5.23 Speed response when $T_L$ changed from 5Nm to 3Nm at 0.45 sec
Figure 5.24 Torque ripple at 5 Nm load torque for set speed 1500rpm

The magnitude of torque ripple is shown in Figures 5.25 and 5.26 for 5Nm load torque for set speeds of 1000 and 1200rpm. The ripple content is about 23.8% and 22.12%. The corresponding values obtained from the simulation are 24.3% and 22.34% which are very close to the experimental results and hence validated.

Figure 5.25 Torque ripple at 5 Nm load torque for set speed 1000rpm
Figure 5.26 Torque ripple at 5 Nm load torque for set speed 1200rpm

The snap shot of the experimental set up is shown in Figure 5.27.

Figure 5.27 Experimental set up of 0.75kW IM
5.6 CONCLUSION

The hardware implementation of TLDCI fed 0.75kW IM with SVM-DTC control using DSP processor is explained in detail. The voltage and current waveforms under no load were captured using power analyser. The speed and torque responses for change in load torque are also captured and analysed. From the analysis, it is very clear that the motor drive follows the set speed very closely for the step change in load torque. The ripple is 21.42% for 5Nm torque in the experimental setup and the ripple content measured with simulation is 21.78% for the same load. This validates the simulation model and hence the results obtained for any other machine from the simulation can be taken as the experimental result. However, the ripple content is very high and cannot be appreciated. An attempt is made to reduce the ripple content with fuzzy logic controller which is considered in the next Chapter.