ABSTRACT

In modern VLSI circuits a single IC consists of several transistors. As semiconductor devices are more sensitive to physical faults, it is quite essential to test and monitor the functioning of IC before initialization of any system. Here lies the importance of Built-in-self Test (BIST), which generates the test patterns that are capable of covering the different faults that can be expected to occur in Circuit under Test (CUT). In general, the functioning of BIST is application of test patterns to the CUT to detect the faults that are present in CUT. The Ideal/Universal BIST applies all different possible combinations of test patterns to achieve very high fault coverage (100%). For e.g. if the CUT is of three input it applies $2^3$ different combinations from 000 to 111 to achieve very high fault coverage. However, in CMOS logic style a significant amount of power consumption is occurred due to presence of transitions. The increase in number of transitions will proportionally increase the power consumption. However general BIST may yield satisfactory results for shorter lengths of test patterns (i.e., CUT with less inputs), and as the length of test pattern increases (inputs of CUT increase) the probability of occurring transitions also increases and this increase in transitions may further increase power dissipation and this may lead to damaging of CUT. Hence the principle of general BIST does not yield successful results for longer lengths of test pattern and further it will reduce the life span of system.

Thus the reduction of power consumption for longer lengths of test patterns is major concern in BIST TPG. A numerous techniques such as running test activity at lower frequency, scan chaining ordering, X filling techniques, test scheduling schemes, scan segmentation into multiple scan chains, static compaction, design of low power BIST TPGs by employing extra hardware logic to random test pattern generators were developed earlier with an aim of reducing the power consumption during BIST operation. Even though there are many methods that work on the principle of reducing power dissipation during the BIST activity, all or many of these methods aims to reduce power dissipation by reducing the transitions that are associated with one or few blocks BIST TPG but not with all blocks that are associated with BIST TPG. By careful investigation further improvement in power...
consumption can be achieved by reducing the transitions that are associated with BIST TPG. Here an attempt is made to achieve maximum power savings by suppressing the transitions that are associated with different modules of BIST TPG. However, these BIST schemes suffer from drawback of reduced fault coverage. On the other hand a number techniques such as deterministic testing, assignment of weights to pseudorandom test patterns, grouping of test vectors were developed with the aim of increasing the amount of fault coverage associated with BIST TPGs and these BIST TPGs suffers from drawback increased power consumption.

This research work will concentrate on developing a new BIST TPG which is efficient with respect power and area by achieving 100% fault coverage. The proposed BIST TPG comprises two BIST TPGs namely, Low Transition BIST and Adder based 3Weighted Random BIST. The Low Transition BIST aims at reducing the power consumption during the BIST activity and aids to fault coverage by detecting the easy to detect faults. Detection of these easy to detect faults is done based on the fact that they are more sensitive to random test sequences. These random sequences are obtained by employing random test sequence generators such as LFSR and the test patterns generated from the LFSR is modified to achieve reduction in the number of transitions.

Adder based 3Weighted Random BIST aims at achieving the improvement with respect to fault coverage and area overhead. The improvement to fault coverage is achieved by detecting the hard to detect faults by employing deterministic test patterns and improvement in area overhead can be achieved by developing the fixing logic which alters and assigns weights to the pseudorandom sequences generated by BSLFSR. The testing of CUT by the proposed BIST TPG is carried out under two phases. First phase of testing is done by Low Transition BIST which achieves a significant amount of power consumption during the BIST activity by reducing different types of transitions that are associated during the BIST activity like, transitions occurring at the input of the scan chains, inherent transitions associated with pseudorandom sequence generator, transitions that are occurred during loading of test vectors and transitions that are occurred at capturing the test response and the second phase of testing is carried out by A3WRBIST to detect the faults that remain
undetected during first phase of testing. A Multiplexer is employed to select the appropriate BIST TPG based up on the selection lines in the implementation.

The performance of proposed BIST TPG is analyzed by testing various standard ISCAS’89 benchmark circuits which can be found in almost all digital and signal processing applications.

The functional behavior of proposed hybrid structure is analyzed by using Modelsim 6.2. The front end is carried out by using Xilinx 14.2. From the front end design various parameters of proposed BIST TPG such as power, area, and delay are estimated.

The back end design of the proposed BIST TPG is carried out at 90nm technology by using Dsch tool and Microwind. The Dsch tool is used create CMOS schematic of proposed BIST TPG and after getting through the functional verification of CMOS schematic of proposed BIST TPG, layouts were generated using Microwind. By using Microwind tool various parameters of proposed BIST TPG such as parasitic capacitances, actual number of PMOS and NMOS transistor required to build the proposed BIST TPG, number of routing wires employed in the building the proposed BIST TPG and number of logic cells required to build proposed BIST TPG are estimated. The parameters like Maximum $I_{DD}$, Current, Frequency of the output node, raise delay, fall delay and actual area that can be occupied on the chip at 90nm technology were estimated from the layouts generated by Microwind.

Additionally the physical design of the proposed hybrid test pattern generator is carried out by ICC complier of synopsis tools. The analysis of implemented results of proposed hybrid type BIST TPG clearly reveals the fact that it is successful in achieving improvements in all aspects of modern VLSI such as reduction in power consumption, decreasing area overhead and marginal improvement with respect to speed.