Chapter 6

Current-mode Neural Circuit for Solving Linear Equations
6.1 Introduction

The term “current-mode processing” was coined by Barrie Gilbert when he worked on strict translinear loops in which the node voltages are incidental [157]. Current-mode circuits are therefore those circuits which exploit current as the main operating parameter i.e. the individual circuit elements should interact by means of currents, and not voltages. Alternatively, current-mode circuits are those where information is represented by the branch currents of the circuits as opposed to nodal voltages in the case of voltage-mode circuits. Such circuits have received considerable research attention owing to the possibility of large dynamic range, wider bandwidth, greater linearity, simple circuitry, low power consumption and less chip area [58, 157]. Another advantage is that the summing of many signals is most readily accomplished when the signals are currents [58]. Therefore, as was to be expected, a lot of research efforts have gone into combining the advantages of ANNs and CM circuits [152, 175, 5, 14, 40].

A current-mode neural circuit, employing non-linear feedback is presented which, apart from enjoying the advantages of the NOSYNN architecture like avoidance of penalty parameters, simpler circuitry and a transcendental energy function, also benefits from the advantages inherent in current-mode processing. A new current-mode energy function has been postulated for the proposed circuit which uses only multi-output Current Differencing Transconductance Amplifiers (CDTAs), to realize weighted neurons unlike its predecessor where opamps were used to realize neurons and transconductance blocks formed the synapses interconnecting the neurons.

This chapter is organized as follows. A brief introduction to the Current Differencing Transconductance Amplifier (CDTA) appears in section 6.2. Section 6.3 comprises of the details of the proposed CM feedback neural network along with the design equations and the Energy Function of the circuit. Proof of the validity of the energy function is also provided. In the same section, it is also shown that the stable state of the network corresponds exactly with
the solution of the given system of linear equations. Section 6.4 presents the results of SPICE simulations of the circuit for problems of varying sizes. A discussion on performance evaluation and VLSI implementability of the proposed circuit appears in section 6.5. Lastly, conclusive remarks appear in section 6.6.

6.2 Current Differencing Transconductance Amplifier (CDTA)

The Current Differencing Transconductance Amplifier (CDTA) was introduced as an active building block for current-mode processing in 2003 [17]. Since its inception, the CDTA has been put to various applications in the field of analog signal processing [17, 18, 158, 148, 19]. However, the present work is the first attempt to employ CDTA as the active element in current-mode neural networks. As shall become evident in later sections, the use of CDTAs ensures resistor-less realizations of neural networks and therefore is suitable for high-level integration. The schematic symbol of the CDTA is shown in Figure 6.1. The terminals \( P \) and \( N \) accept current inputs. These input currents are then used to produce a difference current which is transferred to the \( Z \) terminal and the voltage at the \( Z \) terminal is converted into output current by a multi-output transconductance stage. The port relations characterizing CDTA are given by

\[
\begin{bmatrix}
V_P \\
V_N \\
I_Z \\
I_{X^+} \\
I_{X^-}
\end{bmatrix} = \begin{bmatrix}
0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 \\
1 & -1 & 0 & 0 & 0 \\
0 & 0 & +g_m & 0 & 0 \\
0 & 0 & -g_m & 0 & 0
\end{bmatrix} \begin{bmatrix}
I_P \\
I_N \\
V_Z \\
V_{X^+} \\
V_{X^-}
\end{bmatrix}
\]

For the purpose of use in the proposed current-mode neural circuit, multi-output CDTAs are needed with only X+ type of outputs. Although the schematic in Figure 6.1 shows only one X+ output, the number of such outputs may readily be increased by replicating the output stages in the actual circuit implementations of the CDTA [18]. Such a replication of output stages
has also been done for Current Conveyors, Current-Controlled Conveyors and Differential Voltage Current Conveyors, where multiple outputs were required [19]. Next, an equivalent model of the CDTA is presented in Figure 6.2, which shall prove to be helpful in understanding the operation of the proposed circuit for solving linear equations. Toward that end, we begin by asserting that the CDTA may be thought of as a current differencing block (CDB) followed by an operational transconductance amplifier (OTA) [17].

Current-mode comparators are realized using CDTAs with a very high (ideally infinite) resistance connected between the Z-port and ground. This can be understood by considering that the CDTA may also be thought of as a current-mode opamp if the Z-terminal is not taken outside [158]. The unweighted current output at the X-terminal of current comparator can be modelled by

\[ I_x = I_m \tanh \beta (I_P - I_N) \]  

(6.2)
where $\beta$ is the open-loop gain of the comparator (practically very high) and $\pm I_m$ are the output current levels of the comparator. For the sake of simplicity, it will be assumed that the CDB is an ideal current differencing block and all the non-idealities of the CDTA are associated with the OTA. $R_p$ and $C_p$ are the input resistance and capacitance of the OTA. These parasitic components are included to model the dynamic nature of the OTA, and therefore the CDTA.

### 6.3 Current-mode Linear Equation Solver

Let the simultaneous linear equations to be solved are

\[
AI = B \quad (6.3)
\]

where

\[
A = \begin{bmatrix}
  a_{11} & a_{12} & \ldots & a_{1n} \\
  a_{21} & a_{22} & \ldots & a_{2n} \\
  \vdots & \vdots & \ddots & \vdots \\
  a_{n1} & a_{n2} & \ldots & a_{nn}
\end{bmatrix} \quad (6.4)
\]

\[
B = \begin{bmatrix}
  b_1 \\
  b_2 \\
  \vdots \\
  b_n
\end{bmatrix} \quad (6.5)
\]

\[
I = \begin{bmatrix}
  I_1 \\
  I_2 \\
  \vdots \\
  I_n
\end{bmatrix} \quad (6.6)
\]

where $I_1, I_2, \ldots, I_n$ are the variables and $a_{ij}$ and $b_i$ are constants. As earlier, it will be assumed that the coefficient matrix $A$ is invertible, and hence, the system of linear equations (6.3) is consistent and not under-determined. In other words, the linear system (6.3) has a uniquely determined solution.

The proposed novel current-mode neural-network based circuit to solve the system of equations of (6.3) is presented in Figure 6.3. As can be seen from Figure 6.3, individual equations from the set of equations to be solved are
6.3 Current-mode Linear Equation Solver

Figure 6.3: Proposed current-mode, non-linear feedback neural circuit to solve simultaneous linear equations in $n$-variables

passed through non-linear synapses comprising of current-mode, multi-output comparators designated as $C_1$ through $C_n$. $X_{ij}$ denotes the $j$-th output of $i$-th comparator and $s_{ij}I_{x_i}$ represent the output current of the $i$-th comparator scaled by a factor of $s_{ij}$. Equation 6.2 shows that the synaptic connections in this case are highly non-linear as opposed to the linear synaptic interconnections (implemented using resistances) used in standard Hopfield network and its variants. The outputs of the comparators are fed to neurons as weighted inputs. Weights are assigned to the output currents obtained from the comparators in accordance with the entries in the coefficient matrix $A$. The neurons are realized by using CDTAs wherein the currents arriving at the input of a neuron from various synapses are added. The current-mode amplifiers emulating neurons are designated as $N_1$ through $N_n$.

In due course, it shall be shown that the synaptic weights, or equivalently, the output current scaling factors should be equal to the entries in the co-
6.3 Current-mode Linear Equation Solver

Figure 6.4: Equivalent circuit of the first neuron of the proposed current-mode, non-linear feedback neural circuit to solve simultaneous linear equations in $n$-variables.

Efficient matrix of (6.4). A direct consequence of the use of current-mode comparators is that the use of resistances in the synaptic interconnections is avoided thereby yielding a ‘transistor-only’ implementation. This is due to the fact that the current outputs of the comparators may directly be added at the inputs of the amplifiers emulating neurons. This reduces the complexity and causes the circuit to compare favourably with existing circuits from the viewpoint of monolithic integration.

In order to analyze the operation of the proposed circuit of Figure 6.3, it is imperative that the CDTAs forming the neurons be replaced by their equivalent model given in Figure 6.2. Figure 6.4 shows the first neuron of the proposed circuit with the CDTA replaced by its equivalent model. In the circuit of Figure 6.4, the currents arriving at node ‘A’ add up to yield a...
6.3 Current-mode Linear Equation Solver

combined current $I_A$ which may be written as

$$ I_A = s_{11}I_m \tanh \beta (a_{11}I_1 + a_{12}I_2 + \ldots + a_{1n}I_n - b_1) $$

$$ + s_{21}I_m \tanh \beta (a_{21}I_1 + a_{22}I_2 + \ldots + a_{2n}I_n - b_2) + \ldots $$

$$ + s_{n1}I_m \tanh \beta (a_{n1}I_1 + a_{n2}I_2 + \ldots + a_{nn}I_n - b_n) \quad (6.7) $$

Also,

$$ I_{z1} = -I_A \quad (6.8) $$

Further, application of KCL at node ‘B’ results in

$$ C_{p1} \frac{du_1}{dt} + \frac{u_1}{R_1} = I_{z1} \quad (6.9) $$

where

$$ R_1 = R_{p1} \parallel R_Z \quad (6.10) $$

Therefore,

$$ C_{p1} \frac{du_1}{dt} = -s_{11}I_m \tanh \beta (a_{11}I_1 + a_{12}I_2 + \ldots + a_{1n}I_n - b_1) $$

$$ - s_{21}I_m \tanh \beta (a_{21}I_1 + a_{22}I_2 + \ldots + a_{2n}I_n - b_2) + \ldots $$

$$ - s_{n1}I_m \tanh \beta (a_{n1}I_1 + a_{n2}I_2 + \ldots + a_{nn}I_n - b_n) - \frac{u_1}{R_1} \quad (6.11) $$

Moreover, as has been shown in the next section, the network in Figure 6.3 can be associated with an Energy Function $E$ given by

$$ E = \frac{I_m}{\beta} \sum_{i=1}^{n} \ln \cosh \beta \left[ \sum_{j=1}^{n} a_{ij}I_j - b_i \right] - \sum_{i=1}^{n} \frac{1}{R_i} \int_{0}^{I_i} u_idI_i \quad (6.12) $$

From (6.12), it follows that

$$ \frac{\partial E}{\partial I_1} = a_{11}I_m \tanh \beta (a_{11}I_1 + a_{12}I_2 + \ldots + a_{1n}I_n - b_1) $$

$$ + a_{21}I_m \tanh \beta (a_{21}I_1 + a_{22}I_2 + \ldots + a_{2n}I_n - b_2) + \ldots $$

$$ + a_{n1}I_m \tanh \beta (a_{n1}I_1 + a_{n2}I_2 + \ldots + a_{nn}I_n - b_n) - \frac{u_1}{R_1} \quad (6.13) $$
Also, if \( E \) is the energy function, it must satisfy the following condition [155]:

\[
\frac{\partial E}{\partial I_i} = -C_{pi} \frac{du_i}{dt} \quad (6.14)
\]

Comparing (6.11) and (6.13) according to (6.14) yields

\[
s_{11} = a_{11}; \ s_{21} = a_{21}; \ldots \ s_{n1} = a_{n1} \quad (6.15)
\]

In a similar fashion, scaling factors for the remaining \( X \)-terminals of the various CDTAs may be obtained and are given below. It can be seen that the scaling factors are found to be identical to the coefficients of the linear equations being solved.

\[
\begin{bmatrix}
  s_{11} & s_{12} & \ldots & s_{1n} \\
  s_{21} & s_{22} & \ldots & s_{2n} \\
  \vdots & \vdots & \ddots & \vdots \\
  s_{n1} & s_{n2} & \ldots & s_{nn}
\end{bmatrix}
= \begin{bmatrix}
  a_{11} & a_{12} & \ldots & a_{1n} \\
  a_{21} & a_{22} & \ldots & a_{2n} \\
  \vdots & \vdots & \ddots & \vdots \\
  a_{n1} & a_{n2} & \ldots & a_{nn}
\end{bmatrix}
\quad (6.16)
\]

It is to be noted that the current-mode linear equation solver of presented above facilitates resistor-less realizations and therefore has even lesser circuit complexity than its voltage-mode and mixed-mode counterparts. To solve an \( n \) variable system of linear equations, the current-mode linear equation solver requires only \( 2n \) DC-CDTAs.

### 6.3.1 Proof of the Energy Function

Differentiating the energy function of (6.12) w.r.t. \( I_i \), we get

\[
\frac{\partial E}{\partial I_i} = a_{1i}I_m \tanh \beta(a_{11}I_1+a_{12}I_2+\ldots+a_{1n}I_n-b_1)
+ a_{2i}I_m \tanh \beta(a_{21}I_1+a_{22}I_2+\ldots+a_{2n}I_n-b_2) + \ldots
+ a_{ni}I_m \tanh \beta(a_{n1}I_1+a_{n2}I_2+\ldots+a_{nn}I_n-b_n) - \frac{u_i}{R_{pi}} \quad (6.17)
\]

Further, the time derivative of the energy function is given by

\[
\frac{dE}{dt} = \sum_{i=1}^{N} \frac{\partial E}{\partial I_i} \frac{dI_i}{dt} = \sum_{i=1}^{N} \frac{\partial E}{\partial I_i} \frac{dI_i}{du_i} \frac{du_i}{dt} \quad (6.18)
\]
Using (6.17) in (6.18) we get

$$\frac{dE}{dt} = - \sum_{i=1}^{N} C_{pi} \left( \frac{du_i}{dt} \right)^2 \frac{dI_i}{du_i}$$  \hspace{1cm} (6.19)$$

The transfer characteristics of the output OTA used in Figure 6.4 implements the activation function of the neuron. With $u_i$ being the non-inverting terminal, the transfer characteristic is monotonically increasing and is shown in Figure 6.5 from which it can be seen that,

$$\frac{dI_i}{du_i} \geq 0$$  \hspace{1cm} (6.20)$$

thereby resulting in

$$\frac{dE}{dt} \leq 0$$  \hspace{1cm} (6.21)$$

with the equality being valid for

$$\frac{du_i}{dt} = 0; \hspace{0.5cm} \text{for all } i$$  \hspace{1cm} (6.22)$$

Equation (6.21) shows that the energy function can never increase with time which is one of the conditions for a valid energy function. The second criterion viz. the energy function must have a lower bound is also satisfied for the circuit of Figure 6.4 wherein it may be seen that $I_1, I_2, ..., I_n$ are all bounded (as they are the outputs of OTAs) amounting to $E$, as given in (6.12), having a finite lower bound.
6.3 Current-mode Linear Equation Solver

6.3.2 Stable states of the network

Convergence of the network to the global minimum of the Energy Function, which is exactly the solution of the set of linear equations, and the fact that there are no other minima, can be shown as follows. For \( n \) variables, the second term in the energy function expression (6.12) is significant only near the saturating values of the OTA and is usually neglected [155]. The energy function can therefore be expressed as

\[
E = \frac{I_m}{\beta} \sum_{i=1}^{n} \ln \cosh \beta \left( \sum_{j=1}^{n} a_{ij} I_j - b_i \right)
\]

(6.23)

from which it follows that

\[
\frac{\partial E}{\partial I_i} = a_{i1} I_m \tanh \beta (a_{i1} I_1 + a_{i2} I_2 + \ldots + a_{in} I_n - b_1) \\
+ a_{i2} I_m \tanh \beta (a_{i2} I_1 + a_{i2} I_2 + \ldots + a_{2n} I_n - b_2) + \ldots \\
+ a_{in} I_m \tanh \beta (a_{in} I_1 + a_{n2} I_2 + \ldots + a_{nn} I_n - b_n)
\]

(6.24)

For a stationary point, we have

\[
\frac{\partial E}{\partial I_i} = 0; \quad i = 1, 2, \ldots, n
\]

(6.25)

which yields,

\[
\begin{align*}
&a_{11} \tanh \beta (a_{11} I_1 + a_{12} I_2 + \ldots + a_{1n} I_n - b_1) + \\
&a_{21} \tanh \beta (a_{21} I_1 + a_{22} I_2 + \ldots + a_{2n} I_n - b_2) + \ldots + \\
&a_{n1} \tanh \beta (a_{n1} I_1 + a_{n2} I_2 + \ldots + a_{nn} I_n - b_n) = 0
\end{align*}
\]

(6.26)

\[
\begin{align*}
&a_{12} \tanh \beta (a_{11} I_1 + a_{12} I_2 + \ldots + a_{1n} I_n - b_1) + \\
&a_{22} \tanh \beta (a_{21} I_1 + a_{22} I_2 + \ldots + a_{2n} I_n - b_2) + \ldots + \\
&a_{n2} \tanh \beta (a_{n1} I_1 + a_{n2} I_2 + \ldots + a_{nn} I_n - b_n) = 0
\end{align*}
\]

(6.27)

\[
\begin{align*}
&\vdots \\
&a_{1n} \tanh \beta (a_{11} I_1 + a_{12} I_2 + \ldots + a_{1n} I_n - b_1) + 
\end{align*}
\]
6.3 Current-mode Linear Equation Solver

\[ a_{2n} \tanh(\beta(a_{21}I_1 + a_{22}I_2 + \ldots + a_{2n}I_n - b_2)) + \ldots + \]
\[ a_{nn} \tanh(\beta(a_{n1}I_1 + a_{n2}I_2 + \ldots + a_{nn}I_n - b_n)) = 0 \]  (6.28)

Denoting

\[ \tanh(\beta(a_{11}I_1 + a_{12}I_2 + \ldots + a_{1n}I_n - b_1)) = A_1 \]
\[ \tanh(\beta(a_{21}I_1 + a_{22}I_2 + \ldots + a_{2n}I_n - b_2)) = A_2 \]
\[ \vdots \]
\[ \tanh(\beta(a_{n1}I_1 + a_{n2}I_2 + \ldots + a_{nn}I_n - b_n)) = A_n \]  (6.29)

Therefore, for a stationary point we have,

\[
\begin{bmatrix}
  a_{11} & a_{12} & \ldots & a_{1n} \\
  a_{21} & a_{22} & \ldots & a_{2n} \\
  \vdots & \vdots & \ddots & \vdots \\
  a_{n1} & a_{n2} & \ldots & a_{nn}
\end{bmatrix}
\begin{bmatrix}
  A_1 \\
  A_2 \\
  \vdots \\
  A_n
\end{bmatrix}
= 
\begin{bmatrix}
  0 \\
  0 \\
  \vdots \\
  0
\end{bmatrix} \quad (6.30)
\]

This is a homogenous system of linear equations in variables \( A_1, A_2, \ldots, A_n \).

Since the coefficient matrix of the set of equations (6.30) is the same as that of (6.4) which is invertible, it follows that (6.30) will have a uniquely determined solution which is the trivial solution of the homogenous system. Therefore,

\[
\begin{bmatrix}
  A_1 \\
  A_2 \\
  \vdots \\
  A_n
\end{bmatrix}
= 
\begin{bmatrix}
  0 \\
  0 \\
  \vdots \\
  0
\end{bmatrix} \quad (6.31)
\]

which results in,

\[ a_{11}I_1 + a_{12}I_2 + \ldots + a_{1n}I_n - b_1 = 0 \]
\[ a_{21}I_1 + a_{22}I_2 + \ldots + a_{2n}I_n - b_2 = 0 \]
\[ \vdots \]
\[ a_{n1}I_1 + a_{n2}I_2 + \ldots + a_{nn}I_n - b_n = 0 \]  (6.32)

Thus, the energy function of the proposed neural network has a unique stationary point which coincides exactly with the solution of the given system of linear equations.
6.4 Hardware Simulation Results

The operation of the proposed current-mode circuit to solve linear equations was verified using computer simulations. The application of the proposed circuit to a chosen 2-variable problem (6.33) is discussed below.

\[
\begin{bmatrix}
1 & 2 \\
2 & 1
\end{bmatrix}
\begin{bmatrix}
I_1 \\
I_2
\end{bmatrix}
=
\begin{bmatrix}
10 \\
35
\end{bmatrix}
\quad (6.33)
\]

The circuit to solve (6.33) as obtained from Figure 6.3 is presented in Figure 6.6. As can be seen from Figure 6.6, only one synapse and one neuron is needed per equation. The current-mode synapses are realized using CDTA-based comparators and neurons are emulated by employing multi-output CDTAs.

Operation of the circuit of Figure 6.6 was verified using PSPICE program. CDTAs were realized using the bipolar junction transistor implementation shown in Figure 6.7 [146]. It needs to be mentioned that the output port ‘Z’ of the CDTAs is not explicitly shown in Figure 6.6. A fixed valued resistor \(R_Z = 10\,\text{K\Omega}\) was connected between the Z-output and ground for each of
6.4 Hardware Simulation Results

Figure 6.7: Bipolar implementation of CDTA [146]

Figure 6.8: Transfer characteristics of the CDTA based current-mode comparator

the CDTAs to set the value of the current gain at a high value. The resultant transfer characteristics of the CDTA are presented in Figure 6.8 from which it can be readily verified that the non-linear tanh(.) function is indeed obtained as mentioned in (6.2).
For the purpose of PSPICE simulations, the supply voltages were set to ±3 Volts and all the biasing currents of the CDTA were kept at 1000 µA. Further, to get the output currents according to \((6.33)\) the emitter areas of transistors in the output stage of the CDTAs were set to provide the required current scaling. The scaling factors are denoted on the CDTA symbol as ‘X’, and ‘2X’ where ‘2X’ denote a current output double that of the ‘X’ output. Routine mathematical analysis of \((6.33)\) gives the solution as \(I_1 = 20\) and \(I_2 = -5\). The results of PSPICE simulations yielded \(I_1 = 19.79\) µA and \(I_2 = -4.98\) µA which are in close agreement with the algebraic solution.

\[
\begin{bmatrix}
1 & 2 & 3 \\
3 & 2 & 1 \\
2 & 1 & 3 \\
\end{bmatrix}
\begin{bmatrix}
I_1 \\
I_2 \\
I_3 \\
\end{bmatrix}
= 
\begin{bmatrix}
11 \\
17 \\
13 \\
\end{bmatrix}
\]

(6.34)

Next, a set of three simultaneous linear equations in 3–variables was solved using the proposed approach. Equation (6.34) presents the chosen set of equations and Figure 6.10 shows the corresponding current-mode circuit. Mathematical analysis of (6.34) yields the solution as \(I_1 = 4\), \(I_2 = 2\) and \(I_3 = 1\). The results of PSPICE simulation, for the circuit of Figure 6.10, shown in Figure 6.11, are found to be \(I_1 = 3.94\) µA, \(I_2 = 1.96\) µA and \(I_3 = 0.96\) µA.
It can be seen that the obtained solutions are in close proximity to the exact algebraic solutions.

Further, linear equations in 5 and 10 variables were also solved using the proposed approach. Results of simulation runs for all the problems considered...
Table 6.1: PSPICE simulation results for the proposed circuit applied to different systems of linear equations

<table>
<thead>
<tr>
<th>[A]</th>
<th>[B]</th>
<th>Algebraic Solution</th>
<th>Simulated Results, µA (Using PSPICE)</th>
<th>Percentage Error in the solution (%)</th>
</tr>
</thead>
</table>
| \[
\begin{bmatrix}
1 & 2 \\
2 & 1 
\end{bmatrix}
\] | \[
\begin{bmatrix}
10 \\
35 
\end{bmatrix}
\] | 20 | 19.79 | -1.05 |
| \[
\begin{bmatrix}
1 & 2 & 3 \\
3 & 2 & 1 \\
2 & 1 & 3 
\end{bmatrix}
\] | \[
\begin{bmatrix}
11 \\
17 \\
13 
\end{bmatrix}
\] | 4 | 3.94 | -1.5 |
| \[
\begin{bmatrix}
2 & 1 & 3 & 3 & 1 \\
1 & 2 & 4 & 1 & 2 \\
3 & 2 & 1 & 1 & 1 \\
1 & 1 & 1 & 1 & 1 \\
1 & 1 & 2 & 1 & 2 
\end{bmatrix}
\] | \[
\begin{bmatrix}
38 \\
39 \\
14 \\
20 \\
43 
\end{bmatrix}
\] | -10 | 2.01 | -0.5 |
| \[
\begin{bmatrix}
1 & 2 & 1 & 3 & 4 & 2 & 1 & 1 & 1 & 12 \\
2 & 1 & 1 & 3 & 1 & 2 & 2 & 1 & 2 & 23 \\
1 & 1 & 4 & 3 & 3 & 1 & 1 & 4 & 4 & 1 \\
4 & 2 & 1 & 5 & 3 & 3 & 1 & 1 & 2 & 2 \\
1 & 1 & 5 & 1 & 2 & 1 & 2 & 2 & 5 & 2 \\
3 & 3 & 1 & 2 & 1 & 1 & 5 & 2 & 1 & 1 \\
5 & 5 & 1 & 4 & 1 & 1 & 3 & 4 & 2 & 2 \\
1 & 1 & 1 & 2 & 2 & 2 & 3 & 3 & 4 & 1 \\
4 & 2 & 2 & 1 & 3 & 2 & 5 & 4 & 3 & 2 \\
1 & 2 & 3 & 1 & 2 & 3 & 1 & 2 & 3 & 4 
\end{bmatrix}
\] | \[
\begin{bmatrix}
10 \\
10 \\
4 \\
8 \\
3 \\
-3 \\
-3 \\
7 \\
1 \\
-4 
\end{bmatrix}
\] | -2 | -2.04 | -0.15 |

are presented in Table 6.1. As can be seen from Table 6.1, the proposed network always converges to the solution of the given system of linear equations. The results of PSPICE simulation as obtained for the 10-variable problem in Table 6.1 are presented in Figure 6.12. From Table 6.1 it can be observed that the obtained results are quite near the algebraic solutions with the maximum error being approximately 4% and the average error being −0.31%.
In the previous section, the working of the proposed circuit has been verified by employing the bipolar implementation of CDTA [146]. Although the results of computer simulations are in accordance with the theory and the obtained solutions do not deviate from the exact solutions by any significant amount, the circuit uses bipolar transistors and therefore is not amenable for current monolithic integration processes which, in general, tend to favor CMOS technology. Therefore, it would seem prudent to test the performance of the proposed circuit using CMOS CDTAs. Toward that end, an existing CMOS implementation of the CDTA was selected and employed in the proposed neural network for solving linear equations and is reproduced in Figure 6.13 [18].

For the purpose of PSPICE simulations, biasing voltages for the CDTA of Figure 6.13 were taken to be ±1.8 V and the biasing current $I_B$ was kept to be 40 $\mu$A. 0.35 $\mu$m $n$-well CMOS process parameters from Taiwan Semiconductor Manufacturing Company (TSMC) were used to model the MOSFETs. The aspect ratios of transistors are presented in Table 6.2 below.

All the sets of linear equations of Table 6.1 were also solved with CMOS
CDTAs replacing their bipolar counterparts. The results of PSPICE simulation are presented in Table 6.3. It can be seen that the maximum percentage error in this case is 5% and the mean percentage error is 2.2%. This leads to the conclusion that the error depends upon the particular realization of CDTA used and is marginally more when CMOS CDTAs are employed.

To get a performance appraisal of the proposed circuit, the effect of device non-idealities on the accuracy of the solution was investigated. The gains of the CDTA-based comparators were varied by assigning different values to...
6.5 Discussion on VLSI implementation issues

Table 6.3: Simulation results for the proposed circuit employing CMOS CDTAs and used to solve systems of linear equations

<table>
<thead>
<tr>
<th>[A]</th>
<th>[B]</th>
<th>Algebraic Solution</th>
<th>Simulated Results, μA (Using PSpICE)</th>
<th>Percentage Error in the solution (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
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</tr>
<tr>
<td>[\begin{bmatrix} 1 &amp; 2 \ 2 &amp; 1 \end{bmatrix}]</td>
<td>[\begin{bmatrix} 10 \ -5 \end{bmatrix}]</td>
<td>[\begin{bmatrix} 20 \ -5.01 \end{bmatrix}]</td>
<td>[\begin{bmatrix} 0.25 \ 0.2 \end{bmatrix}]</td>
<td></td>
</tr>
<tr>
<td>[\begin{bmatrix} 1 &amp; 2 &amp; 3 \ 3 &amp; 2 &amp; 1 \ 2 &amp; 1 &amp; 3 \end{bmatrix}]</td>
<td>[\begin{bmatrix} 11 \ 17 \ 13 \end{bmatrix}]</td>
<td>[\begin{bmatrix} 4 \ 2 \ 1 \end{bmatrix}]</td>
<td>[\begin{bmatrix} 4.07 \ 1.96 \ 1.01 \end{bmatrix}]</td>
<td>[\begin{bmatrix} 1.75 \ -2.0 \ 1.0 \end{bmatrix}]</td>
</tr>
<tr>
<td>[\begin{bmatrix} 2 &amp; 1 &amp; 3 &amp; 3 &amp; 1 \ 1 &amp; 2 &amp; 4 &amp; 1 &amp; 2 \ 3 &amp; 2 &amp; 1 &amp; 1 &amp; 1 \ 1 &amp; 1 &amp; 1 &amp; 1 &amp; 1 \ 1 &amp; 1 &amp; 2 &amp; 1 &amp; 2 \end{bmatrix}]</td>
<td>[\begin{bmatrix} 38 \ 39 \ 14 \ 20 \ 43 \end{bmatrix}]</td>
<td>[\begin{bmatrix} 2 \ -10 \ 3 \ 5 \ 20 \end{bmatrix}]</td>
<td>[\begin{bmatrix} 1.98 \ -9.97 \ 3.02 \ 5.05 \ 19.87 \end{bmatrix}]</td>
<td>[\begin{bmatrix} -1.0 \ -3.0 \ 0.66 \ 1.0 \ -0.65 \end{bmatrix}]</td>
</tr>
<tr>
<td>[\begin{bmatrix} 1 &amp; 2 &amp; 1 &amp; 3 &amp; 4 &amp; 2 &amp; 1 &amp; 1 &amp; 1 &amp; 1 \ 2 &amp; 1 &amp; 1 &amp; 3 &amp; 1 &amp; 2 &amp; 2 &amp; 1 &amp; 2 &amp; 3 \ 1 &amp; 1 &amp; 4 &amp; 3 &amp; 3 &amp; 1 &amp; 1 &amp; 4 &amp; 4 &amp; 1 \ 4 &amp; 2 &amp; 1 &amp; 5 &amp; 3 &amp; 3 &amp; 1 &amp; 1 &amp; 2 &amp; 2 \ 1 &amp; 1 &amp; 5 &amp; 1 &amp; 2 &amp; 1 &amp; 2 &amp; 2 &amp; 5 &amp; 2 \ 3 &amp; 3 &amp; 1 &amp; 2 &amp; 1 &amp; 1 &amp; 5 &amp; 2 &amp; 1 &amp; 1 \ 5 &amp; 5 &amp; 1 &amp; 4 &amp; 1 &amp; 1 &amp; 3 &amp; 4 &amp; 2 &amp; 2 \ 1 &amp; 1 &amp; 1 &amp; 2 &amp; 2 &amp; 2 &amp; 3 &amp; 3 &amp; 4 &amp; 1 \ 4 &amp; 2 &amp; 2 &amp; 1 &amp; 3 &amp; 2 &amp; 5 &amp; 4 &amp; 3 &amp; 2 \ 1 &amp; 2 &amp; 3 &amp; 1 &amp; 2 &amp; 3 &amp; 1 &amp; 2 &amp; 3 &amp; 4 \end{bmatrix}]</td>
<td>[\begin{bmatrix} 10 \ -11 \ 10 \ -11 \ 10 \ 3 \ 3 \ 2 \ 2 \ 2 \ 7 \ 7 \ 7 \ 8 \ 8 \ 8 \ 3 \ 3 \ 4 \ 4 \ 4 \ 7 \ 7 \ 7 \end{bmatrix}]</td>
<td>[\begin{bmatrix} -2 \ 1 \ 3 \ 2 \ 2 \ -1 \ -1 \ -9 \ -7 \ -8 \ -8 \ -8 \ -8 \ -8 \ -3 \ -3 \ 4 \ 4 \ 4 \ 4 \ -3 \ -4 \ -4 \end{bmatrix}]</td>
<td>[\begin{bmatrix} -1.99 \ 0.98 \ 2.99 \ -0.99 \ 1.98 \ 6.94 \ -0.85 \ -3.02 \ 4.00 \ 4.00 \ 4.00 \ 4.00 \ 4.00 \ 4.00 \ 4.00 \ 4.00 \ 4.00 \ 4.00 \ 4.00 \ 4.00 \ 4.00 \end{bmatrix}]</td>
<td>[\begin{bmatrix} -0.5 \ -2.0 \ -0.33 \ -1.0 \ -1.0 \ -0.85 \ -0.66 \ 0 \ 1.0 \ 0.75 \end{bmatrix}]</td>
</tr>
</tbody>
</table>

the resistance connected between the Z-terminal of each CDTA and ground. Ideally, these resistances were assumed to have infinite value. The solutions, as obtained for the 3–variable problem, the circuit for which is shown on Figure 6.10, are presented in Table 6.4. Next, the effect of offset currents in the CDTA-based comparators was explored. Offset currents were applied at the \(N\) inputs of the CDTAs of Figure 6.10 and the results appear in Table 6.4. As
can be seen, the offset currents of the comparators do not affect the obtained solutions to any appreciable extent. However, the error does tend to increase with increasing offset currents. Finally, offset currents for the neuron amplifiers were applied at \( P \) inputs of the CDTAs of Figure 6.10 and the results of PSPICE simulations were compared with the algebraic solution as given in Table 6.4. As can be seen, the offset currents of the neuron amplifiers have little effect on the obtained solutions.

Another known limitation of the proposed circuit lies in the technique of altering the transistor size (Emitter area in case of BJTs and \( W/L \) ratio in case of MOSFETs) to introduce current scaling at the outputs of CDTA. This results in a circuit ‘tailor-made’ to solve a particular problem. In order to impart flexibility to the circuit, mechanisms to scale the output currents of CDTA externally need to be explored. One possible option is the use of Current-Controlled Current Differencing Transconductance Amplifier (CC-CDTA) in which the current at the output terminal (port-X) may be controlled by a control current [148]. Controlling the output current at port-X of the CDTA by means of a digital control word is another alternative. This is discussed next. The technique is to control the current transfer parameter from the Z-terminal to the X-terminal of the CDTA by replacing the transistors employed in the generation of current in the X-terminal with transistor arrays associated with switches [66]. The gain parameter \( k \) can take values from 1 to \( (2^n - 1) \), where \( n \) represents the number of transistor arrays. Actually, the transistor arrays implement a current summing network (CSN) at the X terminal. The circuit of the proposed Digitally Controlled CDTA (DC-CDTA) obtained after suitable modifications in the circuit of Figure 6.13 is presented in Figure 6.14. As can be seen from Figure 6.14, current scaling at the X-terminal of the DC-CDTA can be achieved by proper selection of the digital control word. For instance, a current three times the normal X-terminal current can be obtained by setting the control word \([d2 \ d1 \ d0]\) as \([0 \ 1 \ 1]\). The aspect ratios of the transistors used in the CMOS realization of the DC-CDTA are listed in Table 6.5.
### Table 6.4: Performance analysis of the proposed circuit

<table>
<thead>
<tr>
<th>Offset Current applied at N input of CDTAs (µA)</th>
<th>Simulated Results (Using PSpice)</th>
<th>Percentage Error in the Solution (%)</th>
<th>Resistance connected at Z terminal of CDTAs, ( R_z ) (kΩ)</th>
<th>Simulated Results (Using PSpice)</th>
<th>Percentage Error in the Solution (%)</th>
<th>Offset Current applied at P input of CDTAs (µA)</th>
<th>Simulated Results (Using PSpice)</th>
<th>Percentage Error in the Solution (%)</th>
</tr>
</thead>
<tbody>
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<td>3.92</td>
<td>2.00</td>
<td>1 K</td>
<td>3.90</td>
<td>2.50</td>
<td>+0.1</td>
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<td></td>
<td>1.94</td>
<td>3.00</td>
<td></td>
<td>1.94</td>
<td>3.00</td>
<td></td>
<td>1.96</td>
<td>2.00</td>
</tr>
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<td>1.00</td>
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<td>0.95</td>
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<td></td>
<td>0.99</td>
<td>1.00</td>
</tr>
<tr>
<td>+0.2</td>
<td>3.92</td>
<td>2.00</td>
<td>10 K</td>
<td>3.95</td>
<td>1.25</td>
<td>+0.2</td>
<td>3.93</td>
<td>1.75</td>
</tr>
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<td>+0.3</td>
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<td>+0.4</td>
<td>3.91</td>
<td>2.25</td>
</tr>
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<td>2.00</td>
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</tbody>
</table>

143
6.5 Discussion on VLSI implementation issues

Figure 6.14: CMOS realization of the proposed DC-CDTA

The DC-CDTA of Figure 6.14 was employed in the circuit of Figure 6.3 to solve various sets of simultaneous linear equations. Table 6.6 presents the results of proposed current-mode linear equation solver employing the DC-CDTA in place of the CDTA and used to solve different sets of linear equations in two variables. As can be seen, the same circuit can now be configured to solve different sets of linear equations by proper selection of the control words. In Table 6.6, \( B \) is kept constant for all the sets of equations and different coefficients are obtained by setting the corresponding control words. The results of PSPICE simulation as obtained for the first problem in Table 6.6 are presented in Figure 6.15.
6.5 Discussion on VLSI implementation issues

Table 6.5: Aspect ratios of the MOSFETs employed in the CMOS realization of DC-CDTA of Figure 6.14

<table>
<thead>
<tr>
<th>Transistor</th>
<th>W (μm) / L (μm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1 – M3</td>
<td>70/0.7</td>
</tr>
<tr>
<td>M26</td>
<td>58.8/0.7</td>
</tr>
<tr>
<td>M25, M27, MD27, M28, MD28</td>
<td>56/0.7</td>
</tr>
<tr>
<td>M15 – M17</td>
<td>35/0.7</td>
</tr>
<tr>
<td>M7, M10</td>
<td>42/0.7</td>
</tr>
<tr>
<td>M21</td>
<td>28.7/0.7</td>
</tr>
<tr>
<td>M4 – M6, M23</td>
<td>28/0.7</td>
</tr>
<tr>
<td>M22, M24</td>
<td>16.1/0.7</td>
</tr>
<tr>
<td>M8, M9, M11, M13, M14</td>
<td>10.5/0.7</td>
</tr>
<tr>
<td>M12</td>
<td>9.8/0.7</td>
</tr>
<tr>
<td>M8</td>
<td>7/0.7</td>
</tr>
</tbody>
</table>

Table 6.6: Simulation results for the proposed circuit employing CMOS DC-CDTAs and used to solve systems of linear equations in 2 variables. Also shown are the 3-bit digital control words.

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>Digital Control Word</th>
<th>Algebraic Solution</th>
<th>PSPICE Simulation Results</th>
<th>% Error</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>6   2</td>
<td>[20] 101 110 111</td>
<td>[8.69] −3.91</td>
<td>[8.63] −3.82</td>
<td>[0.69] 2.30</td>
</tr>
<tr>
<td>4</td>
<td>3   1</td>
<td>[20] 100 011 001 111</td>
<td>[6.80] −2.40</td>
<td>[6.81] −2.32</td>
<td>[−0.14] 3.33</td>
</tr>
<tr>
<td>1</td>
<td>6   4</td>
<td>[20] 001 110 100 111</td>
<td>[−11.76] 5.29</td>
<td>[−11.64] 5.30</td>
<td>[−1.02] 0.18</td>
</tr>
</tbody>
</table>

145
Table 6.7: Simulation results for the proposed circuit employing CMOS DC-CDTAs and used to solve systems of linear equations in 3 variables. Also shown are the 3-bit digital control words.

<table>
<thead>
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<th>[A]</th>
<th>[B]</th>
<th>Digital Control Word</th>
<th>Algebraic Solution</th>
<th>PSPICE Simulation Results</th>
<th>% Error</th>
</tr>
</thead>
<tbody>
<tr>
<td>7 2 3</td>
<td>5 6 4</td>
<td>15 -25</td>
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<td>0.18</td>
<td>10.00</td>
</tr>
<tr>
<td>15</td>
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<td>100 011 001 011</td>
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<td>16.99</td>
<td>2.13</td>
</tr>
<tr>
<td>2 5 7</td>
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</tr>
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</tr>
<tr>
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<tr>
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<td>34.52</td>
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<tr>
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<td>4 6 3</td>
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</table>

Next, Table 6.7 and Table 6.8 contain the results of PSPICE simulation of the digitally controlled linear equation solvers in three and five variables respectively. The 3–bit control words corresponding to the coefficients ($a_{ij}$) are also listed. As can be seen, in all the cases the obtained solutions are in close agreement with the algebraic solutions. The results of PSPICE simulation as obtained for the first problems in Table 6.7 and Table 6.8 are presented in Figure 6.16 and Figure 6.16 respectively.
### Table 6.8: Simulation results for the proposed circuit employing CMOS DC-CDTAs and used to solve systems of linear equations in five variables. Also shown are the 3-bit digital control words.

<table>
<thead>
<tr>
<th>( [A] )</th>
<th>( [B] )</th>
<th>Digital Control Word ( [d_2 \ d_1 \ d_0] )</th>
<th>Algebraic Solution</th>
<th>PSPICE Simulation Results</th>
<th>% Error</th>
</tr>
</thead>
<tbody>
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<td>1 3 2 7 1</td>
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6.6 Conclusion

A novel current-mode neural circuit employing non-linear feedback to solve simultaneous linear equations in $n$ variables, which uses $n$ neurons and $n$ synapses is presented. Each neuron requires one current-mode amplifier and each synapse is implemented using one current-mode comparator. Both the amplifier and the comparator were implemented first with CDTAs realized with bipolar transistors and then with CMOS CDTAs. No resistances were
needed to realize the weighted synaptic interconnections which facilitate monolithic integration. The energy function associated with the proposed network and the proof of its validity was also given. The proposed network was tested on various sample problem sets of 2 to 10 simultaneous linear equations and the simulation results confirm the validity of the approach. Configurability of the circuit to solve different sets of linear equations was demonstrated by introducing and using a new Digitally Controlled CDTA wherein a 3-bit digital control word was used to set the coefficient values. PSPICE simulation tests on sets of simultaneous linear equations in 2, 3 and 5 yielded promising results.