CHAPTER 3

ANALOG SIGNAL PROCESSING MODULES USING DVCC

This chapter discusses the design of fully differential (FD) VM first-order filters and second-order FD all-pass/notch filters. The circuits so designed are then employed to realize a FD four-phase oscillator. In addition, a Differential Voltage Current Conveyor (DVCC)-based bi-phase amplifier is also realized. Finally, the bi-phase amplifier is utilized to design a precision rectifier. The approach adapted within this chapter results in three new VM FD filter sections: two first-order all-pass sections and a second-order all-pass/notch based on the DVCC. One of the first-order FD all-pass realization uses one DVCC, two resistors and two grounded capacitors while the other utilizes a single DVCC, two grounded resistors and one grounded capacitor. The second-order all-pass realization is obtained using one DVCC, two resistors and two grounded capacitors. A four-phase FD sinusoidal oscillator is then realized by cascading the proposed first-order all-pass section with a FD non-inverting integrator. The second first-order FD filter is implemented in hardware with the DVCCs realized using CFOAs. Results of hardware tests and independent PSPICE simulations for the filter designed using actual CMOS based DVCC realizations are found to be in agreement with the theory proposed. Towards the end of this Chapter, two new biphase amplifiers are presented which are then utilized as precision rectifiers.

All simulations within this Chapter are performed using PSPICE and model parameters were obtained from the 0.5 μm CMOS parameters [59].

3.1 Introduction

Of the several techniques to extend the dynamic range of analog blocks, one standard approach is the use of FD signal processing modules. It results in the extension of the dynamic range by at least one order of magnitude through the cancellation of even harmonics, as well as the suppression of all undesirable common-mode signals [60-76]. Besides being useful in increasing the dynamic range of analog blocks, FD implementations are useful in analog signal processing, especially as electronics filters [59-78]. Such filters exhibit a larger dynamic range, better rejection to power-supply noise, reduced harmonic distortion and clock feed-through errors as compared to single-ended input/output where unintended noise and signals may be processed along with the intended signal. Such a FD signal processing approach is especially desirable in applications like switched-capacitor circuits and multi-standard wireless receivers [67]. A number of FD biquad filter circuits based on a variety of active elements have been reported in literature [61-66]. The design proposed in [61] has three fully differential current conveyors (FDCCIIIs), four floating resistors and two floating capacitors. The differential KHN
ANALOG SIGNAL PROCESSING MODULES USING DVCC

uses three dual-output differential difference current conveyor (DO-DDCCs) [62], two capacitors and five resistors. The circuit in [3] includes three FDCCIIs, six resistors and four capacitors. The circuits in [61] and [63] are capable of generating only low-pass and band-pass responses. The digitally-controlled balanced output transconductance amplifier (DCBOTA) based circuit proposed in [79] is composed of five active elements along with only two capacitors and one resistor while providing programmable high-pass, band-pass and low-pass responses. The circuit of [65] employs five differential OTAs and four capacitors to generate FD low-pass, band-pass and high-pass responses. The work in [66] presents a general circuit configuration for realizing differential-mode first-order all-pass and second-order all-pass/notch filters employing DVCC as the active element. Although circuit complexity is reduced as compared to other techniques, the use of two floating elements would be a limitation while considering the circuit for actual integration.

The simplest possible design approach for obtaining FD filters is to employ two single-ended filters. Although easy to design and implement, FD filters obtained using this approach are, in general, inefficient in terms of area and power. For instance, two active elements would be required for an FD filter using this approach. However, it is possible, by careful design and intuition, to obtain the same functionality by employing only a single active block, thereby offering significant savings in chip area.

This Chapter presents two FD first-order all-pass filters and a second-order APF/notch filter. DVCCs with only Z+ outputs are required for the second first-order all-pass filter and the second-order APF/notch filter realizations. While the first-order APF filter employs all grounded passive components (two resistors and one capacitor), the second-order APF/notch can be obtained using two resistors (one of which is grounded) and two grounded capacitors. The performance analysis of the proposed circuits is also analyzed taking into account the non-ideal effects normally associated with actual DVCC realizations. As an application, a quadrature oscillator employing the proposed first-order FD APF filters and a FD integrator in a closed loop is also designed. Functionality of the proposed circuits is simulated and verified. Further, hardware verification of the proposed second-type first-order filter and notch filter is also carried out. Since DVCC is not yet commercially available as an integrated circuit, AD-844 CFOAs were used to realize the DVCC.

Finally, two precision rectifiers are implemented by employing two DVCCs and passive components. A detailed discussion and literature survey of precision rectifiers is already given in Section 2.1 of Chapter 2.
3.2 Differential Voltage Current Conveyor

The differential voltage current conveyor (DVCC) shown in Fig. 3.1 was proposed in 1997 as a five terminal device characterized by the following port relations [74]:

\[
\begin{bmatrix}
V_x \\
I_{Y1} \\
I_{Y2} \\
I_{Z+} \\
I_{Z-}
\end{bmatrix} = \begin{bmatrix}
0 & 1 & -1 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 \\
k & 0 & 0 & 0 & 0 \\
-k & 0 & 0 & 0 & 0
\end{bmatrix}
\begin{bmatrix}
I_x \\
V_{Y1} \\
V_{Y2} \\
V_{Z+} \\
V_{Z-}
\end{bmatrix}
\]

(3.1)

Figure 3.1 Schematic symbol of the DVCC

While the voltage on the X-terminal follows the difference in voltages of terminals Y₁ and Y₂, a current injected at the X-terminal is multiplied by a factor \( k \) at the Z+ and Z− terminals. For the Z+ terminal, the direction of the conveyed current is the same as that of the current flowing in the X-terminal whereas for the Z− terminal, the current flows in the opposite direction. Ideally, \( k \) should be unity.

Although both Z+ and Z− types of current outputs are mentioned in equation (3.1), the DVCCs used in the proposed fully-differential circuit’s use only Z+ type outputs. Fig. 3.2 shows one possible CMOS implementation of the DVCC [59].

Figure 3.2 CMOS implementation of the DVCC with only Z+ output [59]
ANALOG SIGNAL PROCESSING MODULES USING DVCC

Since its introduction, the DVCC has been extensively employed in a number of analog signal processing functions such as in single-ended filters, oscillators, integrators, etc. [59, 77, 78]. However, not much research has been directed towards the realization of FD filters.

**Non Idealities Associated with DVCC**

The performance of the DVCC deviates from ideal behaviour since the voltage and current conveying actions are not exact, thereby leading to degradation in performance in the circuits based on such active elements. To account for non-ideal sources, two parameters $\alpha$ and $\beta$ are introduced where $\alpha_i$ accounts for current transfer gains and $\beta_i$ ($i = 1, 2$) accounts for voltage transfer gains of the DVCC. These transfer gains differ from unity by the voltage and current tracking errors of the DVCC. More specifically, $\alpha = 1 - \delta_i$ ($|\delta_i| << 1$) $\delta_i$ is the current tracking error from X to Z+ and $\delta_2$ is the current tracking error from X to Z−. Similarly, $\beta = 1 - \epsilon_i$ ($|\epsilon_i| << 1$), where voltage tracking errors are $\beta_1$ (from Y1 to X), $\beta_2$ (from Y2 to X). Incorporating the two sources of error, the modified DVCC port-relationship becomes:

$$V_X = \beta_1 V_1 - \beta_2 V_2$$
$$I_{Z+} = \alpha_1 I_X , \quad I_{Z-} = -\alpha_2 I_X$$

**Parasitics of DVCC**

Considering the parasitic impedances of the DVCC+, the non-ideal DVCC symbol with various parasitic elements is shown in Fig. 3.3. The matrix equation defining a non-ideal DVCC+ is modified to:

$$\begin{bmatrix}
V_{Y_1} \\
V_{Y_2} \\
I_{Y_1} \\
I_{Y_2} \\
I_{Z+} \\
\end{bmatrix} =
\begin{bmatrix}
1 + \frac{1}{R_{V1}} & 0 & 0 & 0 & 0 \\
0 & 1 + \frac{1}{R_{V1}} & 0 & 0 & 0 \\
0 & 0 & 1 + \frac{1}{R_X} & 0 & 0 \\
0 & 0 & 0 & 1 + \frac{1}{R_{Z+}} & 0 \\
\end{bmatrix}
\begin{bmatrix}
I_{Y_1} \\
I_{Y_2} \\
I_{Y_1} \\
\end{bmatrix}
= 
\begin{bmatrix}
V_{Y_1} \\
V_{Y_2} \\
I_X \\
V_{Z+} \\
\end{bmatrix}$$

where $R_X$, $R_Y$, $R_Z$, $C_Y$ and $C_Z$ are the parasitic resistances and capacitances at the respective terminals. From Fig. 3.3 it is seen that the X-terminal exhibits low-value intrinsic resistance $R_X$; $Y_1$ and $Y_2$ terminals exhibit low-value parasitic capacitances $C_Y$ and $C_Z$ and high value parasitics resistances $R_{V1}$ and $R_{V2}$. The Z+ and Z− terminals exhibit high value parasitic resistances $R_Z$ in parallel with low value capacitances $C_Z$. 
3.3 Fully-Differential First-Order Filters

This section presents two fully differential (FD) first-order circuits based on DVCC.

**FD First-Order Filter-I**

A schematic diagram of the proposed FD all-pass filter is shown in Fig. 3.4. It employs one multi-output DVCC (MO-DVCC), two resistors and two grounded capacitors.

Analysis of the above filter results in the following transfer function:

\[ T_{ap} = \frac{V_{o1} - V_{o2}}{V_1 - V_2} = \frac{R_2}{R_1} \left[ s - \frac{1}{R_2 C_2} \right] / \left[ s + \frac{1}{R_1 C_1} \right] \] (3.5)

From equation (3.5) it is clear that the filter realizes FD first-order filter all-pass filter with a pole frequency of:

\[ \omega_o = \frac{1}{R_1 C_1} \] (3.6)

The phase angle of the FD filter is given as:
\[ \angle \phi = \pi - \arctan \omega R_1 C_1 - \arctan \omega R_2 C_2 \] (3.7)

Selecting \( R_1 = R_2 = R \) and \( C_1 = C_2 = C \) the FD all-pass transfer function given in equation (3.5) becomes:

\[ T_{AP} = \frac{V_{o1} - V_{o2}}{V_1 - V_2} = \left[ \frac{s - 1/RC}{s + 1/RC} \right] \] (3.8)

The pole frequency and phase angle are modified respectively as:

\[ \omega_p = \frac{1}{CR} \] (3.9)
\[ \angle \phi = \pi - 2\arctan \omega RC \] (3.10)

**Non Ideal Study**

Considering the non-idealities of the DVCC from equation (3.2) and (3.3) and re-analysis of the circuit shown in Fig. 3.4, the following non-ideal differential-mode and common-mode transfer functions are obtained:

\[ A_{DM} = 0.5 (\beta_1 + \beta_2) \frac{aR_2}{R_1} \left[ \frac{s - 1/R_2 C_2}{s + 1/R_1 C_1} \right] \] (3.11)
\[ A_{CM} = (\beta_1 - \beta_2) \frac{aR_2}{R_1} \left[ \frac{s - 1/R_2 C_2}{s + 1/R_1 C_1} \right] \] (3.12)

However, if equal \( \beta \) voltage gains are achieved in the DVCC, then the common-mode gain in equation (3.12) reduces to zero, which results in a very high CMRR. From equation (3.11) and (3.12), the non-ideal pole-frequency \( \omega_{o,n} \) can be expressed as:

\[ \omega_{o,n} = \frac{1}{R_1 C_1} \] (3.13)

Equation (3.13) reveals that the pole frequency remains unaltered even in the presence of device non-idealities for all the filter functions realized.

**Parasitics’ Study**

The effect of DVCC parasitics on the performance of FD first-order filter is considered next. Taking the parasitics discussed in equation (3.4), the modified expression of FD all-pass transfer function can be expressed as:

\[ T_{AP} = \frac{s^2 C_1 (C'_2 - C_2) R_2 R'_2 - s C_1 (R_2 - R'_2)}{s^3 C_1 C_2 C'_2 R_2 R'_1 R'_2 + s^2 (C_1 C_2 R'_2 R'_2 + R_2 R'_1 C_1 C'_2 + C_2 C'_2 R_2 R'_2) + s (C_1 R'_1 + C'_2 R_2 + C_2 R'_2) + 1} \] (3.14)

where \( C'_2 = C_2 + C_Z, R'_2 = \frac{R_2 R_Z}{R_1 + R_Z} \) and \( R'_1 = R_1 + R_X \) (3.15)

Equation (3.14) shows that the Z-terminal parasitic \( (R_Z/C_Z) \) along with resistor \( R_2 \) and capacitance \( C_2 \) brings extra poles and zeros to the transfer function which restricts the high frequency operation of the
The proposed first-order FD all-pass filter using a single DVCC and grounded passive components is shown in place of the usual Z+ terminal. This implies that the current output is twice than that of the normal Z+ output. Then the transfer function shown in equation (3.14) reduces to:

\[ T_{AP} = \frac{V_{o1} - V_{o2}}{V_1 - V_2} = \frac{R_2'}{R_1'} \left[ \frac{s - 1/R_2' C_2'}{s + 1/R_1' C_1} \right] \] (3.16)

The pole-frequency \( \omega_0' \) becomes:

\[ \omega_0' = \frac{1}{R_1' C_1} \] (3.17)

since \( R_1 \) merges with \( R_X \) to give \( R_1' \), it results in a slight deviation in the pole-frequency.

**FD First-Order Filter-II**

The proposed first-order FD all-pass filter using a single DVCC and grounded passive components is shown in Fig. 3.5. The DVCC used can be termed as a ‘modified’ DVCC since a 2Z+ output terminal is used in place of the usual Z+ terminal. This implies that the current output is twice than that of the normal Z+ output. Such a current scaling can be achieved by either properly scaling the aspect ratios of the Z+ stage MOSFETs (M8 and M12 in Fig. 3.2) or by having two Z+ stages in the DVCC realization and combining their outputs to yield the required current.

![Figure 3.5 Proposed first-order FD all-pass filter - II](image)

The differential output voltage of Fig. 3.5 can be represented as:

\[ V_{od} = V_{o1} - V_{o2} = (V_{i1} - V_{i2}) \left[ \frac{s - (2R_2 - R_1)/CR_2}{s + 1/CR_2} \right] \] (3.18)

From equation (3.18) the differential-mode and common-mode transfer function of the filters are:
ANALOG SIGNAL PROCESSING MODULES USING DVCC

\[ A_{DM} = \frac{V_{o1} - V_{o2}}{V_{i1} - V_{i2}} = \frac{s - (2R_2 - R_1)/CR_1R_2}{s + 1/CR_2} \]  \hspace{1cm} (3.19)

and

\[ A_{CM} = 0 \]  \hspace{1cm} (3.20)

Selecting \( R_1 = R_2 = R \) results in a first-order FD all-pass filter transfer function that is obtained from (3.19) as:

\[ A_{DM} = \frac{s - 1/CR}{s + 1/CR} \]  \hspace{1cm} (3.21)

Expression for the pole-frequency and phase angle of the FD filter of Fig. 3.5 is given as:

\[ \omega_0 = \frac{1}{CR} \hspace{0.5cm} \angle \phi = \pi - 2\tan^{-1}(\omega CR) \]  \hspace{1cm} (3.22)

**Non Ideal Study**

Considering the non-ideal voltages and current relationship of DVCC shown in equation (3.2) and (3.3), the modified differential-mode and common-mode transfer functions can be written as:

\[ A_{DM} = 0.5(\beta_1 + \beta_2) \frac{s - (2\alpha R_2 - R_1)/CR_1R_2}{s + 1/CR_2} \]  \hspace{1cm} (3.23)

\[ A_{CM} = (\beta_1 - \beta_2) \frac{s - (2\alpha R_2 - R_1)/CR_1R_2}{s + 1/CR_2} \]  \hspace{1cm} (3.24)

However, if equal \( \beta \) voltage gains are achieved in the DVCC then the common-mode gain in (3.24) reduces to zero, which in turn results in a very high CMRR. Equation (3.23) reveals that the pole-frequency remains unaltered even in the presence of device non-idealities for all the realized filter functions. The non-ideal pole frequency then becomes:

\[ \omega_{0,n} = 1/CR_2 \]  \hspace{1cm} (3.25)

**Parasitic Study:**

The proposed circuit of Fig. 3.5 is re-analyzed taking into account the parasitics associated with the DVCC as described in equation (3.4). The modified FD all-pass filter functions (assuming \( R_1 >> R_X \) and \( R_2 >> R_3 \)) then becomes:

\[ A_{DM} = \frac{s - (2R_2 - R')/C'R'R_2}{s + 1/C'R_2} \]  \hspace{1cm} (3.26)

where \( R' = R_1 + R_X \) and \( C' = C + 2C_2 \)

The pole-frequency of the proposed filter as a result of these parasitics is modified to:

\[ \omega'_0 = \frac{1}{C'R_2} \]  \hspace{1cm} (3.27)

It is to be noted that \( \omega'_0 \), in the presence of device parasitics, does not deviate much from the ideal value given in (3.22). This can be explained as follows. The parasitic capacitance appearing at the Z-
ANALOG SIGNAL PROCESSING MODULES USING DVCC

terminal (C₂) in parallel with the external parasitic capacitor (C) and the resultant deviation in pole-frequency caused by the marginal increase in the capacitance value (C′) is small (since C₁ ≪ C).

**Design and Verification**

The design of the proposed filter-I, shown in Fig. 3.4, is verified for a pole frequency of \( f₀ = 1.59 \text{MHz} \) with values \( C₁ = C₂ = C = 10\text{pF} \) and \( R₁ = R₂ = R = 10KΩ \). The supply voltages are taken as \( V_{DD} = -V_{SS} = 2.5\text{V} \) and \( V_{BB} = -1.5\text{V} \) [59]. The MOS transistor aspect ratio used for simulation is given in Table 3.1. The observed frequency response for phase and gain is shown in Fig. 3.6, which shows the simulated pole-frequency to be 1.56MHz. The time domain response of the proposed FD filter for a sinusoidal input signal with 600mV peak-to-peak amplitude is shown in Fig. 3.7, which depicts a phase shift of 90° between input and output with a THD of 0.95%.

The FD filter-II of Fig. 3.5 (which is the second proposed filter in this Chapter) is designed for a pole-frequency of \( f₀=1.59 \text{MHz} \) by selecting \( R₁ = R₂ = R = 1KΩ \). Value of the capacitor from equation (3.24) results in \( C = 100\text{pF} \). The aspect ratio of MOS transistors used in the DVCC implementation are again obtained from the parameters listed in Table 3.1. Supply voltages are kept as \( V_{DD} = -V_{SS} = 2.5\text{V} \) and \( V_{BB} = -1.5\text{V} \) [59].

The gain and phase responses of the first-order all-pass filter section are shown in Fig. 3.8. The simulated pole-frequency is found to be 1.57MHz at a phase angle of 90°, which corresponds to an error of 1.2%. The time domain response of the proposed all-pass filter, shown in Fig. 3.9, is obtained by applying a sine wave of differential voltage 600mV (peak to peak) at 1.57 MHz. It can be seen that the output signal is indeed phase shifted from the input signal by 90° as expected from theoretical investigations.

The variation in THD of the all-pass filter section is presented in Fig. 3.10. It is evident that the APF exhibits low values of harmonic distortion (below 3%) for 200mV to 1.0V of peak-to-peak value of differential input.

Although the results of PSPICE simulations for all the circuits proposed in this manuscript are sufficient and complete in themselves, an experimental verification is also performed for the circuits to further ascertain its operation. Towards that end, the circuit of Fig. 3.5 is set up on a breadboard using standard laboratory components. The DVCC was realized using a commercially available Current Feedback Operational Amplifier (CFOA) chip, the AD844 [80].

A previously presented realization [81] of the DVCC using CFOAs has been utilized during hardware verification. The phase plot which was obtained for the first-order all-pass filter circuit of Fig. 3.5 is presented in Fig. 3.11 from where it may be observed that the results obtained are in close
agreement with the theory. The input and output differential signal waveforms for the first-order APF were also displayed on a four-channel CRO. Figure 3.12 shows the waveforms as obtained during the course of hardware verification of the proposed second-order APF wherein the phase quadrature expected between the input and output signals is readily apparent.

Table 3.1 Aspect ratios of the transistors used in the CMOS implementation of the DVCC [59]

<table>
<thead>
<tr>
<th>Transistors</th>
<th>W (μm)</th>
<th>L (μm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1, M2, M3, M4</td>
<td>0.8</td>
<td>0.5</td>
</tr>
<tr>
<td>M5, M6</td>
<td>4</td>
<td>0.5</td>
</tr>
<tr>
<td>M9, M10</td>
<td>14.4</td>
<td>0.5</td>
</tr>
<tr>
<td>M7, M8, M13, M14, M15</td>
<td>10</td>
<td>0.5</td>
</tr>
<tr>
<td>M11, M12, M16, M17, M18</td>
<td>45</td>
<td>0.5</td>
</tr>
</tbody>
</table>

Figure 3.6 Frequency response of FD all pass filter-I of Fig. 3.4
Figure 3.7 Time domain response of FD filter-I of Fig. 3.4

Figure 3.8 Magnitude and phase response of the proposed first order filter-II of Fig. 3.5

Figure 3.9 Time-domain response of FD APF-II of Fig. 3.5
ANALOG SIGNAL PROCESSING MODULES USING DVCC

Figure 3.10 THD performance of the FD APF-II of Fig. 3.5

Figure 3.11 Results of hardware verification of first-order all-pass filter-II circuit of Fig. 3.5

Figure 3.12 Input and Output differential signals of the second order APF-II of Fig. 3.5
3.4 Fully Differential Second-Order All-Pass/Notch Filter

A proposed second-order FD all-pass/notch filter is shown in Fig. 3.13. It is evident that the realization is achieved after a slight modification of the filter shown in Fig. 3.5 wherein a grounded capacitor $C_1$ is added in series with resistor $R_1$.

Figure 3.13 Proposed second-order FD all-pass/notch filter section

Nodal analysis of the circuit shown in Fig. 3.13 yields the differential output voltage:

$$V_{od} = V_{o1} - V_{o2} = (V_{i1} - V_{i2}) \left[ \frac{s^2C_1C_2R_1R_2 - s(2C_1R_2 - C_1R_1 - C_2R_2) + 1}{s^2C_1C_2R_1R_2 + s(C_1R_1 + C_2R_2) + 1} \right]$$  \hspace{1cm} (3.28)

From equation (3.28) the differential gain and common mode gain can be expressed as:

$$A_{DM} = \frac{V_{o1} - V_{o2}}{V_{i1} - V_{i2}} = \frac{V_{od}}{V_{id}} = \frac{s^2C_1C_2R_1R_2 - s(2C_1R_2 - C_1R_1 - C_2R_2) + 1}{s^2C_1C_2R_1R_2 + s(C_1R_1 + C_2R_2) + 1}$$

$$A_{CM} = 0$$ \hspace{1cm} (3.30)

The pole frequency ($\omega_p$) and pole-Q are:

$$\omega_p = \frac{1}{\sqrt{C_1C_2R_1R_2}}$$ \hspace{1cm} (3.31)

$$Q = \frac{\sqrt{C_1C_2R_1R_2}}{C_1R_1 + C_2R_2}$$ \hspace{1cm} (3.32)

**Case 1: Realization of Second-Order All-Pass Filter**

To implement a second-order fully-differential all-pass filter from the circuit of Fig. 3.13, the following parameter selection is made as: $R_2 = 2R_1 = 2R$ and $C_1 = 2C_2 = 2C$. The differential-mode gain as given in equation (3.29) then becomes:

$$A_{DM} = \frac{4s^2C^2R^2 - 4sCR + 1}{4s^2C^2R^2 + 4sCR + 1}$$ \hspace{1cm} (3.33)

From the above equation, the pole frequency ($\omega_p$) and pole-Q are given by:
ANALOG SIGNAL PROCESSING MODULES USING DVCC

\[ \omega_n = \frac{1}{2CR} \]  \hspace{1cm} (3.34)

\[ Q = 0.5 \]  \hspace{1cm} (3.35)

**Case 2: Realization of Notch Function**

For realizing the notch filter the following condition must be satisfied: \( R_1 = R_2 = R \) and \( C_1 = C_2 = C \).

The differential-mode gain as given in (3.33) then becomes:

\[ A_{DM} = \frac{s^2C^2R^2 + 1}{s^2C^2R^2 + s2CR + 1} \]  \hspace{1cm} (3.36)

The expression for the pole frequency (\( \omega_0 \)) and pole-Q remain the same as above.

**Effects of Non-Idealities**

A detailed study of the circuit under device non-idealities is undertaken by employing the non-ideal port relations as in equation (3.2) and (3.3). The circuit of Fig. 3.13 is re-analyzed which leads to non-ideal differential- and common-mode transfer functions as:

\[ A_{DM} = 0.5(\beta_1 + \beta_2) \frac{s^2C_1C_2R_1R_2 - s(2\alpha C_1R_2 - C_1R_1 - C_2R_2) + 1}{s^2C_1C_2R_1R_2 + s(C_1R_1 + C_2R_2) + 1} \]  \hspace{1cm} (3.37)

\[ A_{CM} = (\beta_1 - \beta_2) \frac{s^2C_1C_2R_1R_2 - s(2\alpha C_1R_2 - C_1R_1 - C_2R_2) + 1}{s^2C_1C_2R_1R_2 + s(C_1R_1 + C_2R_2) + 1} \]  \hspace{1cm} (3.38)

Moreover, if equal voltage gains are achieved in the DVCC with careful design, the common-mode gain (\( A_{CM} \)) can again be nullified. The non-ideal gains in both the cases thus become:

**For all-pass filter:** \( C_1 = 2C_2 = 2C \) and \( R_2 = 2R_1/(2\alpha-1) = 2R/(2\alpha-1) \)

\[ A_{DM,a}\big|_{APF} = 0.5(\beta_1 + \beta_2) \frac{s^4C^2R^2 - s4\alpha CR + (2\alpha - 1)}{s^4C^2R^2 + s4\alpha CR + (2\alpha - 1)} \]  \hspace{1cm} (3.39)

**For notch filter:** \( C_1 = C_2 = C \) and \( R_2 = R_1/(2\alpha-1) = R/(2\alpha-1) \)

\[ A_{DM,a}\big|_{Notch} = 0.5(\beta_1 + \beta_2) \frac{s^2C^2R^2 + (2\alpha - 1)}{s^2C^2R^2 + s2\alpha CR + (2\alpha - 1)} \]  \hspace{1cm} (3.40)

**Parasitic Study**

The proposed circuits of Fig. 3.13 are re-analyzed taking into account the parasitic of DVCC as in equation (3.4). The modified FD second-order differential-mode transfer function (assuming \( R_1 >> R_X \) and \( R_d >> R_2 \)) then becomes:
ANALOG SIGNAL PROCESSING MODULES USING DVCC

\[ A_{DM} = k \frac{s^2C_1C'R_1R' - s(2C_1R_2 - C_1R' - C'R_2) + 1}{s^2C_1C'R_1R' + s(C_1R' + CR_2) + 1} \]  \tag{3.41}

where \( R = R_1 + R_X \), \( C = C_2 + 2C_Z \)

From equation (3.41) the non-ideal pole-frequency \( \omega'_0 \) and pole-Q are:

\[ \omega'_0 = \sqrt{ \frac{1}{C_1C'R_1R'} } \]  \tag{3.42}

\[ Q'_0 = \sqrt{ \frac{C_1C'R_1R'}{C_1R' + C'R_2} } \]  \tag{3.43}

Equations (3.42) and (3.43) show that the non-ideal pole frequency \( \omega'_0 \) and pole-Q deviate slightly from their ideal values (as shown in equations (3.31) and (3.32)). This can be attributed to the fact that the parasitic \( R_X \) appears in series with the external resistance \( R_1 \) and since \( R_1 \gg R_X \), \( R_X \) can be neglected. Similarly, since the parasitic capacitance of the Z-port appears in parallel with the external capacitance \( C_Z \) and since \( C_2 \gg C_Z \), the effect of \( C_Z \) on the overall capacitance connected to Z-port is negligible.

**Design and Verification**

The proposed second order all-pass filter shown in Fig. 3.13 is designed with passive element values of \( R_2 = 2R_1 = 2K\Omega \) and \( C_1 = 2C_2 = 100 \text{ pF} \). The pole-frequency is found to be 1.59 MHz. The phase is found to vary with frequency, from 0° to −360°, with a value of −180° at the pole frequency, and the simulated pole-frequency is found to be 1.57 MHz. The magnitude and phase plots are shown in Fig. 3.14 from where it can be verified that there is a deviation of ∼1.25% in the pole frequency between the expected and the obtained performances.

For obtaining a notch filter, the circuit shown in Fig. 3.13 is designed at a pole-frequency of 1.59 MHz by selecting \( R_1 = R_2 = R = 1K\Omega \) and \( C_1 = C_2 = C = 100 \text{ pF} \). The pole frequency obtained during simulation is 1.57 MHz which is very near to the design frequency. Graphical representation of the gain and phase variations for the notch is presented in Fig. 3.15.

Fig. 3.13 was also experimentally verified using standard laboratory components. Fig. 3.16 shows the results obtained for the second-order notch filter realization using the circuit of Fig. 3.13. It is readily apparent that the differential voltage gain obtained from the hardware realization of the notch closely matches the gain predicted by equation (3.36).
Figure 3.14 Magnitude and phase responses of the proposed second-order FD APF

Figure 3.15 Gain and phase plots of the proposed second-order FD notch filter

Figure 3.16 Results of hardware verification of notch implemented using the circuit of Fig. 3.12
3.5 Fully-Differential Four-Phase Oscillators

This section describes two four-phase FD oscillators. To realize a quadrature oscillator, a technique is used in which an all-pass section is cascaded with an integrator in a closed loop.

First Proposed FD Oscillator

The circuit of Fig. 3.4 is used for realizing a FD quadrature oscillator. The resulting circuit is shown in Fig. 3.17, where a MO-DVCC-2 along with a resistor and a capacitor forms a FD integrator.

![Circuit Diagram](image)

Figure 3.17 The MO-DVCC based VM-FPSO

Circuit analysis for the realized oscillator yields the characteristic equation as:

$$s^2 + s \left[ \frac{1}{R_1 C_1} - \frac{1}{R_3 C_3} \right] + \frac{1}{R_2 R_3 C_2 C_3} = 0$$  \hspace{1cm} (3.44)

From equation (3.44) the frequency of oscillation (FO) and the condition of oscillation (CO) are found as:

$$\text{FO: } \omega_0 = \sqrt{\frac{1}{R_2 R_3 C_2 C_3}}, \quad \text{CO: } R_1 C_1 \geq R_3 C_3$$  \hspace{1cm} (3.45)

At the oscillating frequency, the various outputs from Fig. 3.17 have the following relations:

$$V_{2,1} = V_{1,2} = \pi$$

$$V_{4,5} = V_{1,2} = -\frac{\pi}{2}$$

$$V_{5,4} = V_{1,2} = \frac{\pi}{2}$$  \hspace{1cm} (3.46)
**Second Proposed FD Oscillator**

As an application of the proposed first-order APF-II of Fig. 3.5, a FD four-phase sinusoidal oscillator is presented. The technique applied is the same as explained above wherein an APF is cascaded with an integrator in a feedback loop. Fig. 3.18 presents the DVCC-based FD four phase oscillator. It can be seen that the proposed circuit employs grounded capacitors and grounded resistors.

![Proposed four phase FD sinusoidal oscillator](image)

**Figure 3.18 Proposed four phase FD sinusoidal oscillator**

Assuming \( R_1 = R_2 = R, \ C_3 = 2C_2 \), the characteristic equation governing the circuit of Fig. 3.18 can be obtained as:

\[
(2C_1 R_2 C_3) s^2 + (C_2 R_3 - C_1 R)s + 1 = 0
\]  
(3.47)

Analysis of (3.47) yields the following frequency and condition of oscillation (**FO** and **CO** respectively) as:

**CO:** \[ C_1 R \geq 2C_2 R_3 \]  
(3.48)

**FO:** \[ \omega_o = \frac{1}{\sqrt{2C_1 R_2 C_3}} \]  
(3.49)

Selecting \( C_1 = C_2 = C \), equations (3.48) and (3.49) reduce to:

**CO:** \[ R \geq 2R_3 \]  
(3.50)

**FO:** \[ \omega_o = \frac{1}{C\sqrt{2RR_3}} \]  
(3.51)

From (3.50) and (3.51), orthogonal controllability of the frequency and condition of oscillation is evident as it can be readily verified that the value of \( C \) can independently control the frequency of oscillation without disturbing the condition of oscillation.
Design and Verification

The realized FD VM Four Phase Sinusoidal Quadrature Oscillator (FPSO) of Fig. 3.17 is designed for an oscillating frequency of $f_0 = 1.59$ MHz by selecting $R_1 = R_2 = R_3 = 10K\Omega$ in equation (3.51) which results in $C_1 = C_2 = C_3 = 10pF$. The observed waveshapes of the FPSO are shown in Fig. 3.19. The simulated FO is found to be 1.56 MHz, which is very close to the theoretical value with an error of 0.18%. To further support the circuit’s practical utility, $R_2$ was varied so as to vary the FO. The FO tuning through $R_2$ is shown in Fig. 3.20.

Lastly, the four-phase sinusoidal oscillator presented in Fig. 3.18 is designed for a theoretical FO of 1.59 MHZ by choosing $R_1 = R_2 = 2K\Omega$, $R_3 = 1K\Omega$ and $C_1 = C_2 = 50$ pF, $C_3 = 100$ pF. The obtained four-phase waveforms are presented in Fig. 3.21. The frequency measured for the waves, shown in Fig. 3.21 is found to be 1.52 MHz which translates into an error of 4.4%.

![Figure 3.19 The wave shapes of FPSO of Fig. 3.17](image1)

![Figure 3.20 Frequency response of FPSO with $R_2$](image2)
3.6 Comparison of Proposed and Existing Designs

An indicative comparison of the circuit complexity and functionality of the proposed first order all-pass filter-II of Fig. 3.5 and second order all-pass/notch of Fig. 3.13 filters and similar existing circuits is presented in Table 3.2.

Table 3.2 Comparison of the proposed work with existing circuits

<table>
<thead>
<tr>
<th>Reference</th>
<th>First-Order APF</th>
<th>Second-Order APF/Notch</th>
<th>Quadrature Oscillator</th>
<th>Filter pole/oscillator frequency (f)</th>
<th>Hardware Verification Done</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>No. and Type of Active Building Blocks</td>
<td>Passive Elements Used</td>
<td>No. and Type of Active Building Blocks</td>
<td>Passive Elements</td>
<td>Passive Elements</td>
</tr>
<tr>
<td>[66]</td>
<td>1 DVCC 1 grounded R 3 floating C</td>
<td>1 DVCC</td>
<td>1 grounded R 3 floating R 1 grounded C 2 floating C</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>[77]</td>
<td>2 DVCC 1 grounded C 1 floating R</td>
<td></td>
<td>-</td>
<td>3 DVCC 1 grounded R 2 grounded C</td>
<td>636.6 KHz No</td>
</tr>
<tr>
<td>[78]</td>
<td>-</td>
<td>1 FDCCII 1 floating R 1 grounded R 2 grounded C</td>
<td>-</td>
<td>-</td>
<td>15.01 KHz No</td>
</tr>
<tr>
<td>Proposed Circuit</td>
<td>1 DVCC 2 grounded R 1 grounded C</td>
<td>1 DVCC 1 floating R 2 grounded C 1 grounded R</td>
<td>2 DVCC 3 grounded C</td>
<td>1.59 MHz Yes</td>
<td></td>
</tr>
</tbody>
</table>

Table 3.2 shows that FD first-order all-pass filter-II and the second-order all-pass/notch filters are realized using a single active element. The number of passive components is also at a minimum. The capacitors used in all the circuits are grounded hence monolithic implementation in easier.
3.7 Precision Rectifiers

This section describes two precision rectifier circuits using a DVCC-based voltage mode bi-phase amplifier.

**Proposed Circuit-I**

The circuit shown in Fig. 3.22, uses voltage-controlled switches $S_1$, $S_2$. When the switch $S_1$ is closed and $S_2$ is open, the voltage at node P is zero and the output voltage ($V_o$) can be expressed as:

$$V_o = V_{in}$$  \hspace{1cm} (3.52)

With the switch $S_1$ open and $S_2$ closed, the voltage at node Q is zero, and the output voltage becomes:

$$V_o = -V_{in}$$  \hspace{1cm} (3.53)

Thus, from equations (3.52) and (3.53) it is clear that the circuit of Fig. 3.22 realizes a bi-phase amplifier with equal magnitudes.

To implement the precision rectifier from the bi-phase amplifier, the switching operation of the bi-phase amplifier is controlled using the DVCC based comparator as shown in Fig. 3.22. The comparator output currents flow through the very high gate impedance of the MOSFETs. $S_1$ and $S_2$ saturate the gate voltages $V_{C1}$ and $V_{C2}$ which are sufficient to control the switching operations of the two switches. During the positive cycle of the input, switch $S_1$ is ON and $S_2$ is OFF, resulting in $V_o = V_{in}$. However, during the negative cycle of the input, switch $S_1$ is OFF and $S_2$ is ON, thus the bi-phase amplifier behaves in an inverting mode resulting in $V_o = -V_{in}$ thus leading to full-wave rectification.

![Figure 3.22 Precision rectifier-I using a DVCC-based bi-phase amplifier](image-url)
Proposed Circuit-II

The circuit presented in this section is a modified form of the circuit shown in Fig. 3.22 and employs a DVCC-based biphase amplifier. Further, the switch of the biphase amplifier is also realized using a DVCC-based comparator and an NMOS transistor instead of two NMOS transistors (as employed in Fig. 3.22). The DVCC-based precision rectifier is shown in Fig. 3.23. Here, DVCC ② is used as a comparator [59]. During the positive half of the cycle, the comparator output is low and the switch is open thus leading to \( V_0 = V_{in} \). During the negative half of the cycle, the comparator output is high; the switch is closed, and thus the bi-phase amplifier behaves in an inverting mode resulting in \( V_0 = -V_{in} \). As a result, full-wave rectification is achieved. The advantage of this circuit over the previous circuit (shown in Fig. 3.22) is that it provides half-wave in addition to full-wave rectification. The minimum rectified voltage is 20mV and the two NMOS transistors are replaced by a single NMOS transistor which is suitable for IC fabrication in terms of area.

Design and Verification

To verify the proposed theory, the precision rectifier of Fig. 3.22 is designed with a sinusoidal input of 50mV peak at 10KHz, 100KHz, and 1MHz. The values of the resistances were kept as \( R_1 = R_2 = 5K\Omega \) and the switch is realized with an NMOS transistor with 10\( \mu m/0.5\mu m \). The large-sized transistor ensures small ‘ON’ resistance of the switch thereby causing \( V_P = 0 \) (when the switch is ON). The precision rectifier is simulated and the results are shown in Fig. 3.24-3.26.

The proposed circuit of Fig. 3.23 is designed with \( R_1 = 2K\Omega, R_2 = 4K\Omega \) and \( R_3 = 40K\Omega \). The supply voltages are kept as in Section 3.3 [59]. The NMOS transistor aspect ratio is 10\( \mu m/0.35\mu m \). The
ANALOG SIGNAL PROCESSING MODULES USING DVCC

full-wave rectified output at 20mV peaks and at 1 MHz are shown in Fig. 3.27. The aspect ratio of MOS transistors used in the DVCC are again obtained from the parameters listed in Table 3.1.

Figure 3.24 Input and output waveform of the precision rectifier-I at 10KHz

Figure 3.25 Input and output waveform of the precision rectifier-I at 100KHz

Figure 3.26 Input and output waveform of the precision rectifier-I at 1MHz

Figure 3.27 Input and output waveform precision rectifier-II at 1MHz
3.8 Conclusion

This Chapter presented three new voltage mode fully-differential filter realizations. Two first-order all-pass filters and a second-order all-pass/notch filter are realized by with the help of DVCCs and only Z+ outputs. The first order all-pass filter-I incorporates two resistors and two capacitors while the second first-order all-pass filter-II employs two resistors and one capacitor. All capacitors are grounded in both circuits. The second-order APF/notch can be obtained by using two resistors and two grounded capacitors.

It may be noted that two of the implemented filters i.e first order all-pass filter-II and second order all-pass/notch have the following features (Table 3.2): use of a single active element for each filter, FD topology, pole frequency of filter unaltered even in the presence of non-idealities, high input impedance, minimum passive components, suitability for fixed Q applications and high CMRR.

The performance analysis of the proposed circuits is also discussed taking into account the non-ideal effects normally associated with actual DVCC realizations. Further, a quadrature oscillator employing the proposed first-order FD APF filter-I and filter-II is presented. Hardware verification tests are carried out for the all-pass filter-II and the second order notch filter using AD844 CFOAs to emulate the DVCC functionality.

Lastly, two DVCC based biphase amplifiers are realized, which are, in turn, used to realize a full-wave precision rectifier without diodes. The features of this circuit are: minimum rectifiable amplitude is 20mV, diodes are not employed and operating frequency range is 10KHz to 1MHz.

The analog modules in proposed in this Chapter and the previous Chapter do not support tunability. This feature is included in the designs presented in Chapter 4 which makes use of a Dual-X Current Conveyer (DXCCII) along with triode MOSFETs.