CHAPTER 4

SIMULATION AND EXPERIMENT VALIDATION

Simulation and experiment validation of the proposed SSHSM schemes for a five-level CMI are presented in this chapter. MATLAB-Simulink model for single-phase and three-phase five-level inverters was constructed to compare the capabilities of the proposed modulation schemes that are described in the previous chapters. The simulations have been performed in MATLAB-Simulink with simpower system block sets. The simpower system Toolbox allows simulation of power electronic circuit devices and components in Simulink, requiring only interconnection of library components models for building the circuits for simulations. It also helps to confirm the PWM switching strategies which can be implemented in a DSP-CPLD based digital control platform. The parameters of the inverter model correspond to the prototype parameters, and as a load, a series RL circuit was used. The thorough analyses of voltage quality of the proposed modulations in the linear and over-modulation regions are performed and the selected simulation and experimental results are presented.

4.1 POWER LOSS ANALYSIS

The power losses associated with the inverter are of fundamental importance, which result in temperature increase in both switches and the load, which could damage the device. Hence, it is important to estimate the power losses. This section presents an evaluation of switching and conduction losses produced by the most representative modulation schemes used for

CMI. The losses in power converters are conduction loss, switching loss, snubber loss and off-state losses. The leakage current during the off-state is negligibly small; therefore the power losses during this state can be neglected. Snubber losses can be important in some kinds of power devices, such as gate turnoff thyristors. However, Snubbers are not usually required in converters made by other devices, such as IGBT's (Zambra et al 2008). Thus, only conduction and switching losses are considered in this thesis for power loss estimation. New high-power devices can switch faster. Since switching losses are directly related to the switching frequency, these losses are usually greatest in PWM power converters.

To perform these analyses, mathematical models for power devices are derived based on semiconductor characteristic curves which are provided in the datasheets. These models are used in simulation to compute the energy losses produced by different proposed modulations. The losses in a switching period depend on a number of factors: diode characteristics (reverse recovery time and peak current) and IGBT characteristics (rise and fall time, tail time and tail current). The following characteristic curves are used to develop the mathematical models of power devices:

- Output characteristics of IGBT ($V_{ce}(\theta) \times I_l(\theta)$),
- Diode characteristics ($V_F(\theta) \times I_l(\theta)$),
- Turn-on energy loss characteristics $(E_{on}(\theta) \times I_l(\theta))$,
- Turn-off energy loss characteristics $(E_{off}(\theta) \times I_l(\theta))$,
- Diodes reverse recovery characteristics $(E_{rec}(\theta) \times I_l(\theta))$.

where $V_{ce}(\theta)$ is on-state saturation voltage for the IGBT, $V_F(\theta)$ for the diode, $E_{on}(\theta)$ represent the turn-on energy losses during one

commutation, $E_{off}(\theta)$ represent the turn-off energy losses during one commutation, and $E_{rec}(\theta)$ represent energy loss during diode reverse recovery process.

Those characteristic curves are approximated by an exponential equation using cftool (curve fitting tool) of Matlab. The IGBTs selected (IRG4PC40KD) have maximum ratings that are a forward current of 25A and a direct voltage of 1200V. The mathematical models are found using points extracted from datasheets of each semiconductor device. The mathematical models for the power devices are given by;

$$V_{ce} = 0.96\, e^{0.0016\, I_l(\theta)} - 0.4654\, e^{-0.044\, I_l(\theta)} \tag{4.1}$$

$$V_F = 0.6\, e^{0.002\, I_l(\theta)} - 0.4258\, e^{-0.0275\, I_l(\theta)} \tag{4.2}$$

$$E_{rec} = 0.00806\, e^{-0.000322\, I_l(\theta)} - 0.0057\, e^{-0.00446\, I_l(\theta)} \tag{4.3}$$

$$E_{on} = 0.0041\, e^{0.0044\, I_l(\theta)} - 0.0037\, e^{-0.008\, I_l(\theta)} \tag{4.4}$$

$$E_{off} = 0.0443\, e^{0.00021\, I_l(\theta)} - 0.0547\, e^{-0.00107\, I_l(\theta)} \tag{4.5}$$

$$I_l(\theta) = M\, I_{max} \sin(\theta - \phi) \tag{4.6}$$

where $I_l(\theta)$ is the load current, I_{max} is the maximum load current and ϕ is the load displacement angle. ϕ is positive when the load is inductive and negative when the load is capacitive. The simulation parameters used for power loss analysis are as follows.

Supply voltage $V = 200$ v

Modulation signal frequency $(f_o) = 50$ Hz

Carrier signal frequency (f_c) = 5 kHz

Modulation index M = 0.2 to 1.0

4.1.1 Switching Loss

Switching losses are generated during the turn-on and turn-off switching processes of the power devices. These losses are generated because of switching delay that is intrinsic to the power devices. In such processes, the voltages and currents can take significant values simultaneously. Therefore, their instantaneous power can reach high values. Fortunately, these processes only last for short periods, although they are repeated several times within a second. For this reason, they are directly related to the switching frequency (Fazel et al 2007). At high switching frequencies, switching losses constitute a significant portion of the device power distribution. Therefore, accurate calculation of switching losses is an important step in the thermal management system design.

Switching losses are depends upon the number of switching actions per unit time, current and voltage involved in the commutation process, and load power factor. It is obtained by identifying every turn-on and turn-off instants during one reference period. Therefore, the turn-on, turn-off, and reverse recovery losses can be computed, respectively, from the following:

$$P_{on} = \frac{1}{T}\sum E_{on}(I_1(\theta)) \tag{4.7}$$

$$P_{off} = \frac{1}{T}\sum E_{off}(I_1(\theta)) \tag{4.8}$$

$$P_{rec} = \frac{1}{T}\sum E_{rec}(I_1(\theta)) \tag{4.9}$$

Then, the total switching losses are the sum of the turn-on, turn-off, and reverse recovery losses of all semiconductor devices. This algorithm is then realized for a wide range of modulation indexes and for all the modulation methods.

$$P_{swT} = P_{on} + P_{off} + P_{rec} \tag{4.10}$$

Figure 4.1 shows, for the full range of modulation index and the relative angle of the load currents, the ratio of switching loss with HAPOD versus the conventional APOD techniques. Note that the switching loss surface is always below one, which means that the switching losses are significantly smaller for the proposed method. The mean value of the surface is found to be approximately 0.6813, which means that the switching loss reduction is about 31.87 %. At unity power factor, the maximum switching loss reduction is achieved.

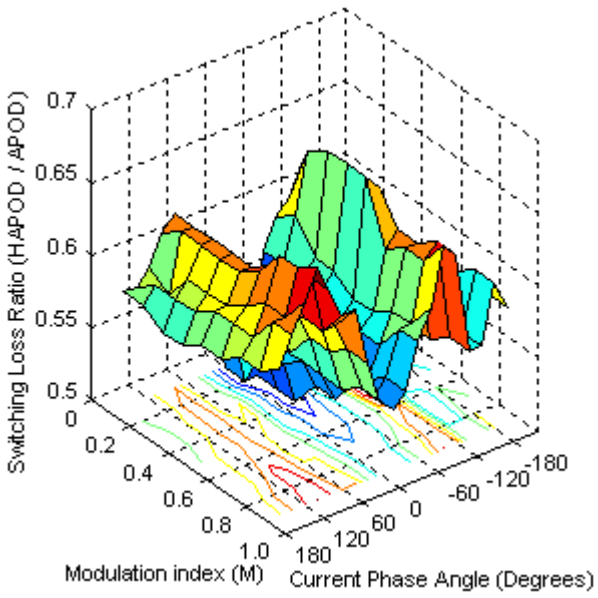


Figure 4.1 Switching loss ratio of sequential switching HAPOD and conventional APOD fed five-level inverter

4.1.2 Conduction Loss

Conduction losses are those that occur while the semiconductor device is conducting current, and there is a voltage between terminals, V_{ce} at the main switch and V_F for the diode. It is computed by multiplying the on-state voltage by on-state current (Kim et al 2001). The conduction losses are depends upon the number of devices in the output current path, modulation index and power factor. The number of devices depends upon which switch is active in each inverter cell. The calculation of conduction losses for each semiconductor of the inverter is given by

$$P_{condSW} = \frac{1}{2\pi}\int_0^{2\pi} V_{ce}(\theta)\, I_1(\theta)\, V_{cmd}(\theta)\ d\theta \tag{4.11}$$

$$P_{cond\,D} = \frac{1}{2\pi}\int_0^{2\pi} V_F(\theta)\ I_1(\theta)\, V_{cmd}(\theta)\ d\theta \tag{4.12}$$

where $V_{cmd}(\theta)$ is the PWM pulse.

Therefore, the total conduction losses are obtained by adding up the conduction losses of all semiconductors.

$$P_{condT} = P_{condSW} + P_{condD} \tag{4.13}$$

The calculation is made for each inverter cell and then losses in all the cells connected are summed over one fundamental period. The conduction loss in HAPOD techniques take higher values than conventional APOD and is shown in Figure 4.2. This is because of increased conduction period due to mixing of FFPWM. But, the percentage of increase in conduction loss is smaller. Moreover, in APOD, the maximum conduction losses are obtained by operation around the unity power factor, whereas in proposed modulation,

they are minimum. In this modulation, the conduction losses represent an average of about 36% of the total losses of the converter.

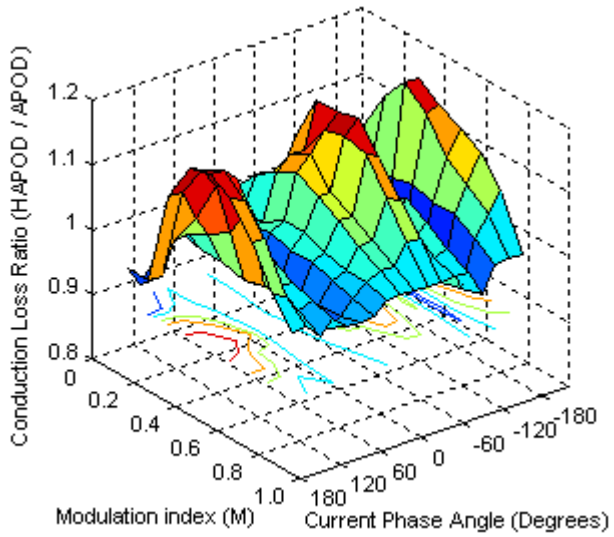


Figure 4.2 Conduction loss ratio of sequential switching HAPOD and conventional APOD fed five-level inverter

4.1.3 Power Loss

Power losses are the sum of switching and conduction losses. Based on the device models, these losses are computed for each semiconductor of the inverter. The sum of all results is computed to obtain the total power losses. Figure 4.3 shows the ratio of power losses between these two methods for the full range of linear modulation ($0 \leq M \leq 1$) and the relative angle of sinusoidal output currents ($-180^{\circ} \leq \phi \leq 180^{\circ}$). Since the switching losses are predominant, the power losses are less than those with conventional APOD operations. The mean value of the power loss ratio surface is found 0.718 approximately; which means loss reduction is about 28.2%. The best case is produced for a unity power factor and modulation index as one in which the power loss saving is about 31%. This SSHSM technique leads to a significant reduction in power loss over APOD in the entire range of fundamental power

factor and also at any given modulation index. The minimum reduction is 19% and the maximum is 31% approximately.

Even though, the power loss ratio between HAPOD and its own APOD operations are presented here, the other proposed modulations make similar power loss saving with respect its own modulation. In a practical high power converter, the switching losses are higher than the conduction losses. Therefore, reducing the switching losses becomes important for improving the efficiency of the converter. As a conclusion from the results, the main objective is achieved because the proposed modulation strategies are focused on minimizing power losses in this converter.

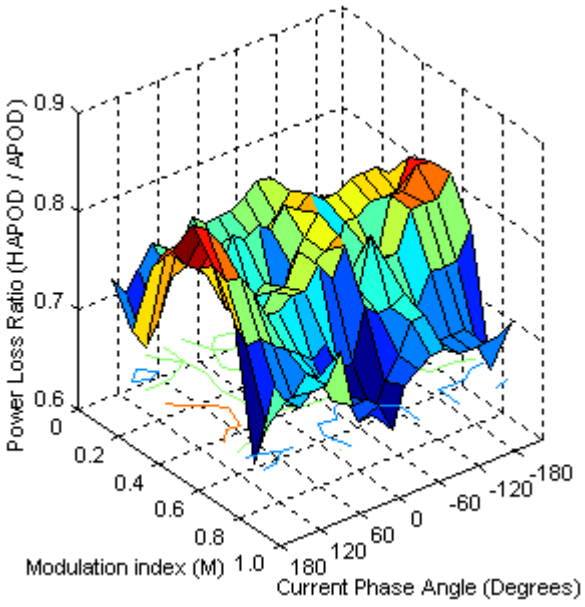


Figure 4.3 Power loss ratio of sequential switching HAPOD and conventional APOD fed five-level inverter

4.2 HARMONIC PERFORMANCE

To analyze the harmonic performance of the proposed modulation techniques, several harmonic measures are possible. The performance indexes used to analyze the quality of the output voltage waveforms are THD, and

Weighted Total Harmonic Distortion (WTHD), and normalized WTHD (WTHD0). These harmonic measures were performed by using MATLAB-Simulink software for a five-level inverter with these proposed modulations. The harmonic and spectrum analyses are made without inverter output filter in order to show the effectiveness of the proposed modulations. The load resistance and inductance are 10Ω and 15mH respectively, and the DC bus voltage is set at 200 V. The frequency of modulation and carrier waves are 50 Hz and 1500 Hz respectively and the inverter is operated in linear as well as over-modulation regions.

THD is one of the measures, which evaluates the quantity of harmonic contents in the output voltage waveform and is a popular performance index for power converters. THD reflects energy of the waveform harmonic content, and is defined as the ratio of the sum of the powers of all harmonic frequencies above the fundamental frequency to the power of the fundamental frequency (Mehrizi-Sani and Filizadeh 2009). As suggested in the IEEE standard 519, the first 50 harmonics are used for calculation of THD. The low pass filter and the nature of the highly inductive load will take care of the higher order of harmonics. The THD is calculated using Equation (4.14) and is plotted in Figure 4.4.

$$THD = \frac{\sqrt{\sum_{n=2}^{50} V_n^{\,2}}}{V_1} \tag{4.14}$$

where V_1 is the RMS value of the fundamental component voltage, n is the order of harmonics, and V_n is RMS value of the n^{th} harmonic.

In SSHSM schemes, the majority of the harmonics cancel and non-zero harmonics are attenuated and occur at higher frequencies. This result in a significantly lower THD compared to the conventional one, thus the

superiority. Furthermore, it is noticed that higher the value of modulation index (M), lower the value of THD, which implies that the output voltage is very near to the sinusoidal.

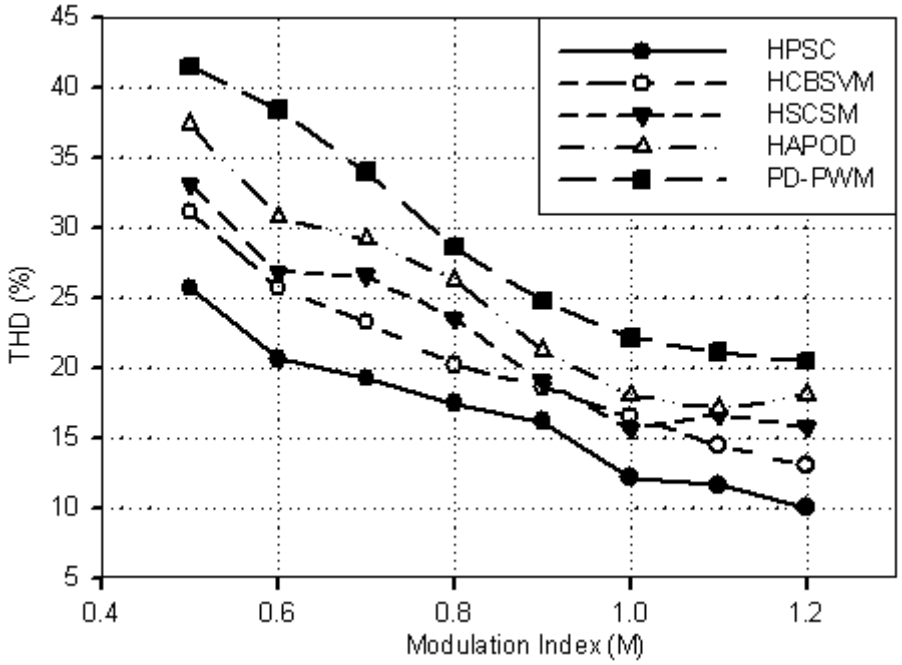


Figure 4.4 THD comparisons of proposed SSHSM schemes

THD measures only the amplitude of harmonics, and the harmonic order is ignored. To include the impact of harmonic frequency, another index is used, known as WTHD. WTHD is superior to THD as a figure of merit for a non-sinusoidal inverter waveform in which the lower portion of the frequency spectrum is weighted heavily, accurately portraying the expected harmonic current of an inductive load (Agelidis et al 2006). The WTHD uses spectral weighting factor and it is calculated using Equation (4.15) and plotted in Figure 4.5. As such, high modulation index that remains in the linear region generally corresponds to a lower WTHD. Consequently, the WTHD values are strongly dependent on the frequency ratio. Since increasing the carrier frequency causes the harmonics to move to higher orders, corresponds to a

lower WTHD. Also, WTHD values are lower when the power factor closer to unity.

$$\mathrm{WTHD} = \frac{\sqrt{\sum_{n=2}^{50} \left(\frac{V_n}{n}\right)^2}}{V_1} \tag{4.15}$$

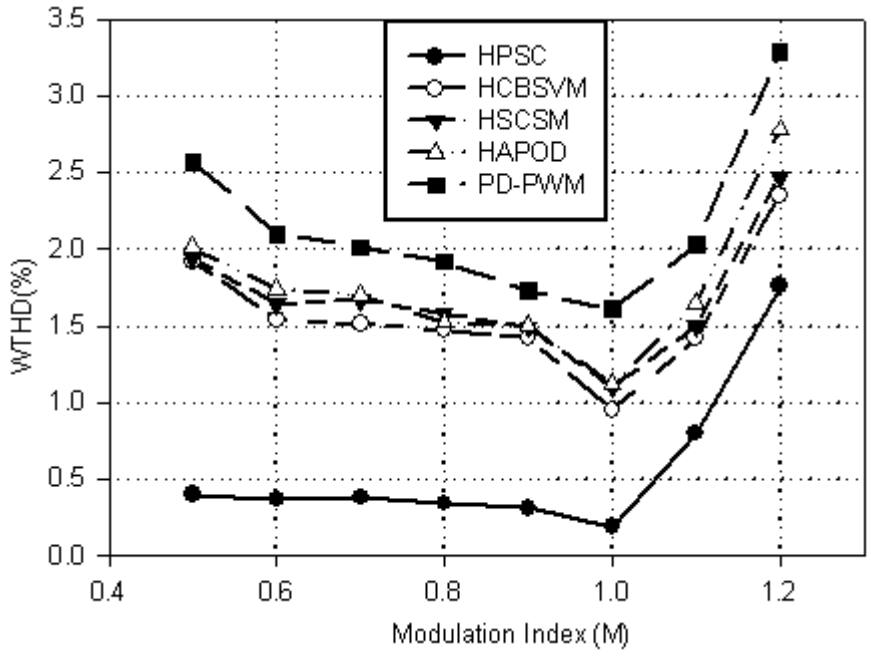


Figure 4.5 WTHD comparisons of proposed SSHSM schemes

The other performance index WTHD0 is suitable choice for PWM inverter, where the DC voltage remains constant and the fundamental component varies and it is calculated using Equation (4.16). Figure 4.6 shows the variation of the normalized WTHD against the modulation index, including over-modulation. WTHD0 is seen to decrease for increase in the modulation index up to maximum achievable and then it increases sharply due to over-modulation.

$$\mathrm{WTHD0} = \frac{\sqrt{\sum_{n=2}^{50} \left(\frac{V_n}{n}\right)^2}}{V_1 \Big| M = 1} \tag{4.16}$$

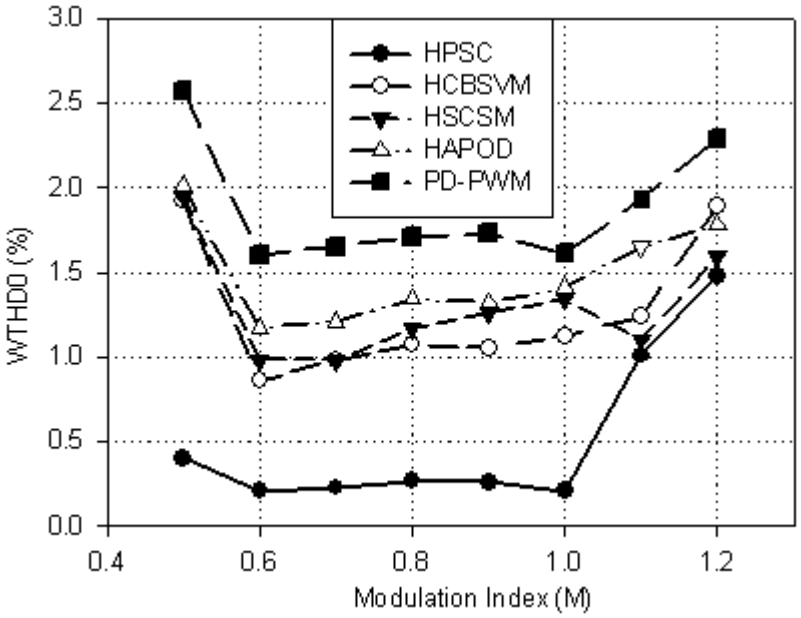


Figure 4.6 WTHD0 comparisons of SSHSM schemes

The ratio of RMS magnitude of the most significant harmonic to fundamental term (X) is found and plotted in Figure 4.7.

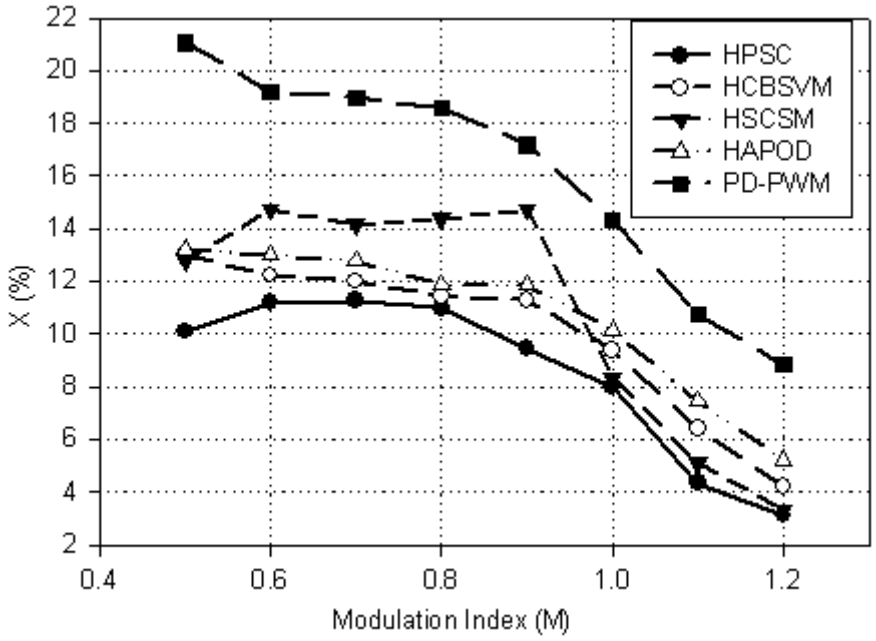


Figure 4.7 Ratio of RMS magnitude of the most significant harmonic to fundamental voltage comparsion of SSHSM schemes

The ratio X is almost same for all carrier frequency operation with frequency ratio over 20. In a linear modulation range (0.5<M<1), the RMS value of significant harmonic (20^{th}) to a fundamental component is with in 15 % and even less in over-modulation (M>1). But the lower order harmonics 3^{rd} and 5^{th} are present under 3% of a fundamental value in over-modulation operations. This inverter operates with odd frequency ratio, produces even side band harmonics and for even frequency ratio, getting odd side band harmonics. Furthermore, harmonics at the carrier and the multiples of carrier frequency do not exist at all.

From these harmonic analyses, it can be noted that:

- The THD of output voltage waveform with SSHSM techniques is considerably less than that with conventional PD-PWM technique as a reference.
- Low order harmonics upto carrier frequency are completely cancelled and results in smaller size of output filter required.
- In all these methods, the phase voltage THD is relatively high and increases dramatically, compared to the line voltage THD, as modulation index decreases.
- The WTHD and WTHD0 of the output voltage waveforms with SSHSM is less than PD-PWM for a wide range of modulation index.
- Throughout its linear modulation range, HPSC offers the least harmonic distortion among the proposed modulation schemes.
- The magnitude of the significant harmonics are reduced considerably, and the lower order harmonic amplitudes are highly suppressed.

- From the Figures 4.5 and 4.6, it can be seen that the proposed SSHSM methods give lower harmonic distortion when the modulation index is closer to unity.
- The HAPOD scheme has almost the same harmonic performance as that of the HSCSM.

4.3 SPECTRUM ANALYSIS OF INVERTER VOLTAGE AND CURRENT WAVEFORMS

The principle of Fourier decomposition is that any regular time varying waveform can be described by an infinite series of sinusoidal harmonic components. In practice, the non periodic nature of a PWM switch waveforms makes to find these components difficult. This problem was first solved by Bennet and Black for communication theory and then adapted for use with power converter systems by representing the switched waveform as a double variable controlled function that is periodic across both the carrier and the reference waveforms (Holmes and Lipo 2003). The harmonics of a non periodic nature of PWM switched waveform can be expressed in general form as a double summation Fourier series

$$\begin{aligned} v(t) = \frac{A_{oo}}{2} + \sum_{n=1}^{\infty} \{A_{on}\cos(n\omega_o t) + B_{on}\sin(n\omega_o t)\} + \\ \sum_{m=1}^{\infty} \{A_{mo}\cos(m\omega_c t) + B_{mo}\sin(m\omega_c t)\} + \\ \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} \{A_{mn}\cos(m\omega_c t + n\omega_o t) + B_{mn}\sin(m\omega_c t + n\omega_o t)\} \end{aligned} \quad (4.17)$$

where v(t) is inverter output voltage waveform.

The coefficients (A_{mn} and B_{mn}) in Equation (4.17) are obtained for any particular PWM strategy by evaluating the double Fourier integral of

$$A_{mn} + B_{mn} = \frac{1}{2\pi^2} \int_{-\pi}^{\pi} \int_{-\pi}^{\pi} V(x, y) e^{j(mx+ny)} \, dxdy; x = \omega_c t, y = \omega_o t \qquad (4.18)$$

The magnitude of each harmonic component is defined by the A_{mn} and B_{mn} coefficients. However, the coefficients presented in equation (4.17) can be separated in four distinct groups. The coefficient A_{00} (m=0 and n=0) represents the DC level of the output voltage. The first sum (m=0) represents the fundamental frequency (n=1) and the lower harmonic multiples of the fundamental frequency (n>1). The second sum (n=0) represents the higher harmonic multiples of the carrier (m≥1). The double sum (m≠0 and n≠0) represent all the possible combinations between the lower and higher harmonics. These harmonics exist around of each multiple of the carrier and are known as sideband harmonics. All the proposed modulations are analyzed with the double Fourier series for a five level inverter.

Simulations has been performed to investigate spectrum performance of the proposed modulations with five-level inverter in linear as well as over-modulation regions, M = 0.85 and M = 1.20, respectively. Selected simulation results of phase voltage and current waveforms with its harmonic spectrum are presented. The simulation parameters used as follows.

DC bus voltage	V = 200 v
Fundamental frequency	f_0 = 50 Hz
Carrier frequency	f_c = 1500 Hz
Load resistance	R = 20 Ω
Load inductance	L = 15 mH.

HAPOD modulation is based on unipolar APOD modulation uses level-shifted carriers with DC bias of $-v_c + 2A_c$ and reference signal. The reference signal is represented by a cosine with amplitude $2MA_c$ and fundamental frequency ω_o. Each carrier, combined with the reference signal, is responsible for the switching of two consecutive levels. The complete analytical expression of the phase (V_{an}) and line (V_{ab}) voltage for the HAPOD modulation are presented in the Equations (4.19)-(4.20), respectively. This modulation places the harmonic energy only in the sideband harmonics in the phase and line voltages.

$$V_{an}(t)\_HAPOD = 2\ M\ V\cos(\omega_o t) + \frac{2V}{\pi}\sum_{m=\pm\infty}^{\infty}\sum_{n=-\infty}^{\infty} J_{2n-1}(2m\ \pi\ M)\cos([m+n]\pi)\ \cos(m\omega_c t + [2n-1]\omega_o t) \quad (4.19)$$

$$V_{ab}(t)\_HAPOD = 2\sqrt{3}\ M\ V\cos(\omega_o t\ + \frac{\pi}{6}) + \frac{4V}{\pi}\sum_{m=\pm\infty}^{\infty}\sum_{n=-\infty}^{\infty} J_{2n-1}(2m\ \pi\ M)\cos([m+n]\pi)\ \sin([2n+1]\frac{\pi}{3}\ ) \quad (4.20)$$
$$\cos(m\omega_c t + [2n-1][\omega_o t - \frac{\pi}{3}])$$

The performance of the inverter output with HAPOD is shown in Figure 4.8. In the harmonic spectrum of the phase voltage in Figure 4.8 (b), the first group of harmonic components is shifted to cluster around the 30th harmonic. Because of half-wave symmetry, even harmonics are not present. THD and WTHD are calculated for the first 50 voltage harmonics and it is 23.45% and 1.52% respectively. Figure 4.8(c) shows phase currents. The lower order harmonics are absent in the current waveform and the higher order current harmonics are filtered by the nature of inductive load, so the current waveform is close to sinusoidal shape.

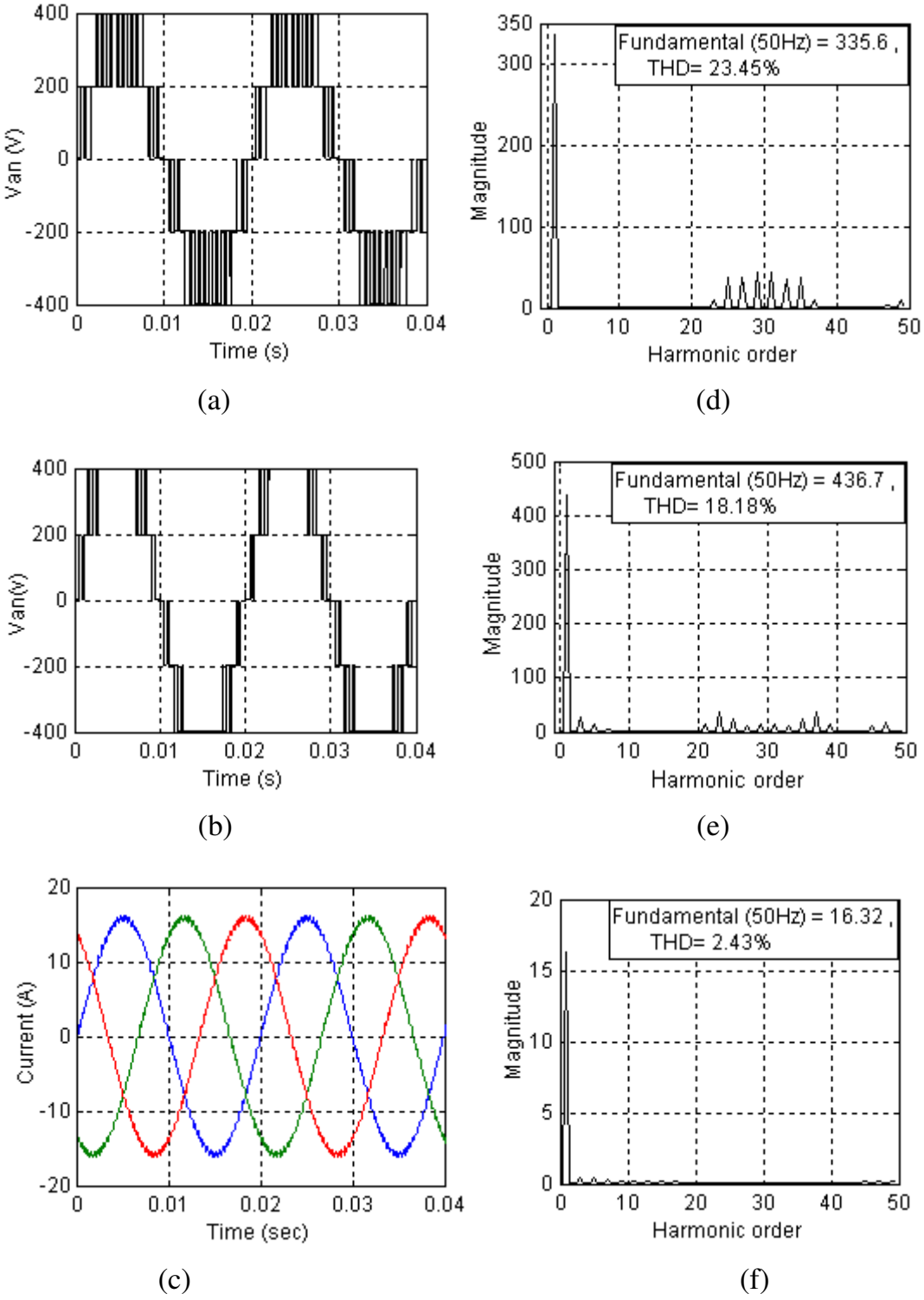


Figure 4.8 **Simulation results for HAPOD modulation: (a)-(c) Phase voltage in linear, over-modulation regions and current waveforms respectively. (d)-(f) Frequency spectrum of voltage and current waveforms of (a)-(c) respectively.**

Results in the case of over-modulation using the HAPOD are shown in Figure 4.8(b). Magnitudes of low order harmonics have been increased. Magnitude of the constructed phase voltage is 436.7 V. If the linear mode of operation could have extended to M = 1.20, a phase voltage also increased. Voltage WTHD has been increased to 2.32%.

Then the inverter is operated with HSCSM in linear modulation range and the corresponding voltage waveform with FFT analysis as shown in Figures 4.9 (a) and (d) respectively. It can be seen that all the lower order harmonics are absent and the fundamental is controlled at the pre defined value. It is interesting to note that the next significant harmonic will be 23^{rd}. The significant harmonics are 23, 29, 31, and 37, which are high frequency, with the RMS values under 12% of the fundamental term.

There are some lower order harmonics in over-modulation as shown in Figure 4.9(e). However, the amplitude of these harmonics is not significant (below 4% of fundamental term). In addition, the current waveform appears highly sinusoidal due to inherent low voltage distortion provided by HSCSM. This can be clearly appreciated with current harmonic spectrum shown in Figure 4.9(f). The output voltage is 336.6 V (RMS) and the load current is 16.38 A (RMS). The current THD is 2.01%.

HPSC modulation is derived from base PSC modulation pulses. All the switching points of the base PSC pulses are defined by comparing the phase shifted carriers with the reference signal. The magnitude of the A_{mn} and B_{mn} coefficients for the phase and line voltages can be calculated solving the double Fourier series for different values of m and n.

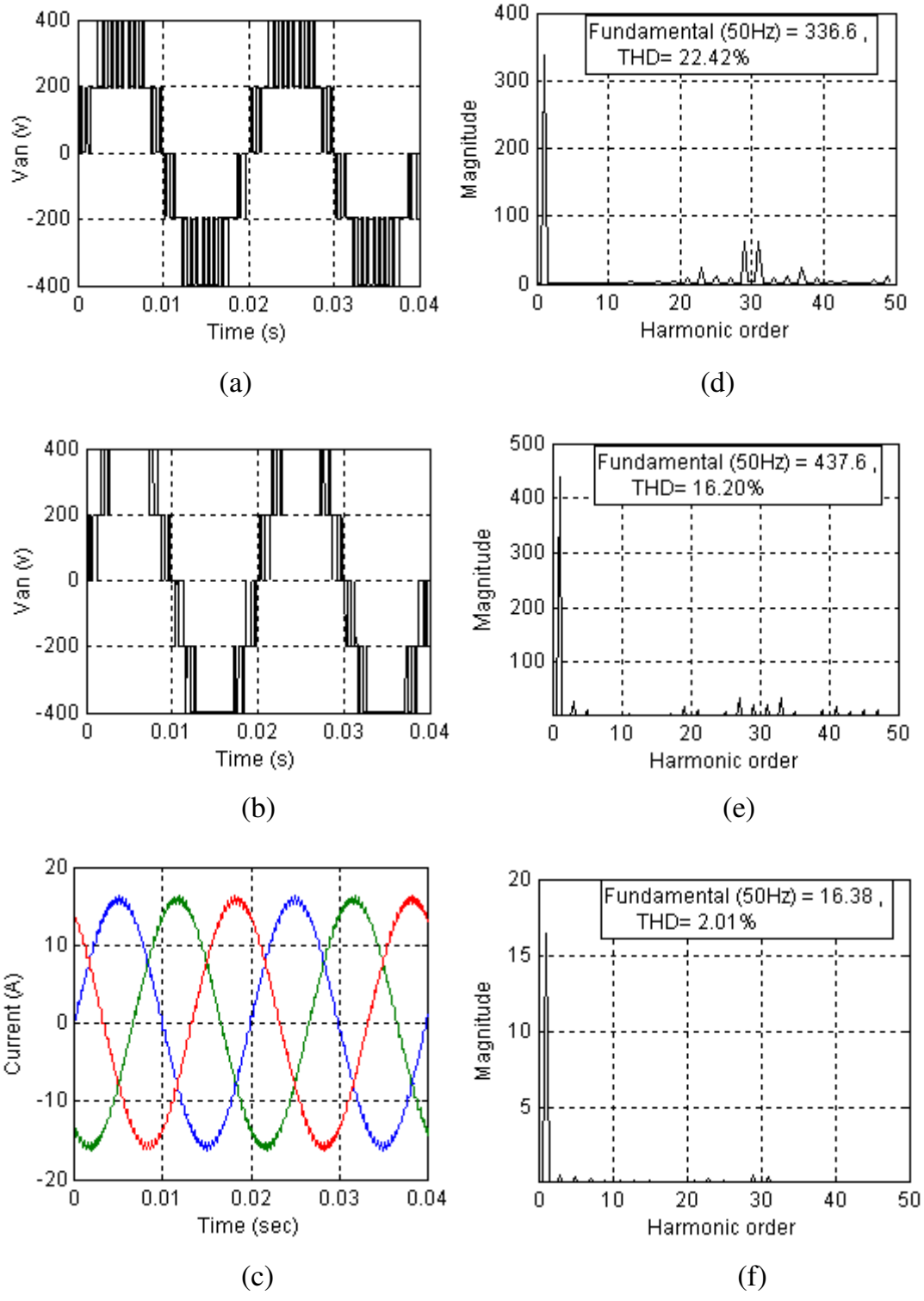


Figure 4.9 **Simulation results for HSCSM operation: (a)-(c) Phase voltages in linear, over-modulations, and current waveforms respectively. (d)-(f) Frequency spectrum of voltage and current waveforms of (a)-(c) respectively.**

The complete analytic expression of the phase voltage for the HPSC modulation is given by

$$v_{an}(t)\_HPSC = K\,M\,V\cos(\omega_o t) + \frac{2V}{\pi}\sum_{m=\pm n}^{\infty}\sum_{-\infty}^{\infty}\{\ \frac{1}{m}J_{2n-1}(K\,m\,\pi\,M)\cos\ ((K\,m+n+1)\pi) \quad (4.21)$$
$$\cos\ (2K\,m\omega_c t+(2n-1)\omega_o t)\ \}$$

where J_{2n-1} is Bessel function using Jacobi-Anger expansion

$$J_{2n-1}(\ K\,m\,\pi\,M\ ) = \frac{j^{(2n-1)}}{2\pi}\int_{-\pi}^{\pi} e^{-j(\ K\,m\,\pi\,M\ )}\cos(2n-1)\,\theta\ d\theta \quad (4.22)$$

The analytical solution for the line voltage for the HPSC modulation is given by

$$V_{ab}(t)\_HPSC = \sqrt{3}\ K\,V\,M\cos\ (\omega_0 t+\frac{\pi}{6})\ + \frac{8V}{\pi}\sum_{m=\pm n}^{\infty}\sum_{-\infty}^{\infty}\frac{1}{2m}\,J_{2n-1}\ (K\,m\,\pi\,M)\ \cos\ ([K\,m+n]\pi) \quad (4.23)$$
$$\sin\ ([2n\text{-}1]\frac{\pi}{3})\ \sin\ (2Km\omega_c t+[2n-1](\omega_0 t\text{-}\frac{\pi}{3}))$$

Complete harmonic cancellation of the switching harmonics up to $2K^{th}$ carrier group side band harmonics is again clearly evident with these analytical expressions, together with the expected cancellation of the triplen harmonics from the $2N^{th}$ carrier group sidebands. The HPSC operation is illustrated in Figure 4.10. In Figure 4.10 (d), it can be seen that the first set of sideband harmonics is centered about four times of the carrier frequency. However, the total numbers of switch transitions are exactly two times of HAPOD. If the over-modulation is desired for HPSC, lower order harmonics are introduced. It is essential that all FBI have exactly the same DC bus voltage to achieve effective harmonic side band cancellation for a CMI.

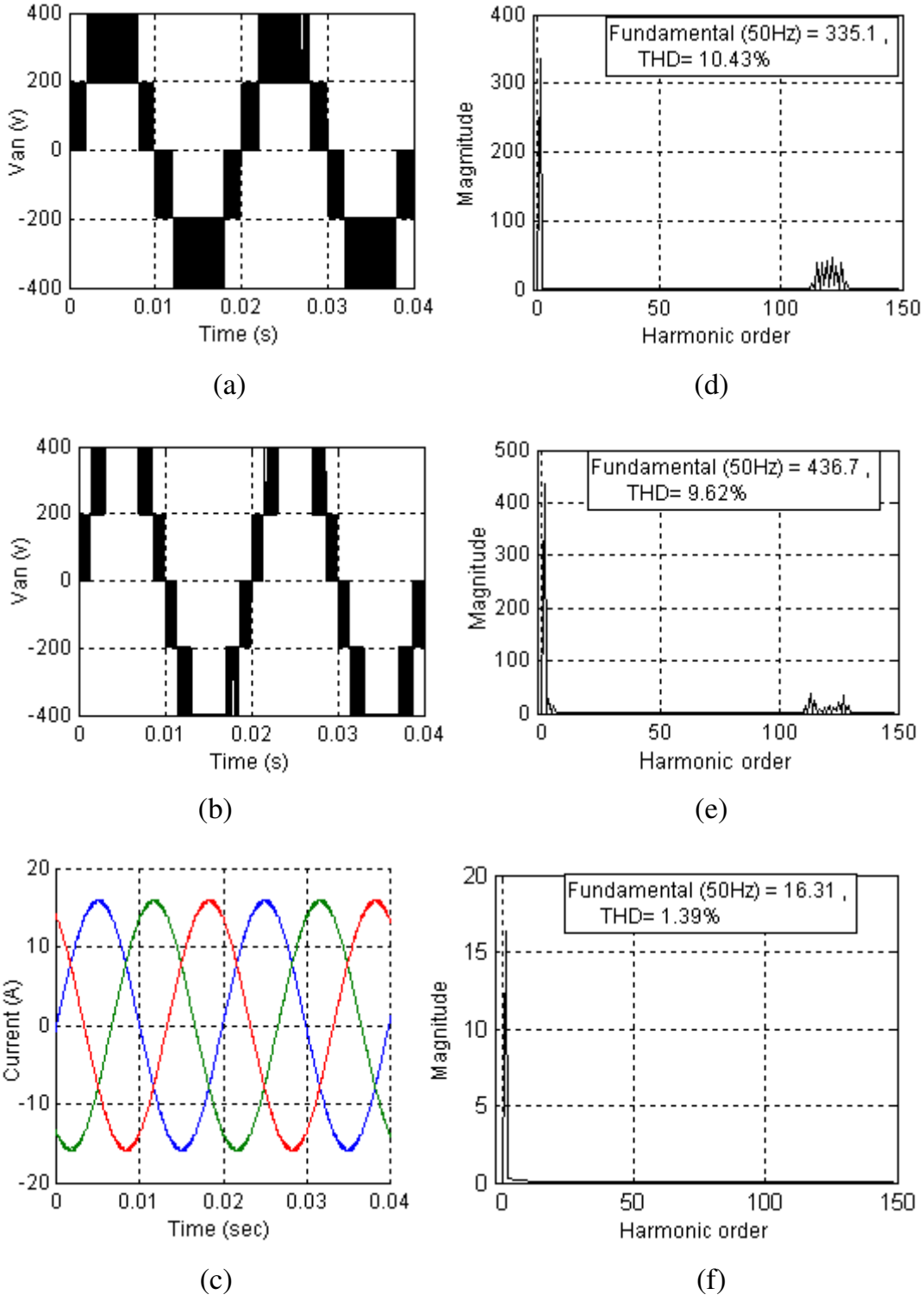


Figure 4.10 Simulation results for HPSC operation: (a)-(c) Phase voltages in linear, over-modulations, and current waveforms respectively. (d)-(f) Frequency spectrum of voltage and current waveforms of (a)-(c) respectively

The phase voltage and current waveforms with its spectrum for HCBSVM operation are shown in Figure 4.11. The WTHD of the phase voltage waveform in Figure 4.11(a) is 1.32% and no individual harmonic component has a magnitude greater than 11% of the fundamental. In HCBSVM modulation, only generates carrier sideband harmonics in the phase voltage, the dominant harmonics are adjacent to the frequency ratio of 30. While triplen multiples of these harmonics cancel in the line voltage, the remaining harmonics are smaller than those left under PD-PWM modulation.

Over-modulation condition, which happens when M>1.15, is shown in Figure 4.11(b). It has a flat top at the peak of the positive and negative cycles because both the reference signals exceed the maximum amplitude of the carrier signal. The low order harmonics in the phase voltage are minimized in the over-modulation region. One important feature of HCBSVM, by injecting offset voltages to reference modulation signals increase the DC bus usage, it also decreases harmonic distortion under low modulation indices.

The simulation results of SSHSM modulation techniques illustrate that the low frequency harmonics of the output voltage are evidently eliminated, especially in linear modulation region. Furthermore, SSHSM is also propitious for power balance of inverter cells in CMI.

4.4 SPECTRUM ANALYSIS OF THE DC CURRENT RIPPLE

Sizing of the DC-link capacitors in the CMI depends on load characterization, inverter rating and switching frequency. The ripple current has limiting effect on the capacitor life time; hence, it should be as small as possible. The DC current ripple of each modulation is unique, and it is a function of modulation index and power factor. To evaluate the effect of SSHSM on DC current ripple, spectrum results are presented, and compared with standard PD-PWM.

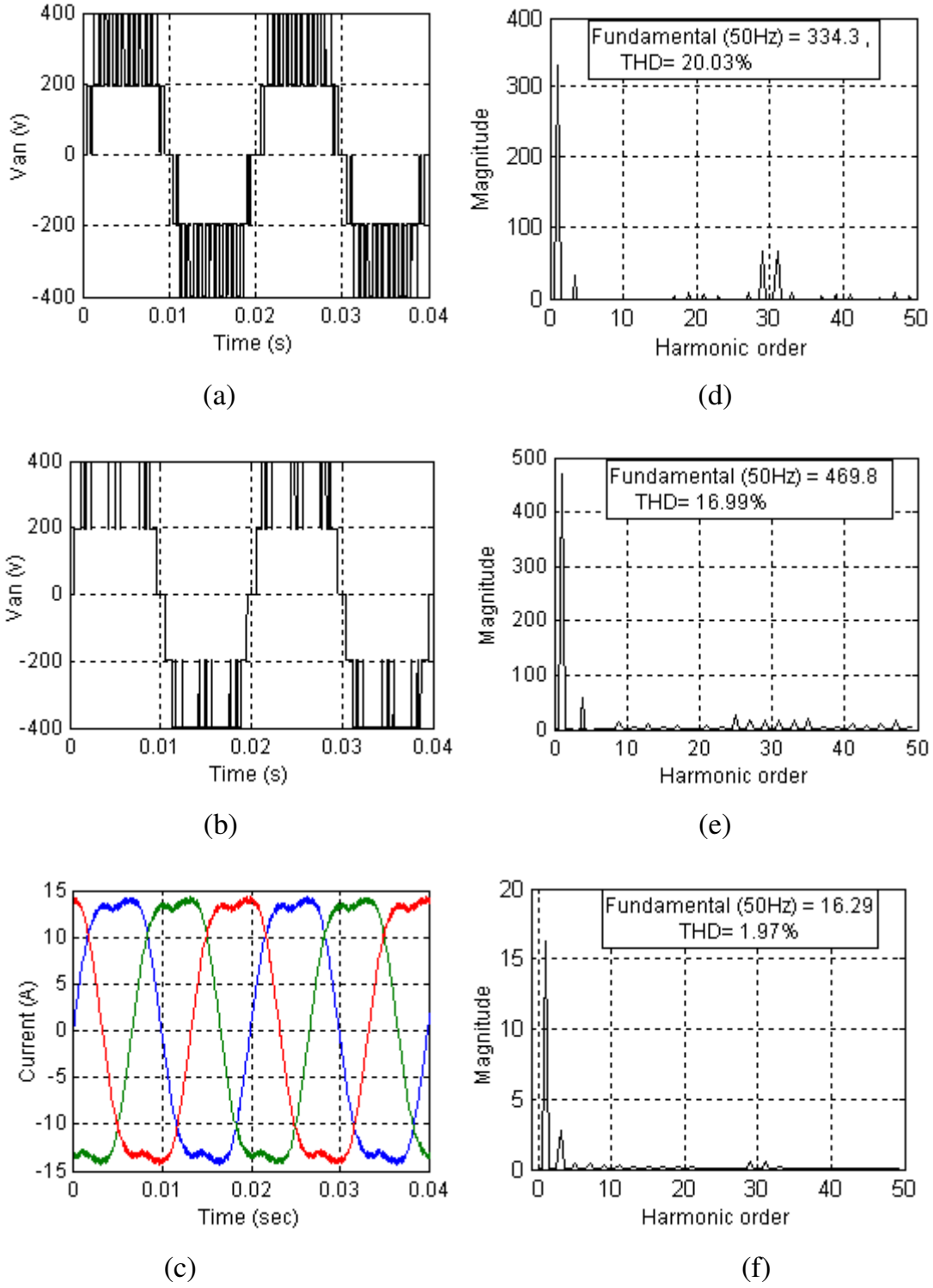


Figure 4.11 Simulation results for HCBSVM operation: (a)-(c) Phase voltages in linear, over-modulations, and current waveforms respectively. (d)-(f) Frequency spectrum of voltage and current waveforms of (a)-(c) respectively

Figure 4.12 shows the FFT of inverter input current at a unity power factor, and modulation index as M=1, for a five-level operation. The average and RMS values of the DC-link current in the inverter cells are different in conventional PD-PWM, the imbalance is noted in the spectrum shown in Figures 4.12(e)-(f). Where as in SSHSM modulation schemes, it is equal in all inverter cells due to inherent nature of SSHSM circulation.

As seen in Figure 4.12, the inverter input current consists of a DC component and higher order switching frequency components. Also, the magnitude of lower order harmonics is less than conventional PD-PWM, and then the spectrum is symmetrical for the inverter cells. As a result, low harmonic distortion and the symmetrical spectrum, reduces the kVA ratings of the DC-link filter components.

4.5 DC LINK CAPACITOR VOLTAGE BALANCING

The SSHSM circulation inherently keeps DC links fairly well in balance, as can be seen in Figures 4.13 (a)-(b), where the DC link voltage waveforms are shown without and with PWM circulations respectively. Without PWM circulation, the first module draws more power from the source, and thus, the DC link voltage varies considerably.

The second module participates in the voltage production at the reference voltage level over one, and thus, its DC link voltage fluctuates slightly less than the first module. In the case of the SSHSM circulation in use, all the inverter modules participate in the voltage production for every switching period, thus the modules share the power almost equally. This leads to a similar behavior of DC link voltages between the modules in a phase. Also, the power distribution is quite uniform, although the method does not contain any measures to achieve voltage balancing.

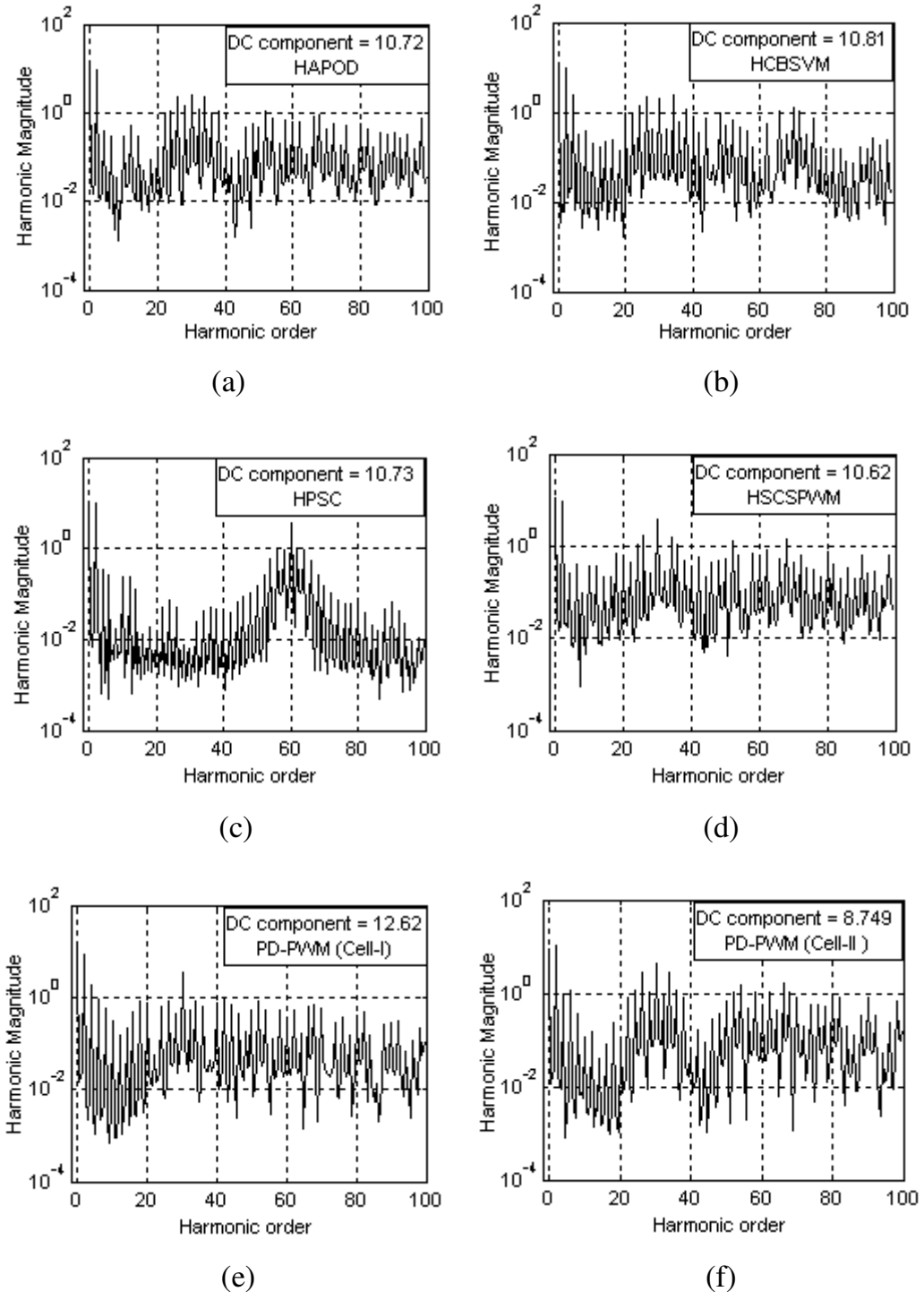
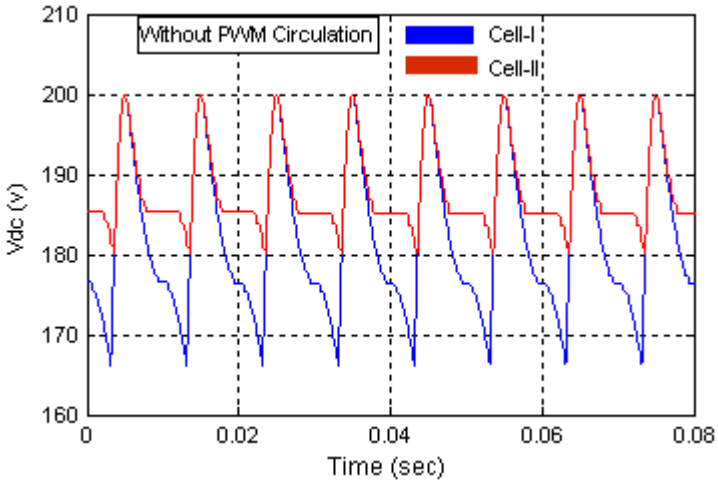
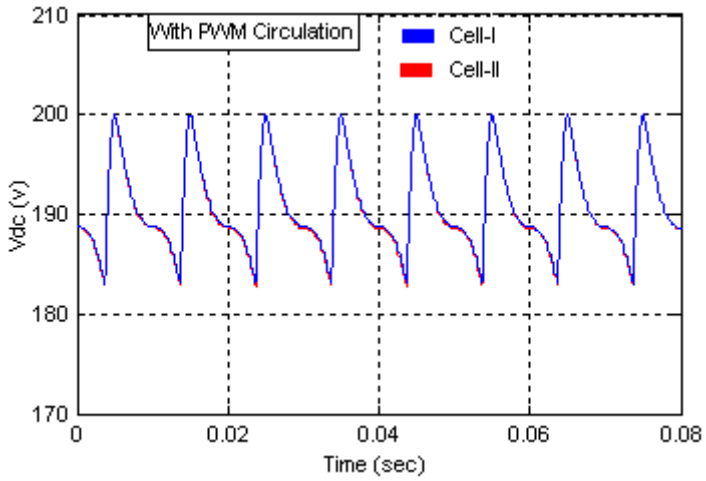


Figure 4.12 Harmonic spectrum of the DC current at unity power factor and M=1



(a)



(b)

Figure 4.13 Simulated DC-link voltages (a) without PWM circulation (b) with PWM circulation

4.6 EXPERIMENTAL RESULTS

The proposed modulation schemes are investigated with DSP-CPLD based five-level CMI. The experimental results for HAPOD, HSCSM, HCBSVM, and HPSC are presented in this section. The inverter is operated in the linear as well as over-modulation regions. A digital real time oscilloscope is used to display and capture the output waveforms and with the feature of

the Fast Fourier Transform (FFT), the spectrum of the output voltage is obtained for different operating points as discussed hereafter. The superiority of these modulations is explored by using the experimental spectral measurements. These results show that the waveforms are identical, but demonstrating that all modulation techniques are slightly different in those harmonic spectrums. The experimental operating conditions are summarized as follows.

DC bus voltage	V = 200 v
Modulation index	M= 0.85 (Linear modulation region)
	M=1.2 (Over modulation region)
Carrier frequency	f_c = 1500 Hz
Fundamental frequency	f_o = 50 Hz
Load resistance	R = 120 Ω
Load inductance	L = 24 mH

First, the voltage and current waveforms generated by HAPOD is shown to prove the effectiveness of the proposed modulation when implemented on real time. Figure 4.14 shows the experimental switched voltage and load currents obtained. It can be seen that the inverter always achieves the harmonically superior performance throughout the fundamental cycle. In Figure 4.14(d), the spectrum spread toward the two sides around the switching frequency and the peak value around the switching harmonics is slightly reduced with this proposed scheme. The HAPOD controller is operated still further and the same set of observations are taken for over-modulation region and it is presented in Figure 4.14(b). Again similar observations can be made in the harmonic spectrum; some low frequency harmonics are seen. However, the amplitude of these harmonics is not significant. The current waveform appears highly sinusoidal due to inherent low voltage distortion provided by the HAPOD. This can be more appreciated with the respective spectrum shown in Figure 4.14(f).

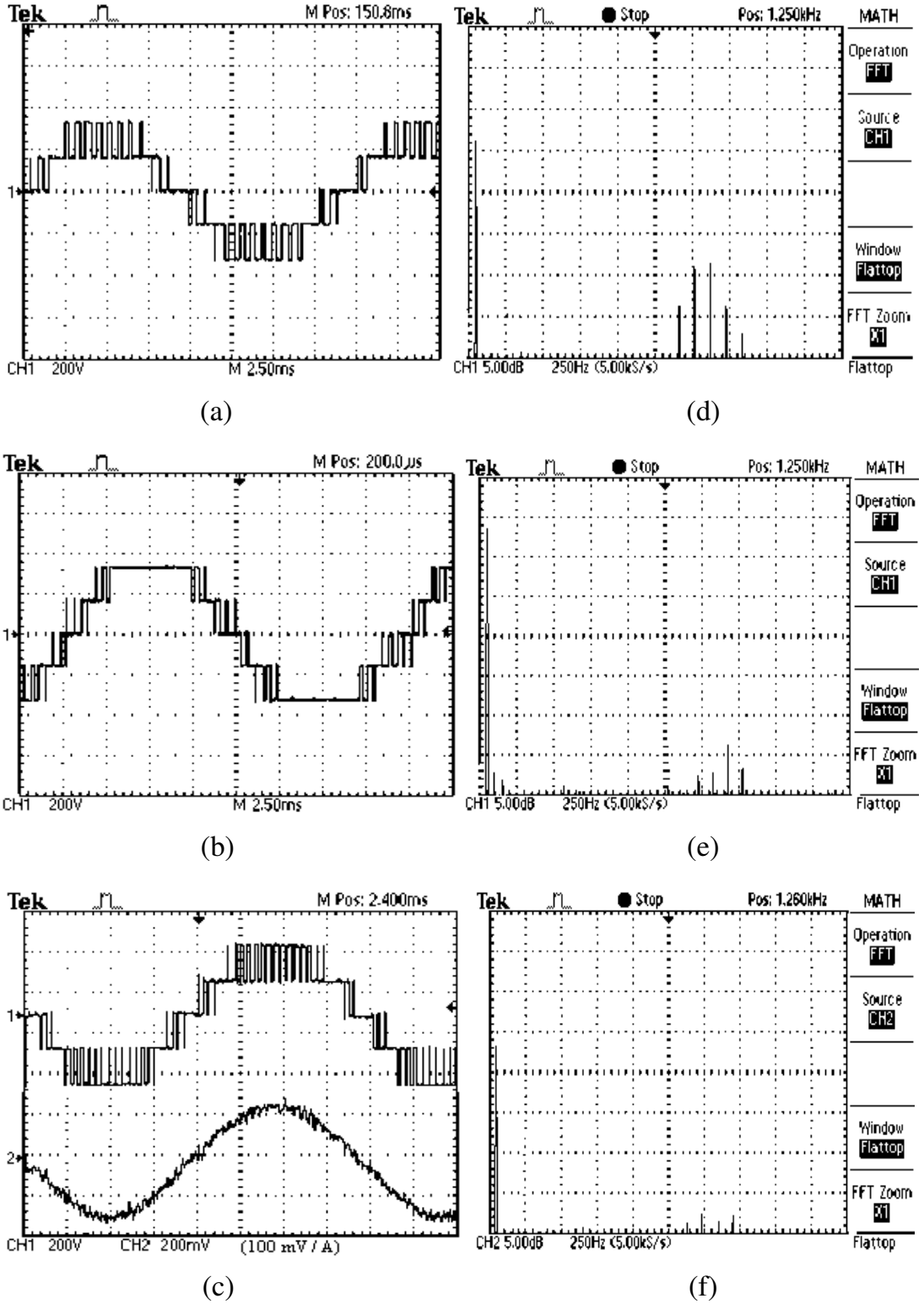


Figure 4.14 Experiment results for HAPOD operation: (a)-(c) Phase voltages in linear, over-modulations, and current waveforms respectively. (d)-(f) Frequency spectrum of voltage and current waveforms of (a)-(c) respectively

Then, the measured voltage waveforms with HSCSM are presented in Figure 4.15. The phase current waveform is found to be sinusoidal and the corresponding harmonic spectrum is shown in Figure 4.15(f). There are no significant harmonic frequencies, if the switching frequency is neglected. The current THD is very low due to inherent characteristics of HSCSM. As seen in the voltage harmonic spectrum, the amplitude of lower order harmonics are reduced and higher order harmonics are shifted to carrier frequency region. Thus the voltage THD and WTHD are minimized considerably. In the over-modulation region, the low frequency harmonics such as third and fifth harmonics are present in the spectrum as shown in Figure 4.15(e). The inverter output current ripple is dependent on the output voltage waveform quality. Thus the output PWM ripple of HSCSM appears favorable. The current distortion is low, a small percentage of the fundamental component, so it is acceptable. Harmonic spectrum, THD and WTHD measures show an excellent quality of the output voltage waveform.

The measured phase voltage and current waveforms corresponding to HCBSVM with its harmonic spectrum is represented in Figure 4.16. As expected, the spectrum shows the harmonic sidebands at multiples of PWM frequency, and it is shown in Figure 4.16 (d). The dominant harmonic components for HCBSVM are around 1.5 kHz and the harmonic magnitudes are quite low. Extending its operating range to the over-modulation region, where higher gain can be obtained while compromising some of the bandwidth is also possible. It is also experimentally verified and results presented in Figures 4.16 (b) and (e), respectively. When compared with the conventional MSPWM technique, this method offers significant benefits for increased modulation index and higher bandwidth tightly controlled throughout the operating region.

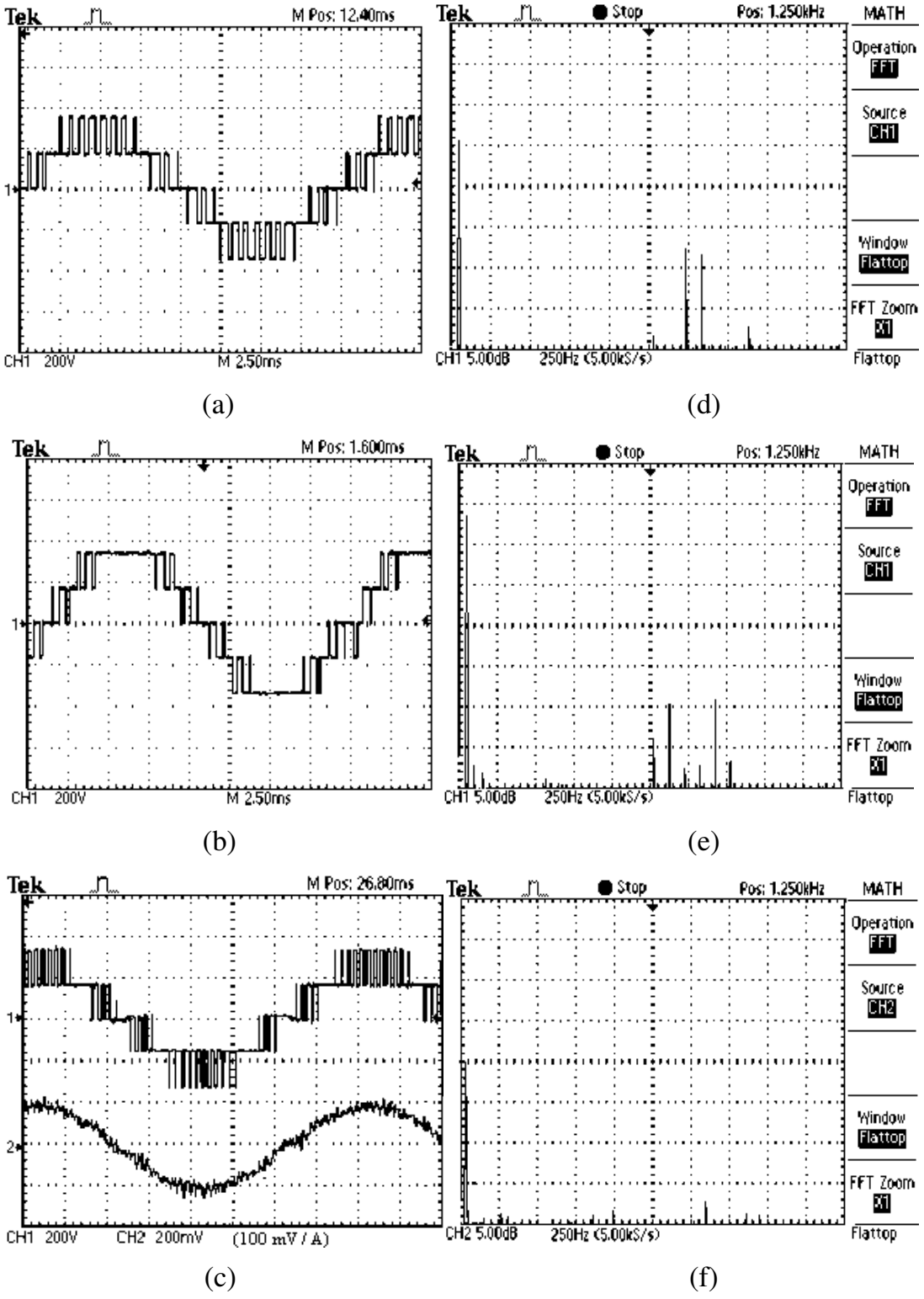


Figure 4.15 Experiment results for HSCSM operation: (a)-(c) Phase voltages in linear, over-modulations, and current waveforms respectively. (d)-(f) Frequency spectrum of voltage and current waveforms of (a)-(c) respectively

The line to neutral voltage and current waveforms with HPSC operation is shown in Figure 4.17 has an increased bandwidth. This is the result of the phase shift introduced which allows the cancellation of the switching frequency harmonics and the associated sidebands. When looking at the spectrum, the first significant harmonics are centered on 3 kHz. The sidebands are also present and these include harmonics of 29^{th}, 31^{th}, 35^{th} and 39^{th}. This implies that the most significant harmonics eliminated due to HPSC switching is 29^{th}, which is shown in Figure 4.17 (d).

The current ripple presents in the inverter output is considerably low, compared to other modulation schemes due to higher inverter equivalent switching frequency, which is desirable for better waveform quality. These improvements in harmonic performance due to the proposed SSHSM techniques are verified experimentally in linear and over modulation regions. Also, it illustrates that SSHSM methods are able to achieve dual performance of better waveform quality with an important reduction in switching frequency. A comparison of harmonic measures of the voltage and current waveforms with simulation results, confirms the superiority of SSHSM schemes for CMI operation.

4.7 THERMAL ANALYSIS

To evaluate thermal performance, power loss distributions over the inverter cells are examined in terms of heat-sink temperature rise. The experimental measures of power loss and heat-sink temperature for SSHSM modulation schemes were made with five-level inverter at same operating, and atmospheric conditions. The inverter specifications are V_{dc}=200 V, carrier frequency f_c=2~10 kHz, output frequency f_o =50 Hz, modulation index M=1, unity power factor, and ambient temperature T_a=30ºC.

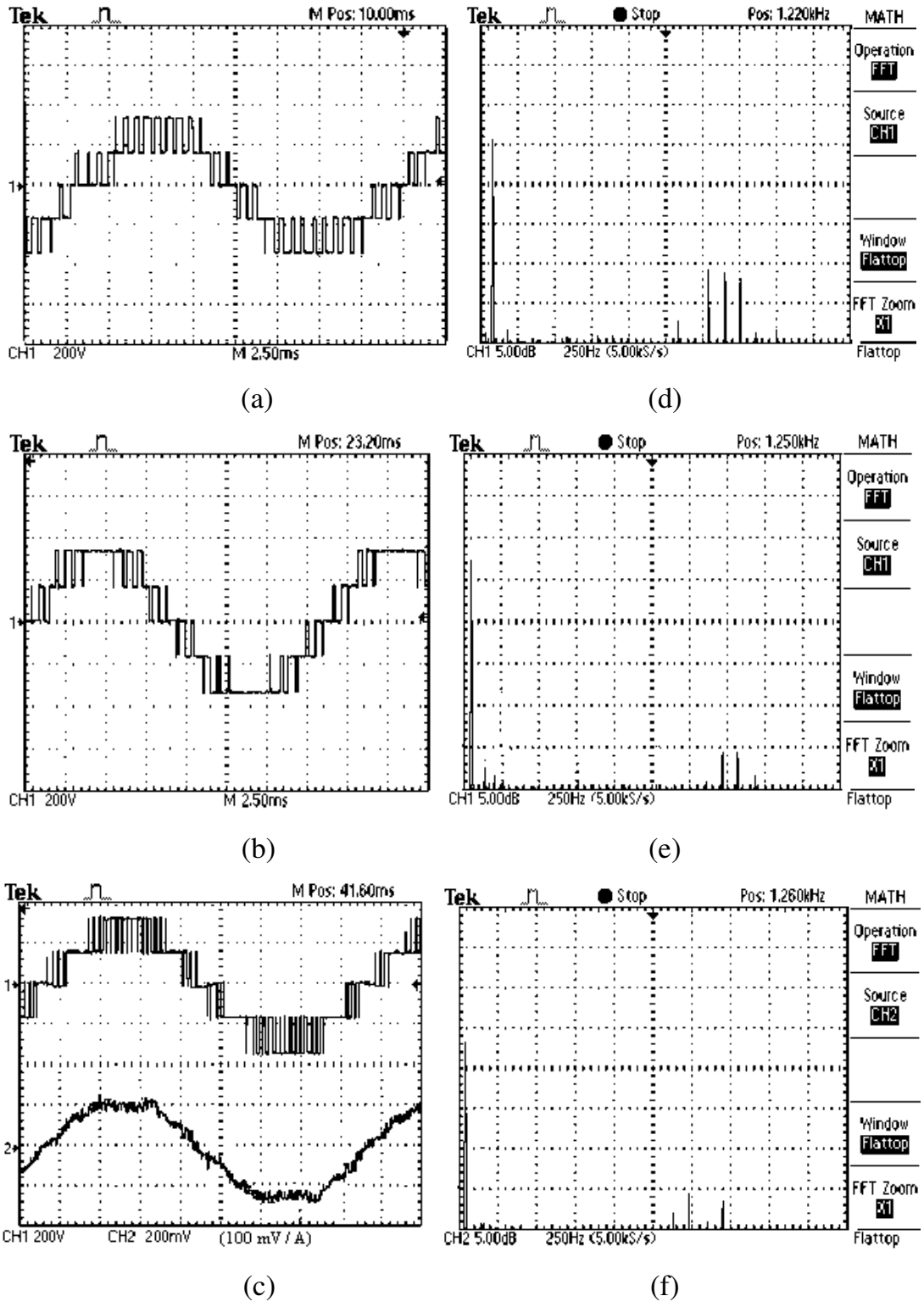


Figure 4.16 Experiment results for HCBSVM operation: (a)-(c) Phase voltages in linear, over-modulations, and current waveforms respectively. (d)-(f) Frequency spectrum of voltage and current waveforms of (a)-(c) respectively.

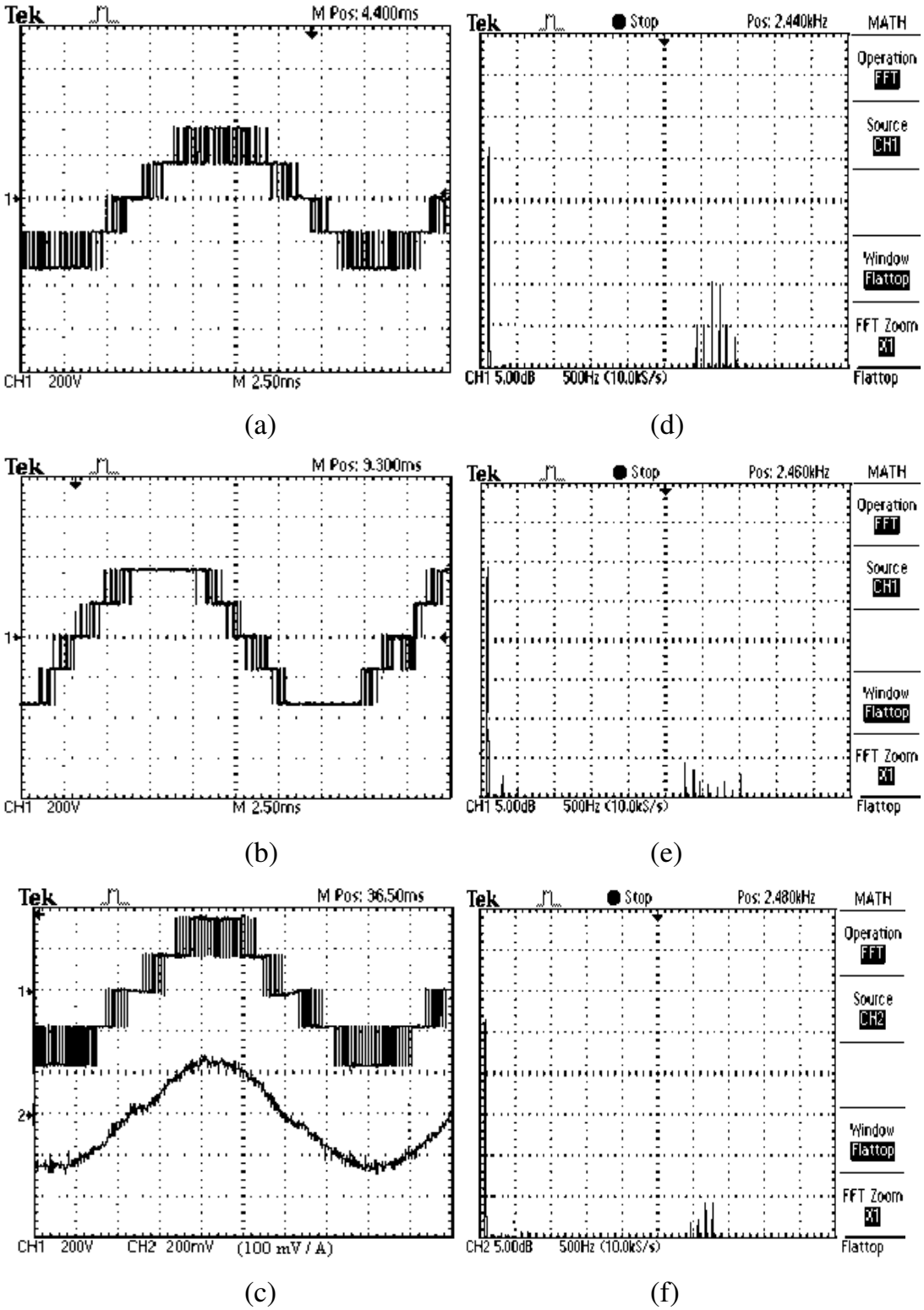


Figure 4.17 Experiment results for HPSC operation: (a)-(c) Phase voltages in linear, over-modulations and current waveforms respectively. (d)-(f) Frequency spectrum of voltage and current waveforms of (a)-(c) respectively.

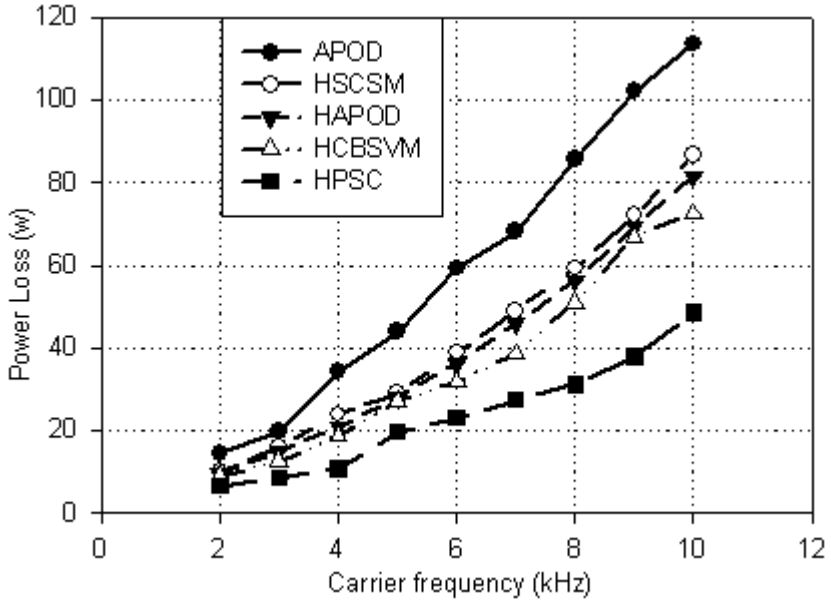
The power losses at different switching frequencies were measured for the proposed modulations, presented in Figure 4.18(a). These measures were made with digital real time oscilloscope having the feature of power analysis application key (TPS2PWR1). Thus, SSHSM ensures that the power loss is less than that of conventional APOD over the entire range of switching frequency. Among the four proposed modulations, HPSC results in minimum power loss.

The heat-sink temperature at steady state over the ambient temperature under different switching frequencies with HAPOD was measured using T-type thermocouple and shown in Figure 4.18 (b). As seen, HAPOD results in the lower heat-sink temperature rise, and thermal equalization as advantage. Also, the proposed modulation quite equally distributes losses, steadily rising with switching frequency.

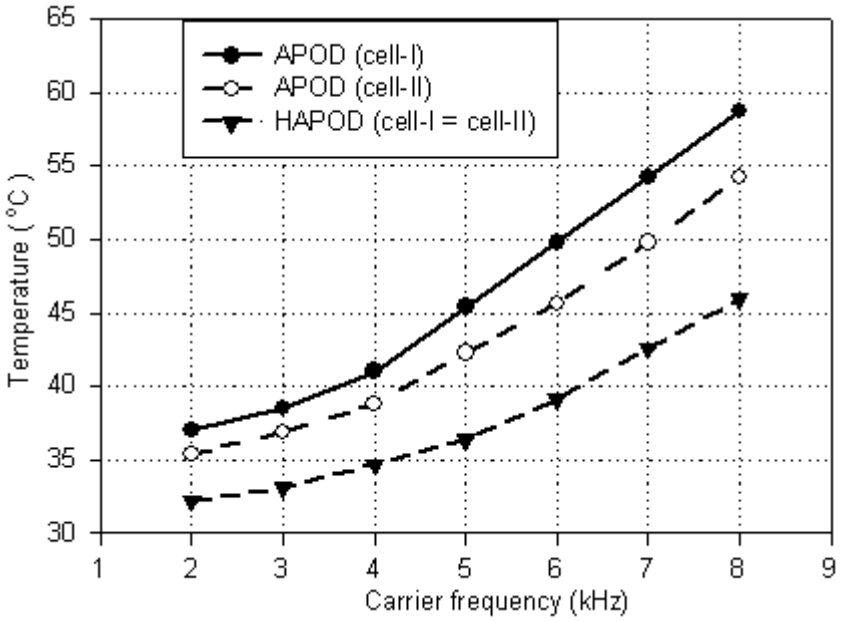
By investigating heat-sink temperature rise and power loss of the each switch of the converter, it is possible to make the thermal stress on the switches homogeneous to achieve higher power device utilization in these modulation schemes.

4.8 PERFORMANCE COMPARISON

The main modulator characteristics, such as the fundamental component, voltage linearity, switching loss, harmonic distortion, DC-link capacitor voltage balancing, and DC current ripple are thoroughly investigated with the proposed SSHSM schemes. First, the performance of standard MSPWM (PD-PWM) is performed with five-level inverter. Then, it is chosen as a reference modulation scheme to compare the features of newly developed SSHSM schemes; HAPOD, HSCSM, HCBSVM, and HPSC modulations are investigated.



(a)



(b)

Figure 4.18 (a) Measured power loss with proposed modulations (b) Measured heat-sink temperature at different switching frequencies

These methods show the incremental improvement in inverter performance including switching loss reduction and the quality of output

waveforms. The proposed modulation offers the low-harmonic content waveforms with the ability to transfer the first PWM harmonic to a higher switching frequency by increasing the effective switching frequency. These methods are closer to MSPWM in terms of THD and it is better than PD-PWM in terms of WTHD.

The HCBSVM features several advantages such as the generation of high quality currents, the capacity to operate at lower switching frequency than conventional one, and the modularity that can reduce the cost of the system. For the generation of HCBSVM, a simplified CBSVM algorithm has been used, having the merit of low computational overhead, easily implemented in industrial DSP controllers. In the higher end of the linear modulation range, HCBSVM performs better than MSPWM methods and it is comparable to PSC modulation.

Throughout its linear modulation range, HPSC has the least harmonic distortion among the other modulation schemes. With HPSC carrying the same attributes of reduced switching losses, low current distortion, and the additional benefit of equal loss distribution among the power devices, it appears to be favorable method for industrial applications.

The switching loss due to SSHSM is less than that of conventional PD-PWM for entire range of modulation index and for power factor. The switching loss reduction is more when the power factor is greater than 0.866 and modulation index is greater than 0.85. Thus, the SSHSM methods perform better than comparable techniques at high modulation indexes and also at high power factors.

The reduction of power losses over the entire range of power factor makes the SSHSM a strong candidate for a variety of applications such as active rectification, motor drives, STATCOM and distributed generation.