CHAPTER 3

SEQUENTIAL SWITCHING HYBRID SINUSOIDAL MODULATIONS

3.1 PRINCIPLE OF SEQUENTIAL SWITCHING HYBRID MODULATION

Hybrid modulation is the combination of FFPWM and MSPWM. The resultant modulation inherits the features of low switching frequency from FFPWM and good harmonic performance from MSPWM, so it provides integrated solutions of switching loss reduction with good output performance. In this modulation technique, the power devices of each inverter cell are operated at two different frequencies, two being commutated at fundamental frequency, while the other two switches are modulated at MSPWM, therefore the resultant switching patterns are same as those obtained with MSPWM.

A sequential switching scheme is introduced with this hybrid modulation in order to overcome unequal switching losses and therefore differential heating among the power devices. It helps for each switch stressed in the same way, and to achieve equal losses in each switch, therefore a uniform temperature distribution within the inverter cell. A simple base MSPWM circulation scheme is also embedded to get resultant hybrid PWM circulation makes balanced power dissipation among the power modules. The general structure of five-level sequential switching hybrid sinusoidal modulation scheme is shown in Figure 3.1.

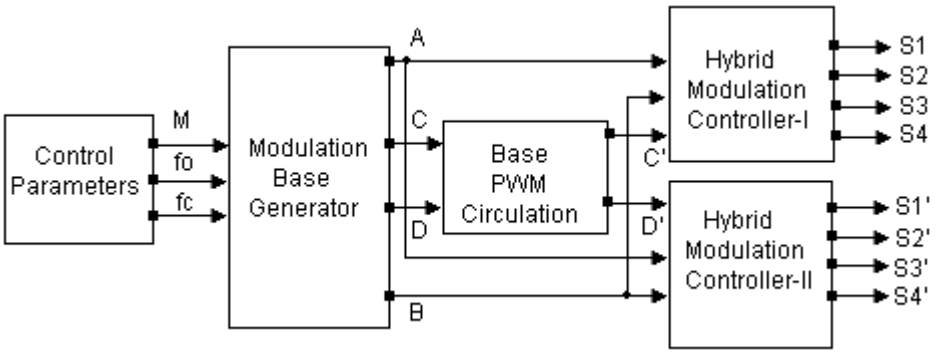


Figure 3.1 Scheme of proposed sequential switching hybrid modulation

The process of developing hybrid modulation pulses consists of modulation base generator, base MSPWM circulation and hybrid modulation controllers. In this modulation strategy, three base modulation pulses are required for each inverter cell in a CMI. Base modulation pulses are Sequential Switching Pulse (SSP), FFPWM and MSPWM for each inverter cell. A SSP (A) is a square wave signal with 50% duty ratio and half the fundamental frequency. This signal makes every power switch operating at MSPWM and FFPWM sequentially to equalize the power losses among the switches within a cell.

FFPWM (B) is a square wave signal synchronized with the modulation waveform; it is active high during the positive half cycle of the modulation signal, and active low during negative half cycle. SSP and FFPWM pulses are same for all inverter cells in each phase. MSPWM (C and D) for each inverter cell is depend upon type of well-known APOD, PSC, CBSVM, and SCSM pulses used. The control parameters are modulation index (M), carrier frequency (f_c), and fundamental frequency (f_o). The proposed hybrid modulation strategies are HAPOD, HPSC, HCBSVM, and HSCSM.

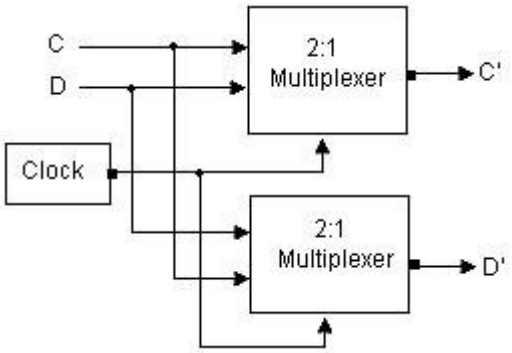
3.2 BASE MSPWM CIRCULATION

Equal loading of the inverter modules has an influence on the DC link voltage balance of a phase. The voltage balance between different inverter cells in a phase is crucial for good voltage quality. Also for long operating time expectancy, it is important to share the power loss among every module, and furthermore, to every power device in the inverter cell. This is one of the key issues the modulation should cover. A simple base MSPWM circulation scheme is introduced here to get resultant SSHSM circulation among the power modules. The scheme of five-level base MSPWM circulation is shown in Figure 3.2 (a), consists of two 2:1 multiplexer, and selects one among the two MSPWMs based on the select clock signal.

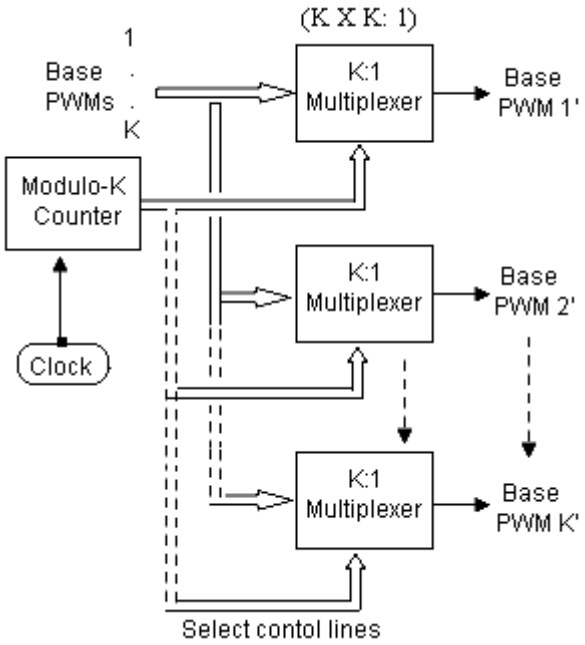
The clock frequency makes the time base for PWM circulation from one module to another. If the clock frequency is $\frac{f_o}{4}$, then the PWM circulation is used in such a way that after each two fundamental periods, every module produces different sections of the voltage required. Normally the clock frequency is same as switching frequency to balance DC-link capacitor voltage, DC current loading, and power dissipation among the series connected cells. This PWM circulation based on simple multiplexer logic circuits, which makes the applicability of the algorithm very effective in a CPLD or FPGA.

Base MSPWMs are circulated using N-level PWM circulation module for N-level inverter operation to balance the power dissipation among the cells. Figure 3.2(b) shows the block diagram for N-level base MSPWM circulation module. This module consists of clock generator, modulo-K counter, and a multiplexer circuit. The clock frequency makes the time base for circulation from one to the number of modules in series. Modulo-K

counter makes control signals for multiplexer to select appropriate input PWM channel. Multiplexer circuit consists of (K X K: 1) module for PWM selection, and it selects the PWM channel based on control signals.



(a)



(b)

Figure 3.2 Scheme of base MSPWM circulation: (a) five-level (b) N-level inverter

The circulation is arranged so that the phase modules in series are numbered from one to the number of modules. For every switching period,

the order is changed so that the first module PWM becomes the second module; the second becomes the third and so on while the last module PWM shifts to the first. The principle of the SSHSM circulation is illustrated in Figure 3.6, where the modules alternately participate in the SSHSM operation and the corresponding phase voltage is presented at the same instant.

3.3 HYBRID MODULATION CONTROLLER

Hybrid Modulation Controller (HMC) combines SSP, FFPWM and MSPWM, that produces hybrid modulation pulses. The input pulses for HMC are SSP (A), FFPWM (B), and MSPWM ($C^{'}$ and $D^{'}$). As level increases, the number of independent HMC also increases. The number of controllers for N-level inverter are (N-1)/2. It is designed by using a simple combinational logic and the functions of the combinational logic for a five-level hybrid PWM operation are expressed as

$$\begin{aligned} S1 &= A\,B\,C^{'} + \overline{A}\,B \\ S2 &= \overline{A}\,B\,C^{'} + \overline{A}\,\overline{B} \\ S3 &= \overline{A}\,\overline{B}\,C^{'} + A\,\overline{B} \\ S4 &= \overline{A}\,B\,C^{'} + A\,B \end{aligned} \quad \text{and} \quad \begin{aligned} S1' &= A\,B\,D^{'} + \overline{A}\,B \\ S2' &= \overline{A}\,B\,D^{'} + \overline{A}\,\overline{B} \\ S3' &= \overline{A}\,\overline{B}\,D^{'} + A\,\overline{B} \\ S4' &= \overline{A}\,B\,D^{'} + A\,B \end{aligned} \qquad (3.1)$$

The functional logic diagram of five-level hybrid modulation controller is shown in Figure 3.3. An independent HMC is used to mix a SSP, FFPWM and its corresponding MSPWM for developing hybrid modulation pulses in K^{th} inverter cell. Similarly, SSHSM pulses are developed for all inverter cells of a CMI. Totally 4K gate pulses per phase are developed to operate N-level inverter.

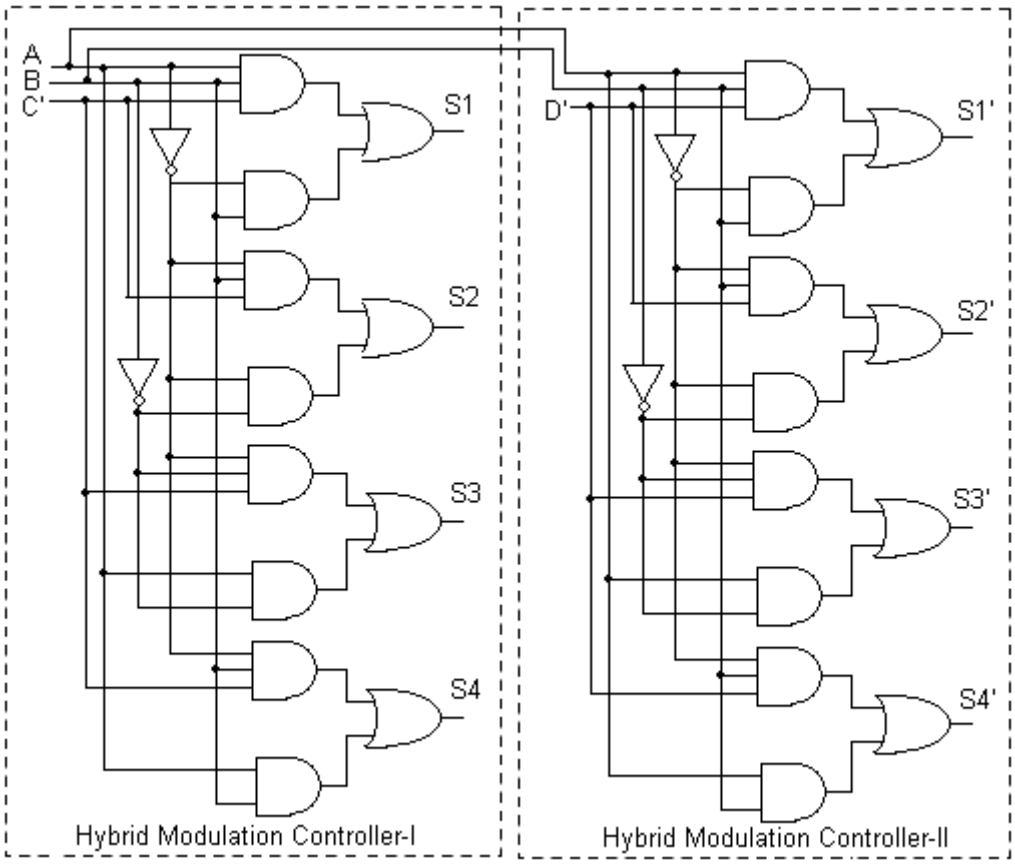


Figure 3.3 Functional logic diagram of five-level hybrid modulation controller

3.4 HYBRID ALTERNATE PHASE OPPOSITION DISPOSITION MODULATION

In this proposed modulation strategy, FFPWM and APOD pulses are combined to produce HAPOD pulses for each inverter cell. Figure 3.4 shows the general structure of the proposed sequential switching HAPOD modulation scheme. It consists of base APOD modulator, APOD circulation module, and HMC to generate new HAPOD modulation pulses. Unipolar N-level APOD operation consists of (N-1)/2 different carriers. The carriers have the same frequency f_c, the same peak to peak amplitude A_c, and are disposed so that the bands they occupy are contiguous. They are defined as

$$C_i = V[(-1)^{x(i)} v_c(f_c, \varphi) + i - \frac{N}{2}],\ i=1, 2\ldots (N-1)/2 \qquad (3.2)$$

A normalized symmetrical triangular carrier (v_c) is defined as

$$v_c(f_c, \varphi) = (-1)^{[\theta]}[(\theta \bmod 2) - 1] + \frac{1}{2},\quad \theta = \frac{2\pi f_c t + \varphi}{\pi} \qquad (3.3)$$

where φ represents the phase angle of v_c. v_c is a periodic function with period $T_c = 1/f_c$.

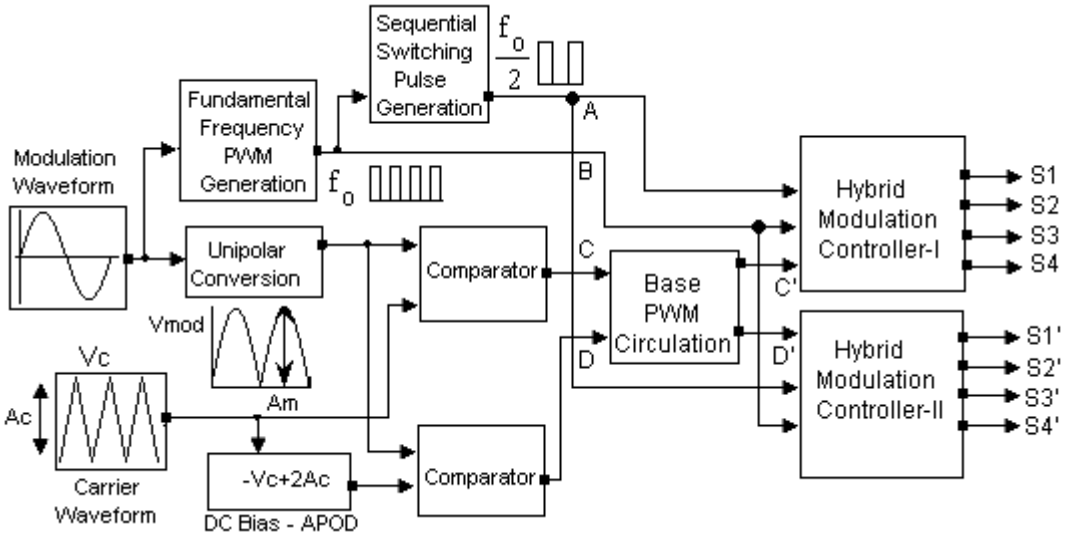


Figure 3.4 Scheme of five-level sequential switching HAPOD modulation

Symmetrical triangular carriers used in this modulation generate less harmonic distortion at the inverter's output. Disposition form x (i) may assume 0 or 1 and identifies whether C_i is in phase or in opposition to an assumed reference carrier. Here we choose C_1 as the reference carrier; thus x(1) =0. The zero reference is always placed in the middle of the carrier set. All carriers are alternatively in phase opposition for APOD modulation

$x_{APOD}(i)=(i-1) \bmod 2$. The modulating waveform v_m is an arbitrary waveform with the frequency f_o. The sinusoidal modulation signal can be described as

$$v_{mod} = A_m \sin \omega_o t \tag{3.4}$$

APOD pulses for inverter cell-I (C) are obtained by the comparison of unipolar modulation waveform (v_{mod}) with carrier waveform (v_c). APOD pulses for inverter cell-II (D) are obtained by the comparison of same unipolar modulation waveform with level shifted carrier waveform ($-V_c + 2A_c$). The base APOD pulses (A, B, C and D) for five-level HAPOD are shown in Figure 3.5. The HMC combines the base APOD pulses and produce sequential switching HAPOD pulses.

In Figure 3.6, it is shown that each gate pulse is composed of both FFPWM and APOD pulses. If SSP A=1, then S1, S2, S1' and S2' are operated with APOD, while S3, S4, S3', S4' are operated at FFPWM. If SSP A=0, then S1, S2, S1' and S2' are operated at FFPWM, while S3, S4, S3' and S4' are operated with APOD. Since A is a sequential signal, the average switching frequency amongst the four power devices in each inverter cell is equalized. Voltage stress and current stress of power switches is also inherently equalized with this modulation.

After every two fundamental frequency periods, the SSHSM pulse pattern is changed so that the first module (S_1, S_2, S_3, and S_4) becomes the second module (S_1', S_2', S_3', and S_4'), and the second one shifts to the first, and it is shown in Figure 3.6. It can be observed from the waveforms of Vh1 and Vh2 that the implementation of SSHSM circulation makes the inverter modules operate at same average switching frequency with the same conduction period.

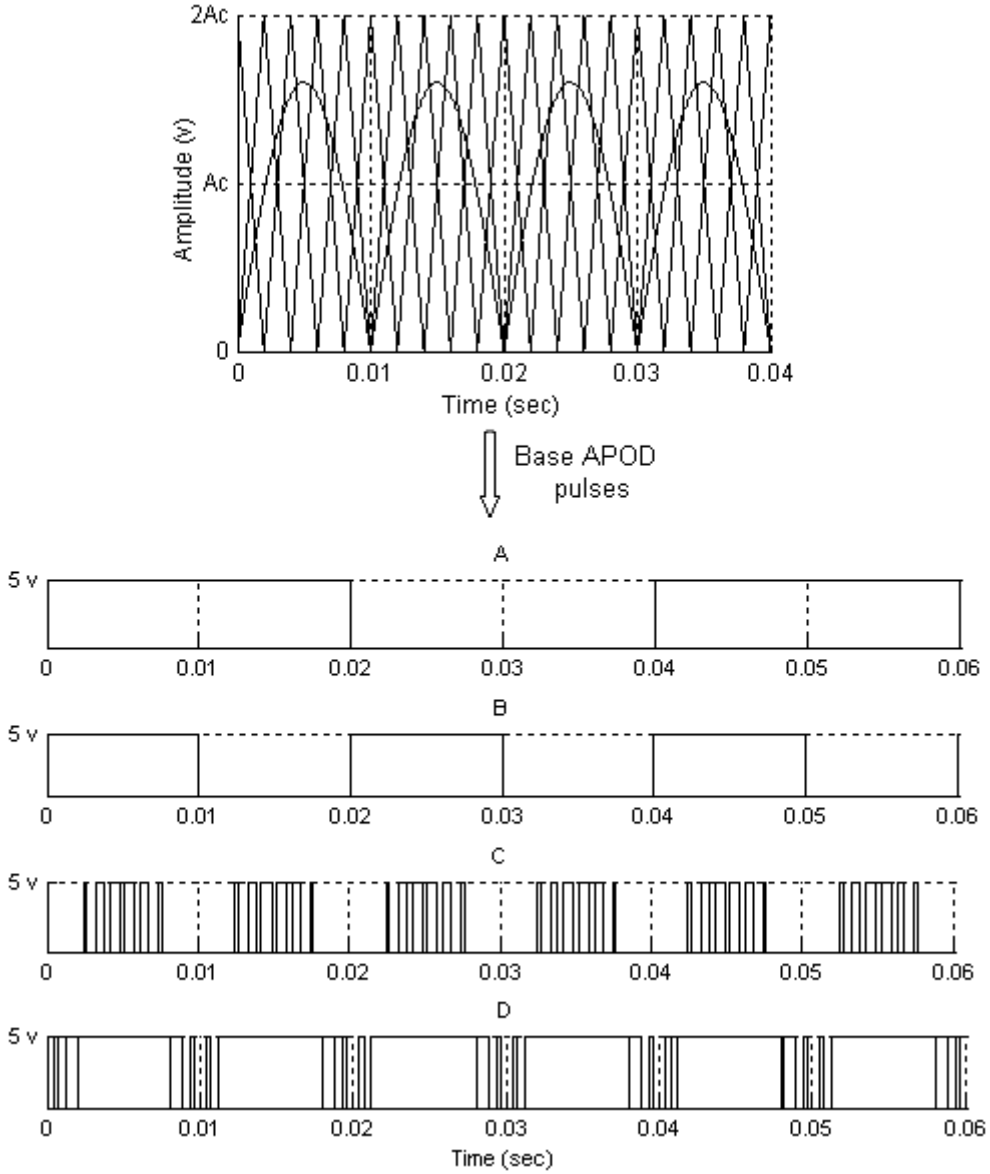


Figure 3.5 Five-level base APOD pulse pattern

The principle of the HAPOD circulation is illustrated in Figure 3.6 with clock frequency $\frac{f_o}{4}$, so that for every two fundamental periods, each module produces different sections of the voltage required, whereas the operating clock frequency is same as switching frequency. As a result, all inverter modules operate in a balanced condition with the same power handling capability and switching losses.

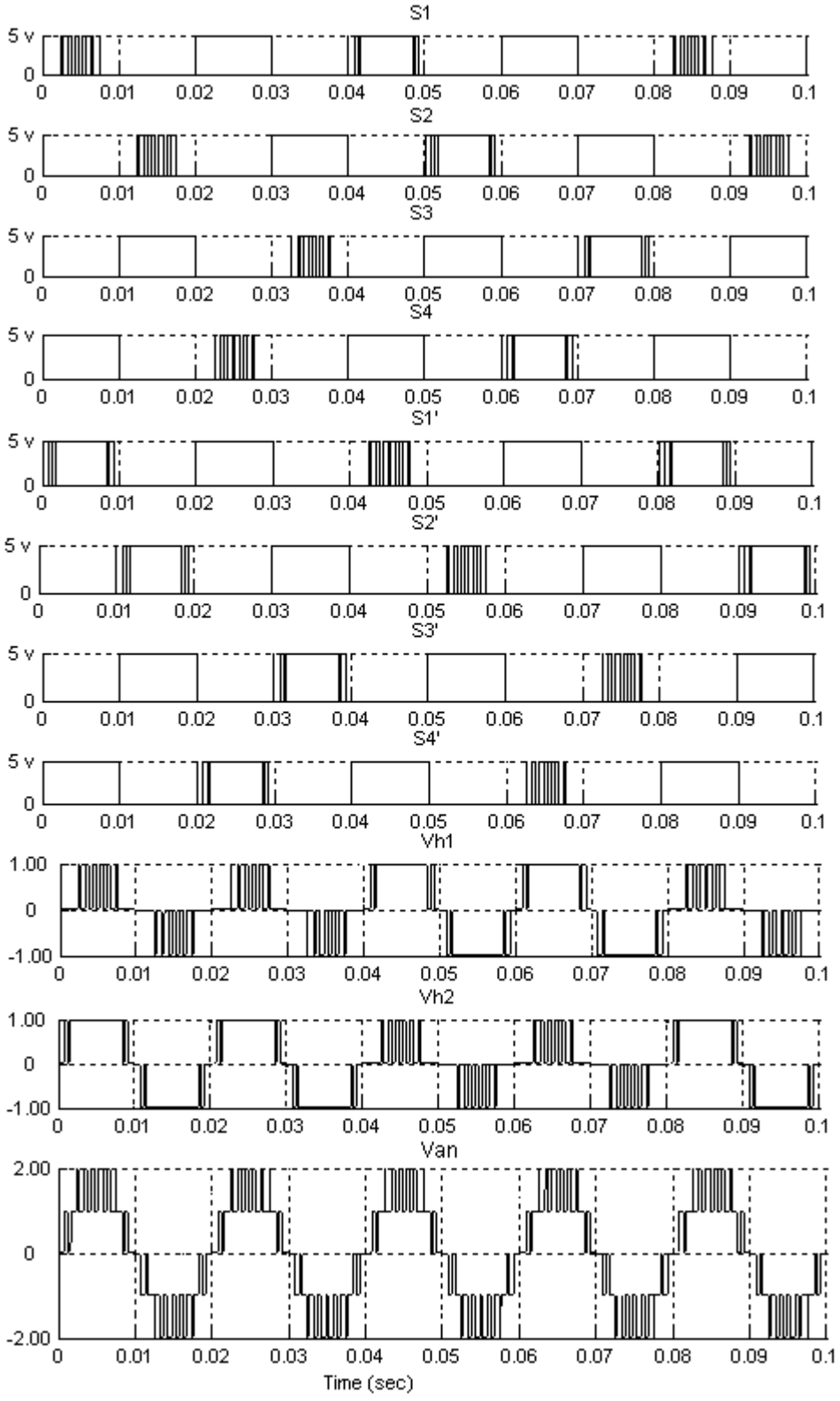


Figure 3.6 Five-level sequential switching HAPOD pulse pattern

It can be observed from the waveforms of V_{h1} and V_{h2} that the implementation of the rotating sequence makes the inverter cells operate at the same average switching frequency with the same conduction period. The inverter output (V_{an}) is the sum of voltage output from inverter cells (V_{h1} and V_{h2}). As it is concluded from Figure 3.6, the resultant inverter switching is same as the type of MSPWM used. In addition to that, the FFPWM operates in parallel with MSPWM, this leads to the reduction of switching frequency of the power devices. Thus, their switching losses also decrease.

3.5 HYBRID SINGLE CARRIER SINUSOIDAL MODULATION

In HSCSM, FFPWM and SCSM pulses are mixed for each inverter cell operation, and therefore the output contains the features of FFPWM and SCSM. Figure 3.7 shows the scheme of the proposed sequential switching HSCSM. It consists of base SCSM modulator, SCSM circulation module and HMC to generate new HSCSM pulses.

SCSM pulses are obtained by the comparison of unipolar modulation waveform of each inverter cell with single carrier waveform. The amplitude of the modulation waveform is defined as $A_m = K\,M\,A_c$, where A_c is amplitude of the carrier and M is modulation index. The modulation and carrier signals can be described as

$$M_1(t) = A_m \sin \omega_o t \tag{3.5}$$

$$M_2(t) = A_m \sin\ \omega_o t - A_c \tag{3.6}$$

$$C(t) = A_c[4\ t\ f_c - \frac{1}{2}](-1)^{[2f_c\ t]} \tag{3.7}$$

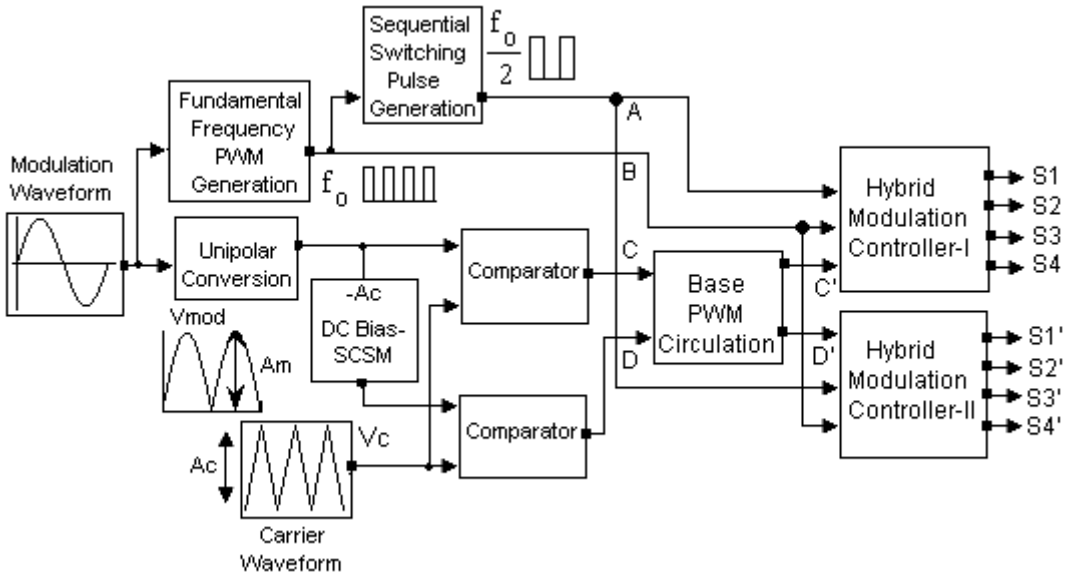


Figure 3.7 Scheme of five-level sequential switching HSCSM

SCSM pulses for inverter cell-I (C) are obtained by the comparison between unipolar modulation waveform and carrier signal, while SCSM pulses for inverter cell-II (D) are obtained by the comparison between unipolar modulation waveform with bias of $-A_c$ and the same carrier waveform. The comparison is designed such that if M_1 (t) is greater than C (t), C is generated. On the other hand, if M_2 (t) is greater than C (t), D is generated. If there is no intersection, the C and D remain at 0. The base modulation pulses (A, B, C, and D) are shown in Figure 3.8.

It is desirable to obtain mathematical expressions that define the switching instants for SCSM. The i^{th} rising edge is defined as the intersection of the carrier slope and two set of sampled modulation signals M_1 (i) and M_2 (i).

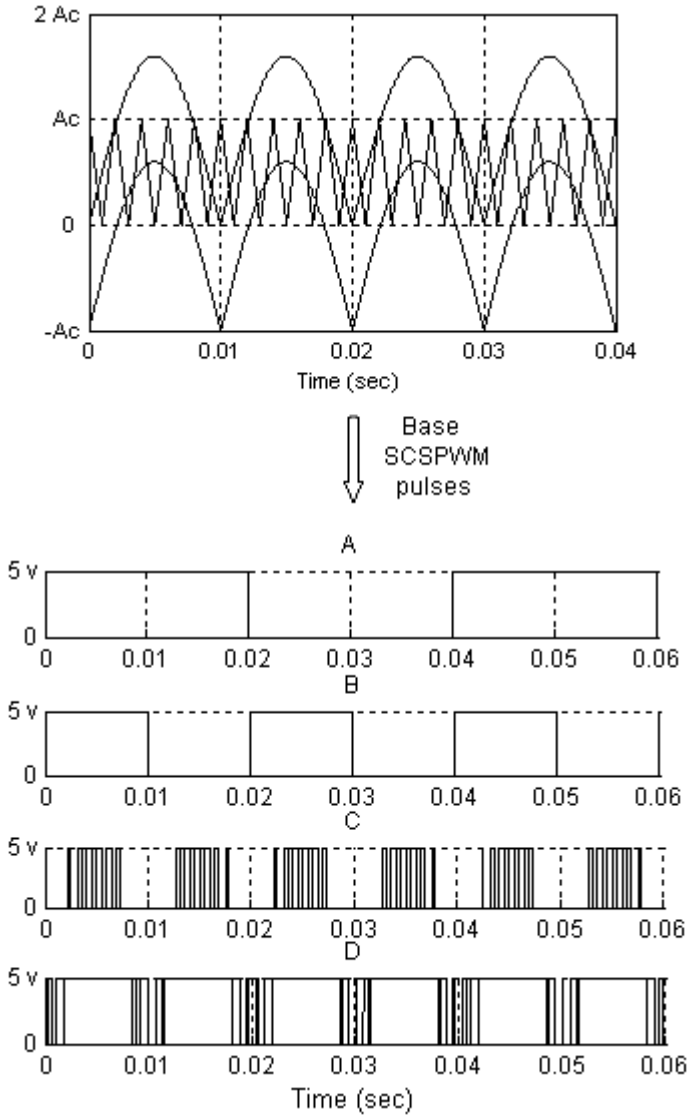


Figure 3.8 Five-level base SCSM pulse pattern

The symmetric regular sampled modulation and carrier signals $M_1(i)$, $M_2(i)$, and $C(i)$ can be expressed as:

$$M_1(i) = A_m \sin [\ \omega(i)\ + \frac{\pi}{P}] \tag{3.8}$$

$$M_2(i) = A_m \sin [\ \omega(i) + \frac{\pi}{P}] - A_c \tag{3.9}$$

$$C(i) = -2\ A_c\ f_c\ \alpha(i) + h\ A_c,\ h=1,\ 2,\ 3\ldots \tag{3.10}$$

where angular frequency $\omega = \frac{2\pi}{P}$.

A mathematical expressions used to generate the i^{th} SCSM pulses for inverter cells (C and D) is given by

$$\alpha_C(i) = \frac{1}{2f_c}[(2i-1) - \frac{A_m}{A_c}\sin(\omega\,(i-1) + \frac{\pi}{P})] \tag{3.11}$$

$$\alpha_D(i) = \frac{1}{2f_c}[(2i) - \frac{A_m}{A_c}\sin(\omega\,(i-1) + \frac{\pi}{P})] \tag{3.12}$$

where i represents a position of each modulated pulses (i=1, 2, 3….. P/2).

It is also important to note that frequency modulation ratio (P) of the inverter must be selected to be even. This provision must be obeyed to ensure the output waveform obtained is quarter wave symmetry. HMC is designed to combine base SCSM pulses to generate HSCSM pulses. The developed HSCSM pulses are shown in Figure 3.9. The HSCSM is composed of both FFPWM and SCSM pulses. If SSP A=1, S1, S2, S1' and S2' are operated with SCSM, while S3, S4, S3', S4' are operated at FFPWM. If SSP A=0, S1, S2, S1' and S2' are operated at FFPWM, while S3, S4, S3'and S4' are operated with SCSM.

The HSCSM circulation is shown in Figure 3.9, with clock frequency $\frac{f_o}{4}$, so that for every two fundamental frequency periods, the HSCSM pattern is changed so that the first module (S_1, S_2, S_3, and S_4) becomes the second module (S_1', S_2', S_3', and S_4'), and the second one shifts to the first. Consequently, the resultant switching pattern of the inverter are the same as those obtained with SCSM. As the modulation pulse of one switch is clamped to active high, in parallel with SCSM operation of another switch. This leads to the switching frequency of the power devices being reduced, and therefore switching losses also decreased.

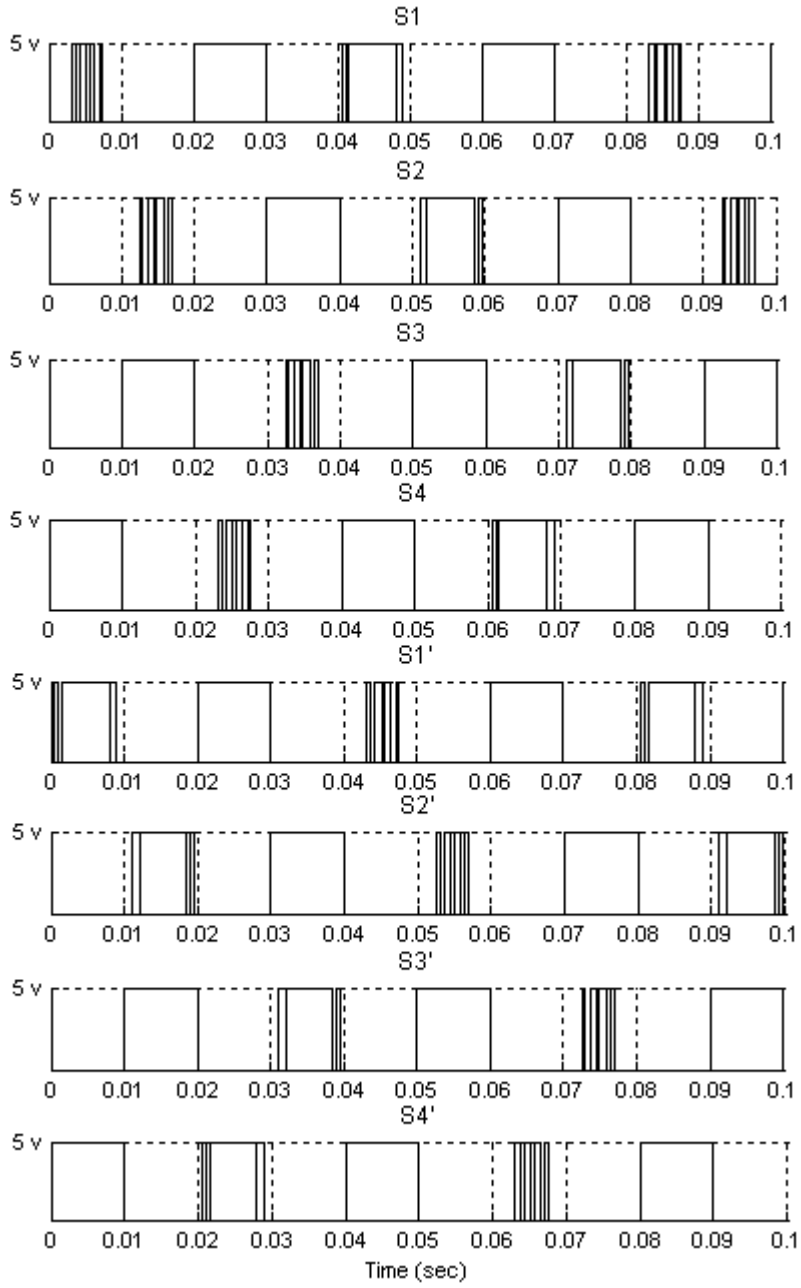


Figure 3.9 Five-level sequential switching HSCSM pulse pattern

3.6 HYBRID CARRIER BASED SPACE VECTOR MODULATION

HCBSVM is a combination of CBSVM and FFPWM. CBSVM is derived from the addition of a common offset voltage to the three-phase voltage references. This will center the active space-vectors in the switching

period, and hence match the carrier modulation to get optimized SVM. The offset voltage for multilevel operation can be calculated as:

$$V_{off} = -\frac{\max(V_a, V_b, V_c) + \min(V_a, V_b, V_c)}{2} \tag{3.13}$$

$$V_k' = (V_k + V_{off} + V_{dc}) \bmod \left(\frac{2V_{dc}}{N-1} \right), k = a, b, c \tag{3.14}$$

$$V_{off}' = \frac{V_{dc}}{N-1} - \frac{\max(V_a', V_b', V_c') + \min(V_a', V_b', V_c')}{2} \tag{3.15}$$

The modified phase references are then obtained by adding V_{off} and V_{off}' to the reference waveform V_a, V_b or V_c. The modulus function in V_k' shifts the reference voltages vertically so that their carrier intersections lie within a common carrier band in the entire modulation range. An additional common mode voltage V_{off}' correctly positions the first and last switching transitions in each switching period.

This five-level CBSVM operation consists of two different carriers, where these are in phase. The carriers have the same frequency f_c, the same peak to peak amplitude A_c and are disposed so that the bands they occupy are contiguous. The carriers used in this modulation are based on PD category. For three phase output, the triplen harmonics of voltage or current will be eliminated due to star or delta connection of the load. PD scheme is more convenient for CBSVM which is an optimal solution for three phase inverters. Base CBSVM is based on sampled amplitude of phase references and this algorithm is suitable for real time implementation on DSP processors.

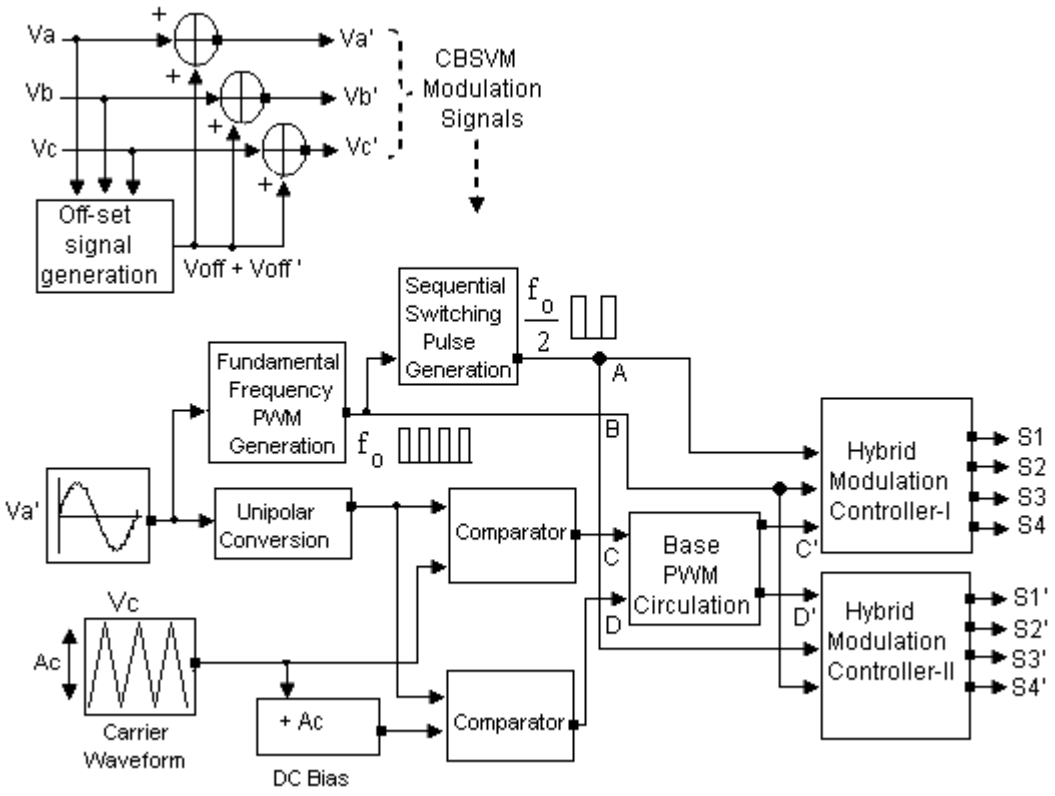


Figure 3.10 Scheme of hybrid carrier based space vector modulation

In this modulation also, three base modulation pulses are required for each inverter cell operation. SSP is a square wave with a 50% duty ratio and half of the fundamental frequency. FFPWM is a square wave signal synchronized with a modified phase reference waveform; B=1 during the positive half cycle of the modulation signal, and B=0 during negative half cycle.

CBSVM is based on a comparison of the modified sinusoidal reference signal ($V_k + V_{off} + V_{off}'$) with each carrier to determine the voltage level that the inverter should switch to. SSP and FFPWM pulses are the same for all inverter cells in each phase. The base CBSVM pulses for a HCBSVM controller are shown in Figure 3.11.

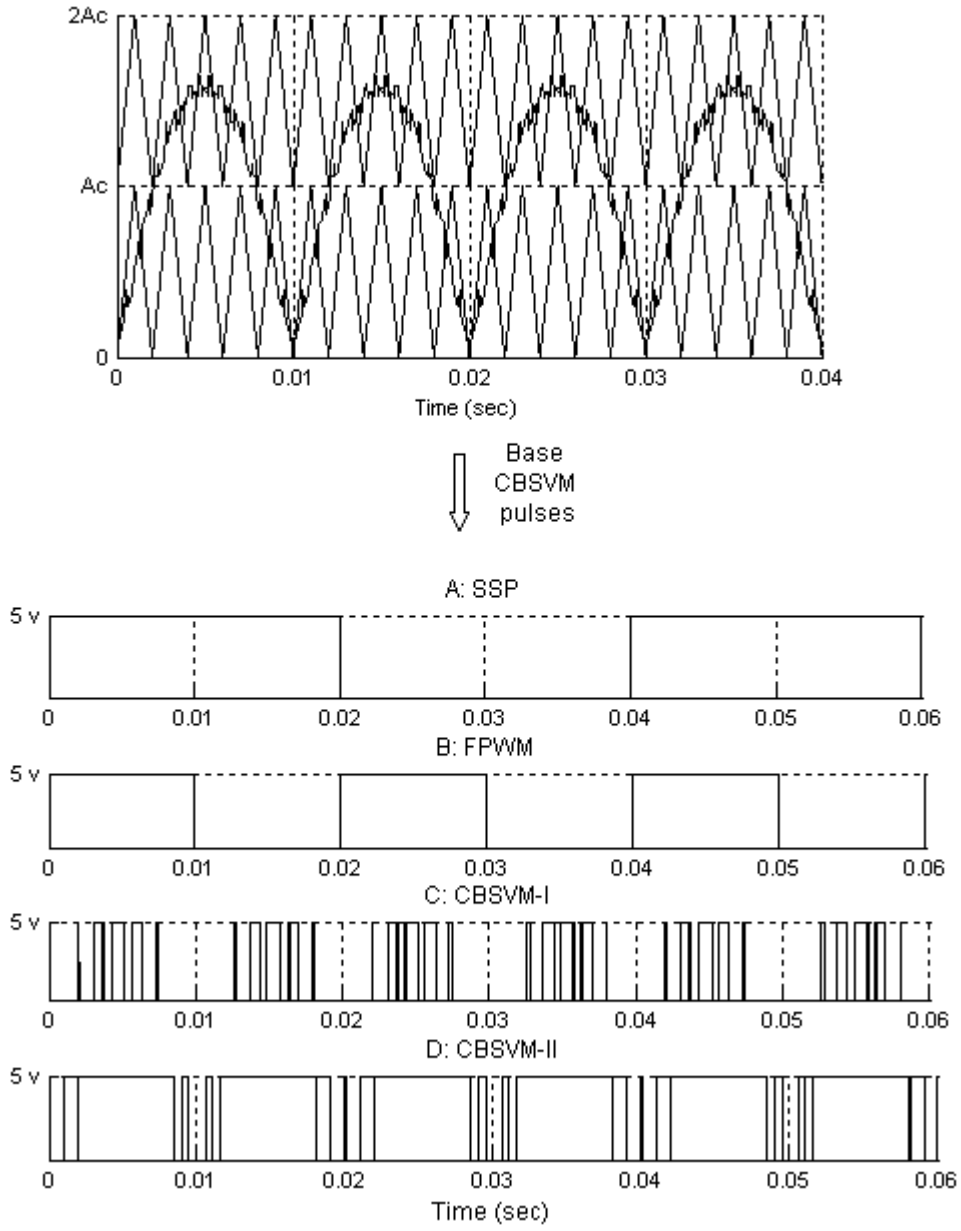


Figure 3.11 Five-level base CBSVM pulses

Base CBSVM pulses are periodically rotated using base MSPWM circulation scheme to get resultant HCBSVM circulation among the series connected inverter cells. Then, the base modulation pulses are combined using HMC to produce HCBSVM pulses for five-level inverter operation. The resultant HCBSVM is composed of both FFPWM and CBSVM pulses. The sequential signal makes every power switch operate under CBSVM and FFPWM sequentially to equalize the power losses among the switches. If the

SSP A=1, S1, S2, S1’ and S2’ are operated with CBSVM, while S3, S4, S3’, S4’ are operated with FFPWM. If the SSP A=0, S1, S2, S1’ and S2’ are operated with FFPWM, while S3, S4, S3’ and S4’ are operated with CBSVM. The principle of HCBSVM is also clarified in Figure 3.12, where the inverter modules alternately participate in HCBSVM circulation, and thus share the load evenly among each other.

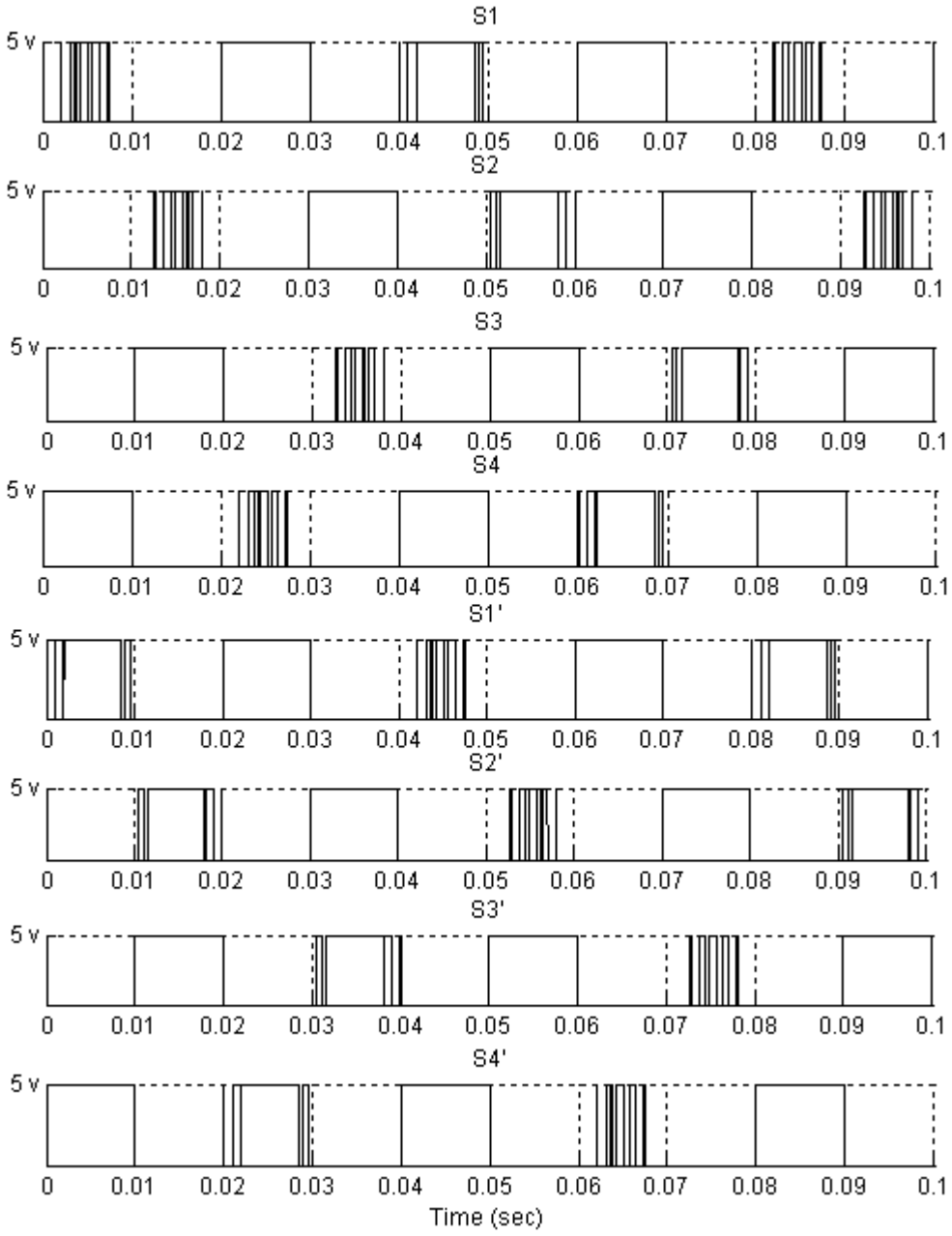


Figure 3.12 Five-level sequential switching HCBSVM pulse pattern

3.7 HYBRID PHASE SHIFTED CARRIER MODULATION

HPSC is the combination of FFPWM and PSC modulations. PSC modulation is well known for its important advantage of offering an increased bandwidth as the number of carriers multiplied with their frequency directly controls the location of the dominant harmonics. The scheme of HPSC modulation for a five-level inverter is shown in Figure 3.13. Base PSC consists of (N-1)/2 carriers with the frequency $f_c' = f_c/(N-1)$, where f_c is the switching frequency of the resulting PWM waveform. The carriers for five-level PSC-PWM is defined as

$$C_1^{'} = A_c \; y_c(f_c^{'}, 0) \tag{3.16}$$

$$C_2^{'} = A_c \; y_c(f_c^{'}, \pi/2) \tag{3.17}$$

where $f_c^{'} = f_c/4$ and A_c as peak to peak amplitude of the carrier. The carriers are shifted by $2\pi/(N-1)$ incrementally. The modulation and phase shifted carrier waveforms are shown in Figure 3.14(a).

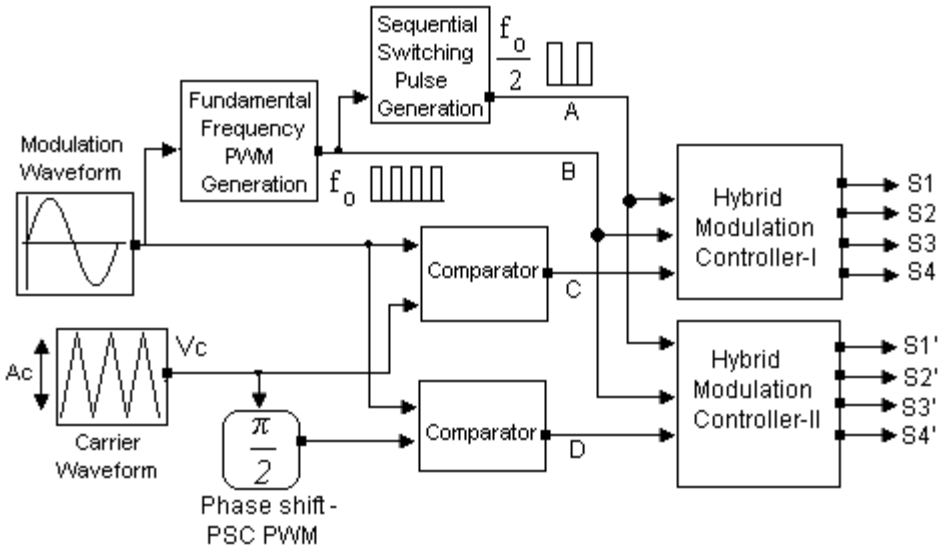


Figure 3.13 Scheme of hybrid phase shifted carrier modulation

The normalized triangular carrier y_c is mathematically defined as

$$y_c(f_c, \varphi) = (-1)^{[\theta]} ((\theta \bmod 2) - 1) + \frac{1}{2}, \tag{3.18}$$

$\theta = \frac{2\pi f_c t + \varphi}{\pi}$. where φ represents the phase angle of carrier.

Base PSC modulation pulses (C and D) are obtained by the comparison of modulation waveform with the corresponding phase shifted carrier for each inverter cell. SSP (A) is a square wave signal with a 50% duty ratio and half of the fundamental frequency. FFPWM (B) is a square wave signal synchronized with a modulation waveform; B=1 during the positive half cycle of the modulation signal, and B=0 during negative half cycle. SSP and FFPWM pulses are same for all inverter cells in each phase and should be synchronized with phase references. The base modulation pulses for HPSC are shown in Figure 3.14(b).

The function of HMC is to combine base PSC modulation pulses with FFPWM and produce HPSC modulation pulses. The resultant HPSC consists of both FFPWM and PSC modulation pulses. If SSP is active high, S_1 and S_2 in cell-I and S_1' and S_2' in cell-II are operated with PSC-PWM while S_3 and S_4 in cell-I and S_3', S_4' in cell-II are operated at FFPWM. If SSP is active low, S_1 and S_2 in cell-I and S_1' and S_2' in cell-II are operated at FFPWM while S_3 and S_4 in cell-I and S_3', S_4' in cell-II are operated with PSC-PWM. For HPSC modulation, base PWM circulation can be omitted because it has the feature of inherent balanced power distribution among the inverter cells.

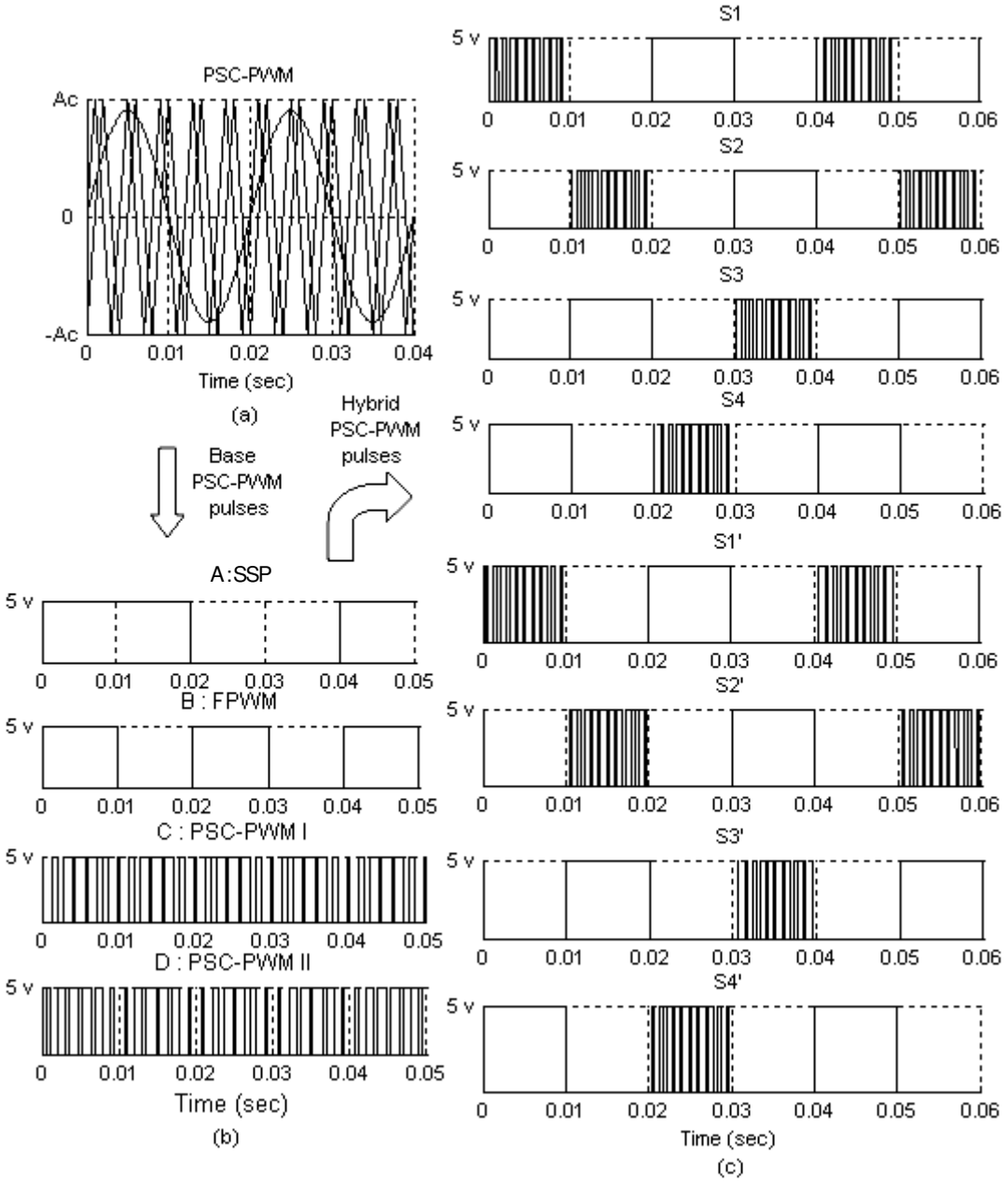


Figure 3.14 (a) Phase shifted carrier and modulation waveforms (b) Base modulation pulses (c) Five-level HPSC pulses

3.8 HARDWARE IMPLEMENTATION OF SSHSM CONTROLLER

The experimental setup is composed of a personal computer, Digital Signal Processor (DSP), Complex Programmable Logic Device (CPLD)

controller, Isolation and IGBT driver circuit, CMI power circuit, DC power supply, and Tektronix TPS2024 digital real time oscilloscope. The functional block diagram of SSHSM controller implementation for a five-level CMI is shown in Figure 3.15. In order to implement the SSHSM strategies and generate the SSHSM pulses to the appropriate switches, DSP-CPLD control platform is used. DSP controller mainly finished the control strategies for base PWM generation and output of base modulation pulses to CPLD. The CPLD controller is used to perform three main tasks namely base MSPWM circulation, sequential switching hybrid PWM formation and dead time control in the hybrid PWM pulses.

3.8.1 DSP Based Base PWM Generation

Texas Instruments TMS320F2407 DSP is a low cost high speed programmable digital controller with C2xx DSP central processing unit as the core processor used for base MSPWM generation. It offers 40 million instructions per second performance. The on-chip peripherals on the F2407 DSP processor make virtually for PWM generation. The peripherals are two event manager (A and B), General Purpose (GP) timers, PWM generators for digital control, analog to digital converter, Controller Area Network (CAN) interface, Serial Peripheral Interface (SPI), Serial Communication Interface (SCI), general purpose bi-directional digital I/O, and watch dog timer. Communication peripherals make possible the communication with personal computers and external peripherals. Code Composer Studio (CCS) is a user friendly windows based debugger for developing and debugging software for the F2407 DSP processor. CCS assembles and links the source files and creates a DSP compatible (*.out) file that will ultimately be loaded on to the DSP. The .out file contains the user program and also information as to where in program memory it will be placed.

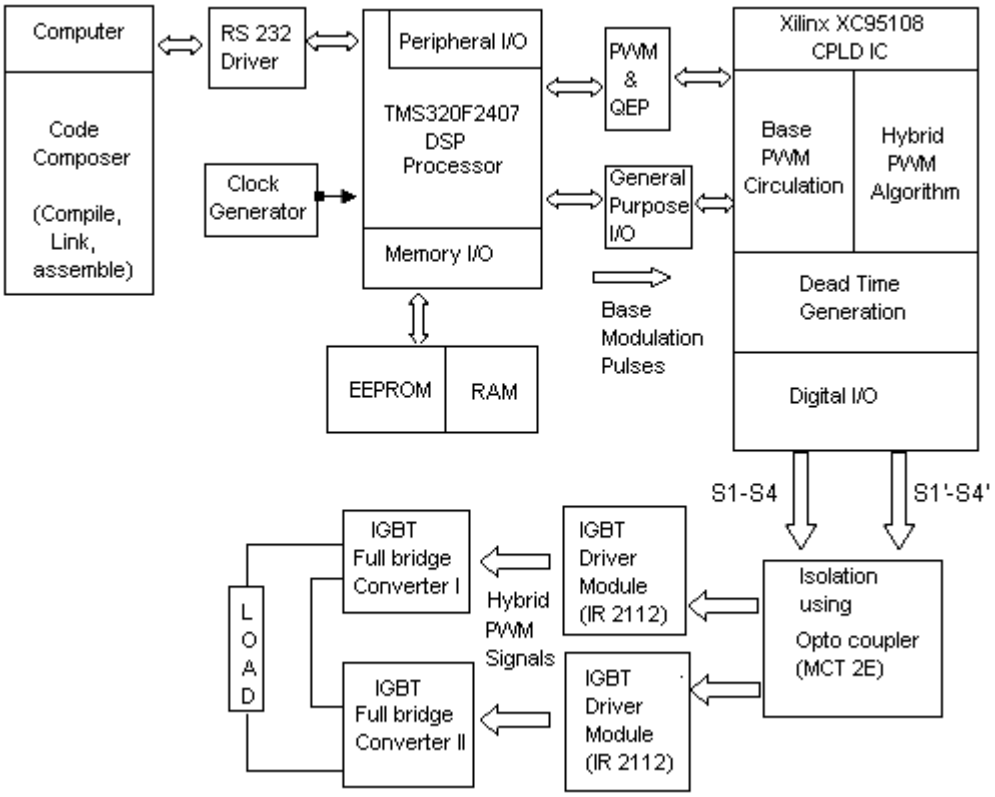


Figure 3.15 Experimental setup for SSHSM controller implementation for five-level inverter

Event manager modules of the DSP have the general purpose timer that can be used as time reference. Full compare and PWM units as a comparison mechanism and have dedicated digital PWM outputs. There are two GP timers in each event manager that can work independently from each other. GP Timer 1 and 2 are controlled by event manager A, GP Timer 3 and 4 are controlled by event manager B. Each GP Timer has updown counter TxCNT, compare register TxCMPR, period register TxPR, control register TxCON and direction input TDIRx registers.

In order to generate MSPWM pulses digitally, a timer is set to continuously repeat a counting period. The GP Timer period is selected based on the frequency of the carrier signal used for MSPWM generation. The initial value of the GP timer counter can be any value from 0000h to FFFFh.

The maximum count is initialized in accordance to the required switching frequency. The counting pattern of the timer is configured as continuous up/down counting mode for symmetric PWM generation. The compare register associated with GP timer stores the value that will be constantly compared with the current value of the timer counter. When a match occurs, the output toggles high to low, or low to high. The on and off time of the pulse is directly dependent on the value loaded in to the timer's compare register. By varying the number in the compare register by the modulation signal, a PWM signal that represents the modulating signal can be produced.

Due to the large amount of memory available, a complete sinusoidal cycle can be easily stored within the DSP, which minimizes the time taken to get the voltage reference value at every sampling instant. The up-down counting process undergoes an underflow, an interrupt is occurred. As a result, the control jumps to the PWM Interrupt Service Routine (ISR). At the end of the PWM ISR execution, the count content of the compare registers is upgraded based on modulation signal of MSPWM selected and the control returns back to the waiting loop. With continuous counting as soon as underflow occurs again, interrupt occurs and same procedure is repeated. In MSPWM, the phase references are generated in such a way that the frequency and magnitude of these references are the function of modulation index and fundamental frequency. Programming is done to generate the MPWMs such as APOD, SCSM, and PSC modulation pulses at different carrier frequency.

The digital implementation of the CBSVM consists of time critical tasks required for PWM generation. The time critical tasks are driven by the interrupts generated by event manager embedded in the DSP. The timers in the event manager are programmed to generate the interrupt at exactly half the carrier interval. Upon receipt of the interrupt, the processor executes the ISR. The ISR is written to determine the new modulation reference values and load

into the compare registers for comparison with the timers. The timers are programmed to count in up–down counting mode, which will generate the carrier signal for comparison with the stored values in the compare registers. The PWM signals are generated upon the comparison of these values with the timer counts. Once the new reference values are calculated, and loaded into the respective registers, the program comes out of the ISR and is free till next interrupt (after half the carrier period) arrives.

The PWM technique does not involve any sector identification and reduces the computation time considerably, when compared to conventional SVM technique. The multilevel CBSVM pulse generation provides linear transfer characteristics between fundamental component of output voltage and modulation index. The addition of offset to the reference phase voltage ensures that the modified reference voltages always remain within the carrier regions in the entire linear modulation range.

Structure of MSPWM modulator is very simple and requires only few mathematical operations in order to provide base modulation pulses. In CBSVM, the most time consuming operation is offset signal component calculation. The number of switching pulses per fundamental cycle that is decided by the maximum switching frequency. Also the other base modulation pulses such as FFPWM and SSP are generated. The base PWM pulses are transmitted to the CPLD controller through DSP SPI port which provides high speed data transmission between the two processors.

3.8.2 CPLD Based Hybrid Modulation Controller

In SSHSM controller implementation, the control algorithms are implemented in a Xilinx CPLD XC95108 IC. This controller can be operated with maximum PWM frequency up to 40 kHz with a duty cycle resolution of 1% and also this IC can be easily interfaced to DSP system. XC95108 IC is

used to develop the control algorithms which suited for this application that has the features of better response for high frequency input pulses, narrow pulse width pulses and no jitter of the delay in the circuit. The functional block diagram of control algorithm realization in CPLD controller is shown in Figure 3.16. The programming was done in the high speed IC hardware description language (VHDL); each functional block is an entity in VHDL.

CPLD controller is configured to receive the base modulation pulses such as FFPWM, SSP and MSPWM pulses. Base PWM pulses are loaded into the double-buffered register bank in the CPLD to be used for processing. The double-buffered register bank consists of timer registers and state registers, the numbers of which vary for different applications. Each register is double-buffered, so that the PWM data used in the current switching cycle is not affected by the asynchronous DSP.

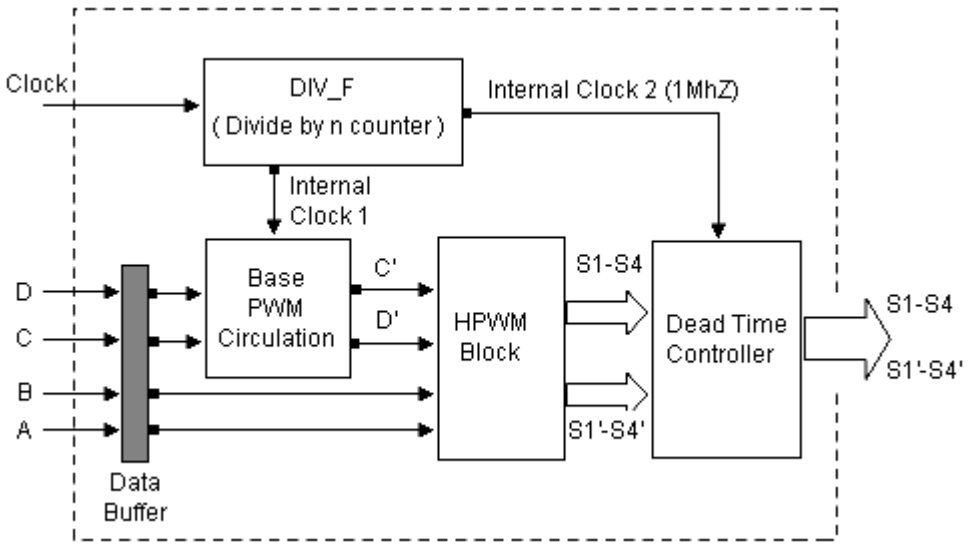


Figure 3.16 Functional block diagram of control algorithm realization in CPLD

The DIV_F block in CPLD controller generates the two internal clocks from the IC input clock. The internal clocks can be adjusted in the

range of 2-500 kHz. The external clock frequency is 40 MHz. PWM circulation block circulates MSPWMs periodically based on internal clock-I signal. This is implemented with multiplexers and modulo-K counters. The proposed HMC is based on a specially designed, combinational logic circuit. The HPWM block generates eight SSHSM pulses by combining FFPWM, SSP and two MSPWMs.

Dead-time protection is provided to avoid any shoot through the inverter legs. This is done by delaying the rising edges of all the SSHSM pulses by a particular number of clock cycles and then logical AND with respective PWM pulses. A switching dead time of 1μs is introduced in the CPLD hardware so that dead times fit into the transition edges of the trigger signals.

A software program was developed, for synthesizing the architecture using the Xilinx foundation software V3.1. The final design is converted in configuration data file and loaded into CPLD IC. The proposed architecture occupies only a small percentage of the corresponding device logic blocks, thus permitting the integration of additional control operation in the same IC. CPLD serves as a coprocessor, producing eight independent SSHSM pulses based on base PWM pulses. Due to hardware parallelism of CPLD, eight independent PWM pulses are synchronous.

3.8.3 Isolation and Driver Circuit

The optically coupled isolators (MCT2E) are used to provide an electrical isolation between the CPLD controller and the power circuit. IGBTs are voltage controlled devices and it requires a minimum gate threshold voltage (Vge(th)) of about 15V for establishing the rated collector to emitter conduction. This requirement makes it difficult to directly interface an IGBT to CPLD IC.

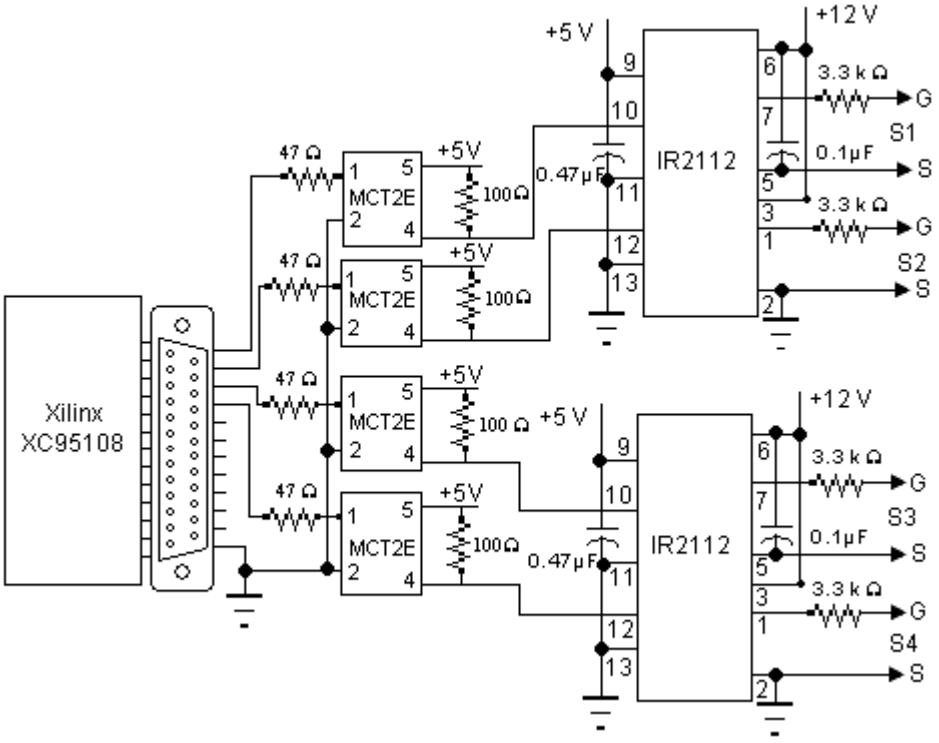


Figure 3.17 Isolation and driver circuit for one inverter cell

For proper operation of IGBTs, correct power levels are required (Vge(th)=15 V and Ig= 50 mA). Voltage and current levels of CPLD controller output signals fail to operate the IGBTs. IGBT driver circuit provides power gain for CPLD output pulses to the required level for triggering the IGBTs. Four high voltage high speed IGBT drivers (IR2112) are used to provide proper and conditioned gate pulses. The output waveform will have the same one as the input waveform except the magnitude and power. The gate drive IC's are powered with regulated +12V DC auxiliary power supply. It is MOS-gate driver, operates on the bootstrap mode.

3.8.4 CMI Power Circuit

A five-level CMI consists of two modules, each containing a structure of three phase diode rectifier, DC link capacitor and a FBI. The series connection of the inverter cells produce multilevel voltage, which

corresponds to the addition of the output voltage of each cell. Each inverter cell is made with four IGBT switches with internal anti-parallel diodes (IRG4PC40KD) from International Rectifier. The voltage and current ratings of the IGBTs are 1200 V and 25 A respectively. The DC link power is obtained through a three phase full-bridge diode rectifier. A 2200μF/500V aluminum electrolytic type capacitor is used as filter at the rectifier output and provides constant DC-link for inverter cell. The DC bus voltage is 200 V, with a current rating of 10 A.

The proposed SSHSM schemes such as HAPOD, HSCSM, HCBSVM and HPSC are presented in this chapter. The functional logic for HMC is introduced to develop SSHSM from MSPWM to get the dual performance of FFPWM and MSPWM. Base PWM circulation algorithm for five-level and N-level inverters, are proposed for DC link capacitor voltage balancing, and for balanced loading of the inverter cells. DSP-CPLD based digital controller is designed to implement the proposed modulations, and to show the effectiveness of SSHSM in a five-level CMI.