CHAPTER 1

INTRODUCTION

1.1 INTRODUCTION

The development of new series modulation techniques to improve some specific characteristics of multilevel inverters is focused in this thesis. So, in order to make the text understandable, it is necessary to make a brief overview of the most common multilevel inverter topologies introducing the used nomenclature and the operation basis of these types of inverters.

Multilevel Inverters (MI) are finding increased attention in industry and academia as one of the preferred choices of electronic power conversion for high-power applications. They have successfully made their way into the industry and therefore can be considered as a mature and proven technology. Although it is an enabling and already proven technology, MI presents a great deal of challenges, and even more importantly, they offer such a wide range of possibilities that their research and development is still growing in depth. Researchers all over the world are contributing further to improve energy efficiency, reliability, power density, simplicity, and cost of MI, and broaden their application field as they become more attractive and competitive.

1.2 MULTILEVEL INVERTER TOPOLOGIES OVERVIEW

Multilevel converters are power electronic conversion systems composed by an array of power semiconductors and capacitive voltage sources that, when properly connected and controlled, can generate a multiple step voltage waveform with variable and controllable frequency, phase, and

amplitude. It is an effective solution for increasing power and reducing harmonics of AC waveforms. The general idea of MI is to synthesize a sinusoidal voltage from several voltages of levels, typically obtained from capacitor voltage sources (Franquelo et al 2008). The number of levels of a converter can be defined as the number of steps or constant voltage values that can be generated by the converter between the output terminal and any arbitrary internal reference node within the converter. As the number of levels increases, the synthesized output waveform adds more steps, producing a staircase wave which approaches the sinusoidal wave with minimum harmonic distortion (Meynard et al 2002). When considering a three-phase system, the levels of one phase are combined with those of the other phases, generating more different levels in the line-to-line voltage.

The attractive features of a MI can be briefly summarized as follows (Rodriguez et al 2009) and (Rodriguez et al 2002).

The voltage stress on each switch is decreased due to series connection of the switches. Therefore, the rated voltage and consequently the total power of the inverter can be safely increased. This allows use of high performance devices available at low voltage rating. The rate of change of voltage (dv/dt) is decreased due to the lower voltage swing of each switching cycle.

Harmonic distortion is reduced due to more output voltage levels. Therefore, it increases the power quality: in this way, the AC side filter can be reduced, decreasing its costs and losses. Also, it can draw input current with low distortion. Lower acoustic noise and electromagnetic interference are obtained. It produces smaller common mode voltage; therefore, the stress in the bearings of a motor connected to a MI can be reduced. It operates at lower switching frequency usually means lower switching loss and higher efficiency.

The hardware cost can be dramatically reduced at high power level using the MI topologies instead of conventional two-level one. One of the dominant factors contributing to the decrease of cost is the low power rating devices. Furthermore, MI can be directly connected to high voltage sources without using transformers; this means a reduction of implementation cost. The power devices do not encounter any voltage sharing problem. For this reason, MI can easily be applied for high power applications such as large motor drives and utility supplies.

Higher the numbers of levels better the quality of output voltage which is generated by a greater number of steps with a better approximation of a sinusoidal wave. So, increasing the number of levels gives a benefit to the harmonic reduction of the generated voltage, but a more complex control system is required due to greater number of power semiconductor switches with gate drive circuit.

Although there are a large number of MI topologies in the literature, the most common topologies are presented in this chapter. Nowadays, there exist three commercial topologies: Diode Clamped Multilevel Inverter (DCMI) or Neutral Point Clamped (NPC) inverter, Cascaded Multilevel Inverter (CMI), and Flying Capacitors Multilevel Inverter (FCMI). These converters are commercialized by several manufacturers in the field (Wen and Smedley 2008), offering different power ratings, front-end configurations, cooling systems, semiconductor devices, and control schemes, among other technical specifications. Several surveys of MI have been published to present these topologies (Fazel et al 2007). Among these inverter topologies, CMI reaches the higher output voltage and power levels (13.8 kV, 30 MVA) and the higher reliability due to its modular topology (Rodriguez et al 2007).

1.2.1 Diode Clamped Multilevel Inverter

A DCMI consists of N-1 capacitors on the DC bus and produces N-levels on the phase voltage. The DC bus voltage is split into many steps by capacitor banks. In this way, no extra DC sources are needed with respect to the standard two-level inverter. The clamping diodes are to clamp the voltage between two switches (Bruckner et al 2005). Figure 1.1 (a) shows a five-level diode clamped inverter in which the DC bus consists of four capacitors C_1, C_2, C_3, and C_4. There are five switch combinations to synthesize five-level output voltage across a and n.

- For voltage level V_{an}=V/2, turn on all upper switches S_1-S_4.
- For voltage level V_{an}=V/4, turn on three upper switches S_2-S_4 and one lower switch S_1'.
- For voltage level V_{an}=0, turn on two upper switches S_3 and S_4 and two lower switches S_1' and S_2'.
- For voltage level V_{an}= -V/4, turn on one upper switch S_4 and three lower switches S_1'-S_3'.
- For voltage level V_{an}= -V/2, turn on all lower switches S_1'-S_4'.

An N-level inverter leg requires (N-1) capacitors, 2(N-1) power devices and (N-1)(N-2) clamping diodes (Busquets-Monge et al 2008). DCMI presents some peculiarities which other topologies do not have. First of all, it is quite simple to control. Indeed, a simple extension of a traditional analog Pulse Width Modulation (PWM) control can directly gate the switches without any switching table in between. It is quite easy to implement a digital control system over a diode-clamped with commercial parts only, using some external hardware and designing a proper code (Cheng and Wu 2007). It is definitely more suitable for back-to-back regenerative applications.

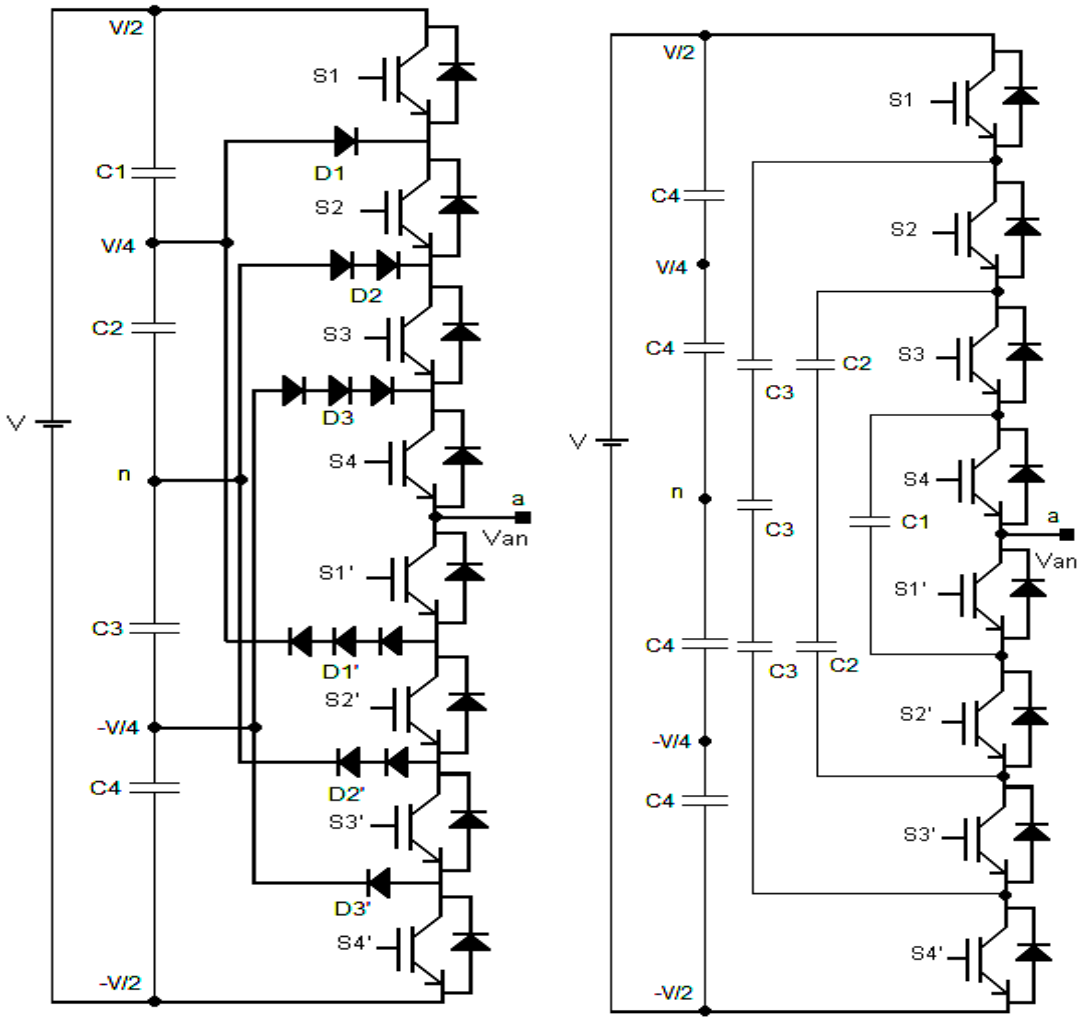


Figure 1.1 **Classic multilevel inverter topologies (one phase leg) (a) five-level diode clamped inverter (b) five-level flying capacitor inverter (c) output voltage waveform.**

Despite all the advantages mentioned, the DCMI has a characteristic which usually limits the use of such structure with more than five levels. Although each active switching device is only required to block a voltage of $\frac{V}{N-1}$, where N is the number of levels, the necessary reverse voltage blocking capability of the clamping diodes is proportional to the level for which they are used to employ clamping action.

As a result, series connection of diodes is required, which complicates the design and raises reliability and cost concerns. Anyway this can be avoided using a series of more diodes or a different kind of rating for a greater reverse voltage.

This fact, together with the increasing difficulty to control the DC-link capacitor unbalance, has kept the industrial acceptance of the NPC topology up to three levels only. A very serious problem regards the mean current through the switches is different. Therefore the inverter design uses different current ratings for the switching devices. Choosing different kind of switches with the same reverse voltage and similar dynamic characteristics is quite difficult among commercial parts. DCMI does not require isolated DC sources to create the voltage level, but exploits several capacitors to equally split a single DC source. But, unbalance of capacitors voltage between different levels can take place and the control must keep it into consideration. Furthermore, this converter is connected in a back-to-back configuration, a proper synchronization between inverter and rectifier controls is sufficient to keep the capacitors balanced.

1.2.2 Flying Capacitor Multilevel Inverter

An alternative topology, called FCMI, which basically replaces the clamping diodes by flying capacitors, was proposed by Meynard and Foch.

The voltage synthesis in a FCMI has more flexibility than a DCMI. Using Figure 1.1 (b), the five-level output phase voltage with respect to neutral point n, Van, can be synthesized by the following switch combinations.

- For voltage level V_{an}=V/2, turn on all upper switches S_1-S_4.
- For voltage level V_{an}=V/4, there are three combinations in which switches are turned on: S_1, S_2, S_3, S_4'; S_2, S_3, S_4, S_4'; S_1, S_3, S_3', S_4
- For voltage level V_{an}=0, there are six combinations: S_1, S_2, S_1', S_2'; S_3', S_3, S_4, S_4'; S_1, S_3, S_3', S_1'; S_1, S_4, S_3', S_2'; S_2', S_2, S_4, S_4'; S_2, S_3, S_4', S_1'.
- For voltage level V_{an}= -V/4, there are three combinations in which switches are turned on: S_1, S_1', S_2', S_3'; S4, S_2', S_3', S_4'; S_1', S_3', S_3, S_4'.
- For voltage level V_{an}= -V/2, turn on all lower switches S_1'-S_4'.

An N-level inverter leg requires (N-1) (N-2)/2 auxiliary capacitors per phase in addition to (N-1) DC bus capacitors (Krug et al 2007). Here the load cannot be directly connected to the neutral of the converter to generate the zero voltage level. Instead, the zero level is obtained by connecting the load to the positive or negative of DC supply through the flying capacitor with opposite polarity respect to the DC-link. The important peculiarity of this converter is the high portability. Indeed the flying capacitor can substitute a standard two-level converter even more easily than the diode-clamped because the DC bus capacitor is still present and correctly rated, so there is no need to change it. Both real and reactive power can be controlled in this inverter.

It naturally creates a degree of freedom to balance the flying capacitor by using redundant states where the same output voltage level can

be achieved by two or more switching combinations. However, the flying capacitors are submitted to different voltage levels, similar to the blocking requirements of the clamping diodes. In a three-level converter, there is only one capacitor to keep balanced and the implementation of the control algorithm is quite easy. When the number of level rises, the voltages to keep controlled increase a greater number of voltage sensors and a more complicated control are needed. Even for this topology, the switch average currents could be different because they strictly depend on the control choice of redundant states. Some estimations of this value can be done, but is difficult to rate each switch for the exact current value.

Converter initialization is an another problem, in which clamping capacitors must be setup with required voltage levels that complicates modulation process and hinders the performance under ride-through conditions. Furthermore, for low switching frequency, the clamping capacitors become large in size thus decreasing the power density of the inverter. Although the topology is modular in structure and can be increased in an arbitrary number of levels, the additional flying capacitors and the involved costs has kept traditional configurations up to about four levels. In addition, more cells do not necessarily signify an increase of the power rating of the converter, since the output voltage amplitude does not vary only the number of levels, hence the power quality.

1.2.3 Cascaded Multilevel Inverter

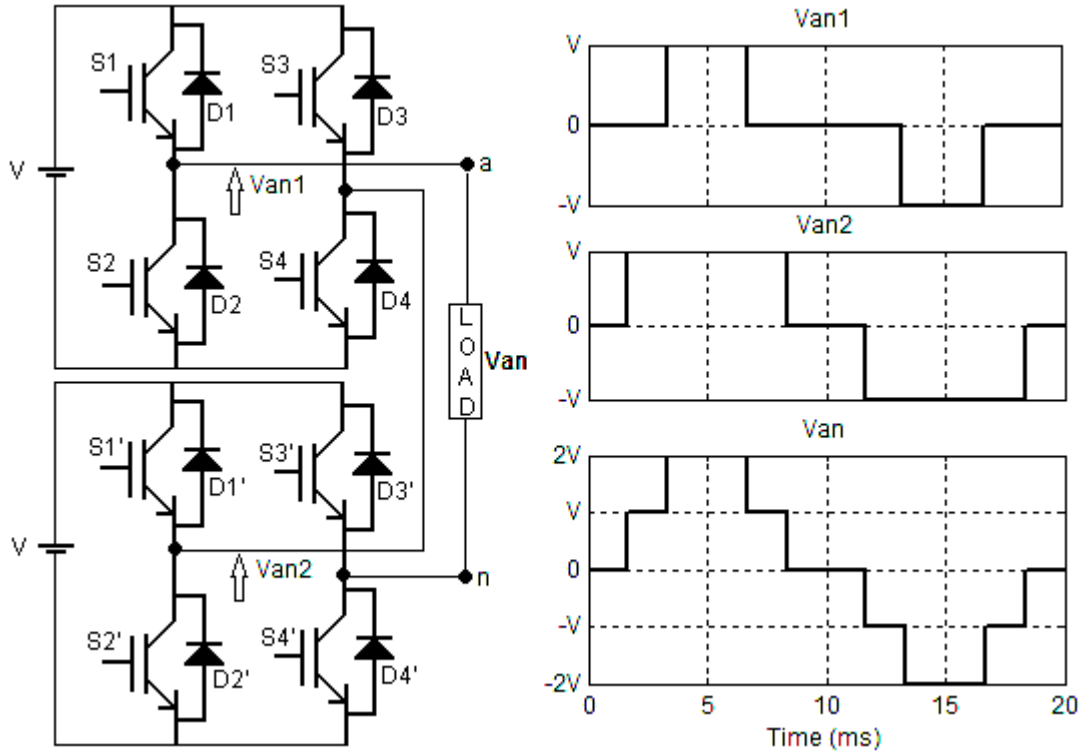
In order to eliminate extra clamping elements (diodes and capacitors) and avoid inherent problems caused by voltage imbalance, the CMI has been introduced. CMI is the series connection of two or more single phase Full Bridge Inverters (FBI) with separate DC sources. When two or more FBI is connected in series, their output voltages can be combined to form different output levels, increasing the total inverter output voltage and also its rated power. This structure is capable of reaching medium output

voltage levels using only standard low-voltage mature technology components. Typically, it is necessary to connect three to ten inverters in series to reach the required output voltage (Kou et al 2006).

The number of levels is proportional to the number of isolated FBI cells according to the expression N = 2K + 1, where K is the number of FBI per phase. In addition, the number of steps (Q) in the line voltage is Q=2N-1. The connection of a cell in each phase adds two more levels to the phase voltage and four more levels in the line voltage. An increase in the number of steps in the output voltage produces a reduction in harmonic distortion. A five-level CMI consists of two individual cells; each containing its own FBI is shown in Figure 1.2 (a). Each FBI uses a DC-link voltage to generate a modulated voltage at the output terminals.

CMI presents more redundancies than the previous topologies, since each FBI or power cell has one redundant switching state, and the series connection inherently introduces more redundancies. The number of redundancies grows over proportionally when increasing the number of cells. These redundancies and the natural modularity of this topology are advantages that enable fault-tolerant operation.

Each inverter requires an isolated DC voltage which is usually obtained by an arrangement of three-phase or single-phase rectifiers, and a multi-pulse transformer which provides the electrical isolation. In some applications, these DC voltages can be obtained directly by isolated DC sources, for example, photovoltaic panels or DC to DC isolated converters. In another application, like static compensator (STATCOM), which does not require, the injection of active power, the DC link voltages can be floating, and the control strategy keeps the DC-link voltage adjusted to the reference.



(a) **(b)**

Figure 1.2 (a) Schematic diagram of the five-level cascaded multilevel inverter (b) Output voltage waveform

The resulting phase voltage is synthesized by the addition of voltages generated by the different cells. As Figure 1.2(b) illustrates, each of the FBI active devices switching only at the fundamental frequency, the resultant output voltage (V_{an}) is the sum of single cell output voltages for an inverter composed by K cells.

$$V_{an} = \sum_{j=1}^{K} V_{anj} \tag{1.1}$$

where j=1, 2, …, K.

For each FBI, the output voltage and input DC current is given by Equations (1.2) and (1.3) respectively.

$$V_{anj} = V(S_{1j} - S_{3j}) \tag{1.2}$$

$$I_{dcj} = I_a(S_{1j} - S_{3j}) \tag{1.3}$$

where I_a is the output current of the CMI and S_{1j} and S_{3j} are the upper switch of each FBI.

For N-level inverter requires (N-1)/2 separate DC sources and (N-1)/2 power devices. Unlike the diode-clamp or flying capacitor inverters, the CMI does not require any voltage clamping diodes or voltage balancing capacitors. Each FBI can generate three different voltage outputs, +V, 0, and –V, by connecting the DC source to the AC output side by different combinations of four switches. High and low couple of switches can be defined in the respect of voltage output direction. Considering Figure 1.2, the couple of switches composed by S_1 and S_4 are the high one, whereas S_1' and S_4' constitute the low couple. The high output of one cell is shortcut to the low output of another one to realize a cascade connection between two cells.

Each cell in the cascade connection adds two levels more to the output waveform as Table 1.1 shows for a five-level inverter leg. Some switch configurations are harmful for the converter and they must be avoided; for instance, the switches S_1 and S_2 are not allowed to be turned on at the same time because this situation causes a shortcut of the source. There are many possible switch combinations that can synthesis stair case waveform for CMI. The number of switch combinations is proportional with the inverter level (N). The relationship between the number of switch combinations and the inverter level is expressed by Equation (1.4).

$$\text{Number of switch combinations} = 2^{N-1} \quad (1.4)$$

For example, the number of switch combinations for five-level inverter is 16. Hence, the flexibility in voltage synthesizing for this topology is more than DCMI and FCMI.

Table 1.1 Switch status and output voltages of a five-level cascaded multilevel inverter

Switch Status (ON)	Output voltage (V_{an})	State
S_1-S_4-S_1'-S_4'	2V	+2
S_1-S_3-S_1'-S_4'	V	+1
S_1-S_4-S_2'-S_4'		
S_1-S_4-S_1'-S_3'		
S_2-S_4-S_1'-S_4'		
S_1-S_3-S_1'-S_3'	0	0
S_1-S_3-S_2'-S_4'		
S_1-S_4-S_2'-S_3'		
S_2-S_3-S_1'-S_4'		
S_2-S_4-S_1'-S_3'		
S_2-S_4-S_2'-S_4'		
S_2-S_3-S_1'-S_3'	-V	-1
S_2-S_4-S_2'-S_3'		
S_2-S_3-S_2'-S_4'		
S_1-S_3-S_2'-S_3'		
S_2-S_3-S_2'-S_3'	-2V	-2

A particular advantage of this topology is that the modulation, control and protection requirements of FBI are modular. A modular design of medium-voltage converters is an important requirement, which enables a platform based on development, manufacturing, and service of converter

systems. Therefore, in the case of a fault in one of these modules, it is possible to replace it quickly and easily. Moreover, with an appropriate control strategy, it is possible to bypass the faulty module without stopping the load, bringing an almost continuous overall availability. It has inherent capacitor voltage balancing and balanced average power flow through each cell with proper modulation (Lezana et al 2008).

Compared with the DCMI and FCMI inverters, it requires the least number of components to achieve the same number of voltage levels and consequently requires the lowest implementation cost. Also, extra clamping elements are not necessary. Moreover, it provides the flexibility for expansion for a higher number of levels. Optimized circuit layout and packing are possible because each level has the same structure. In these converters, lower average device switching frequencies are possible for the same output voltage waveform quality. Therefore, air cooling and higher fundamental output frequency can be achieved without derating and without use of an output filter.

It is the one that has no unbalance problems since each DC-link is fed by an isolated DC source. However, for STATCOM, active filters, and other applications in which the capacitors are floating, a voltage control algorithm is necessary to keep the voltages controlled at the desired level.

1.2.4 Multilevel Inverter Driven Applications

Multilevel inverters are considered today as a very attractive solution for medium-voltage high-power applications. In fact, several major manufacturers commercialize NPC, FCMI, or CMI topologies with a wide variety of control methods; each one strongly depends on the application. Particularly, the NPC has found an important market in more conventional high-power AC motor drive applications like conveyors, pumps, fans, and

mills, among others, which offer solutions for industries including oil and gas, metals, power, mining, water, marine, and chemistry (Klug and Klaassen 2005), (Bernet 2006). The back-to-back configuration for regenerative applications has also been a major plus of this topology, used, for example, in regenerative conveyors for the mining industry (Rodríguez et al 2002b) or grid interfacing of renewable energy sources like wind power (Alepuz et al 2006), (Portillo et al 2006). On the other hand, FCMI have found particular applications for high bandwidth and high switching frequency applications such as medium-voltage traction drives.

Finally the CMI has been successfully commercialized for very high-power and power-quality demanding applications up to a range of 31 MVA, due to its series expansion capability. One of the best suited applications for CMI is the power quality devices, like STATCOM and Unified Power Flow Controllers (UPFC). Also, it has been used as a part of a power-quality compensator to reduce harmonics, reactive power, negative sequence, and the volatility of the load (Dixon et al 2005). This topology has also been reported for electric and hybrid vehicles (Tolbert et al 2002), photovoltaic power conversion (Rahiman et al 2004), (Naik and Udaya 2005), uninterruptible power supplies (Hua et al 2006), magnetic resonance imaging (Sabate et al 2004), high speed railway traction, hydro-pumped storage and large conveyor drive systems.

Although the choice of the MI topology is directly linked to the application and the list of specifications, in order to minimize losses, volume and costs, usually the number of components plays the most important role. Among the various MI structures are reported in the literature; the CMI appears to be superior for higher level structures. In this thesis, the topology of the CMI is chosen for investigation because of its attractive feature of modularity over the other two main topologies. In brief, the heart of any MI is

the selection of the power circuit topology and its associated switching strategy. The power circuit topology is dictated by a particular application and the nature of the DC supply that feed the inverter. The switching strategy will determine the harmonic performance of the output voltage waveform.

1.3 THESIS ORGANIZATION

This thesis reports the results of research work carried out by the author during the years 2007–2010. The research focused on MI modulation, with a special reference to a CMI. The outline of the thesis is as follows.

In Chapter 1, the standard MI topologies are described with its features in the literature. A power circuit for CMI used to verify the modulation methods is introduced. Also, the MC driven applications are pointed out. The outline of the thesis is also given. The author's contribution to this thesis is reported at the end of the chapter.

In Chapter 2, the background of the research is presented through detailed literature survey. The existing modulation techniques for CMI related to switching loss reduction, harmonic performance improvements, DC-link capacitor voltage balancing and power sharing issues are concentrated here. Selected simulation results for Multilevel Sinusoidal Pulse Width Modulation (MSPWM) are presented for comparative analysis.

Chapter 3 presents Sequential Switching Hybrid Sinusoidal Modulation (SSHSM) techniques for CMI operation. A design of hybrid modulation controller using a combinational logic is presented. A scheme of base MSPWM circulation is also introduced to get SSHSM circulation among the inverter cells. A series of Hybrid Alternate Phase Opposition Disposition (HAPOD), Hybrid Phase Shifted Carrier (HPSC), Hybrid Carrier Based Space Vector Modulation (HCBSVM) and Hybrid Single Carrier Sinusoidal

Modulations (HSCSM) are developed from standard MSPWM modulations, that aims at switching loss reduction with its own MSPWM advantages. The hardware implementation of SSHSM controller on DSP-CPLD control platform is presented at the end the chapter.

Simulation and experimental measures are discussed in the chapter 4 to show the feasibility of proposed modulations. Also, results include the analysis of the switching loss, power loss, heat-sink temperature rise, the effects of SSHSM circulation on DC-link capacitor voltages, and comparative harmonics analyses of different modulation schemes are presented.

The generalization of SSHSM for higher level inverter operation is presented in chapter 5, the corresponding results are given. Chapter 6 describes the extension of SSHSM for multiphase inverter operations. In Chapter 7, a summary of the modulation schemes, results, and the analyses are given.

1.4 SCIENTIFIC CONTRIBUTIONS

A sequential switching hybrid modulation controller for CMI is designed to combine Fundamental Frequency PWM (FFPWM) and MSPWM, so that the resultant PWM posses the hybrid characteristics. This sequential switching scheme solves the problem of differential heating among the power devices due to unequal switching losses. In addition, base MSPWM circulation scheme is also embedded, the formulation of SSHSM circulation in such a way that the inverter cells are equally loaded, and the balance of the individual DC link voltages is maintained throughout voltage region. These control algorithms are simple and low computational cost.

A new series of SSHSM modulation methods such as HAPOD, HSCSM, HCBSVM, and HPSC are developed from well known MSPWM to

make superior harmonic performance with reduced switching frequency. Hardware realization of SSHSM modulations are accomplished in DSP-CPLD digital control platform. It needs a little modification when the inverter level increases.

A complete set of analytical equations are derived from the device switching characteristics for switching and conduction loss estimation. Switching loss, power loss and thermal analysis with these proposed modulations are examined to show the features of switching loss reduction and thermal equalization. The harmonic spectrum studies on inverter output voltage and current waveforms, DC current ripple are also investigated.

A generalized procedure for the proposed SSHSM schemes is presented for higher level inverter operation and the corresponding results are illustrated. Also, these modulation algorithms are extended for multiphase multilevel inverter operations and its feasibility is verified.