CHAPTER 7

CONCLUSIONS AND FUTURE WORK

7.1 CONCLUSION

Sequential switching hybrid sinusoidal modulation techniques for cascaded multilevel inverters are investigated in this thesis, which provides a unique integrated solutions, high power quality and minimum switching losses. A new family of SSHSM techniques such as HAPOD, HPSC, HSCSM and HCBSVM were investigated. The main features of these modulations are to operate with lower switching frequency while retaining the leading advantages of MSPWM. All these methods are aimed at multilevel output voltage generation applicable in high-power converters.

With the popularity they gained as easy alternatives for high power apparatus in industry, multilevel inverters demand the development of more feasible topologies and control techniques. A few such topologies like diode clamped, flying capacitor, and cascaded multilevel inverters and their applications were discussed. One of these topologies, CMI is concentrated in this thesis.

The existing modulation techniques for CMI in the field of power loss reduction, harmonic performance improvement and power sharing issues have been reviewed. MSPWM modulation schemes were revewed, and some simulation results were presented for comparative reasons. MSPWM are easier in the sense of practical implementation as the switching transitions are

directly controlled by the comparison of signals which can be easily varied to control the modulation index.

Hybrid modulation is the combination of FFPWM and MSPWM. The resultant modulations inherit the features of switching loss reduction from FFPWM, and good harmonic performance from MSPWM. A computationally efficient hybrid modulation and MSPWM circulation algorithms, based on a simple combinational logic is proposed. These algorithms are also applicable for all MSPWM schemes used for SSHSM generation. The principle of all proposed modulators with sequential switching and SSHSM circulation schemes were shown in block diagrams. The modulated waves of SVM are transformed into CBSVM by adding proper offset voltages, for development of HCBSVM to get SVM performance with reduced switching frequency. This scheme reserves the advantages of multilevel SVM and can be easily realized.

A sequential switching scheme solves the problem of differential switching loss and therefore differential heating among the power devices. Also, it has inherent feature of reduced, equal voltage and current stress among the power switches, which makes the reliable inverter operation. A base MSPWM circulation scheme was embedded with these modulations for SSHSM circulation for the phase circuit of the CMI. The method aims at sharing the load evenly among the modules, even power dissipation and the voltage in the DC links remains in balance. It was shown that the method is effective, and most of all, implementable. These techniques establish the effectiveness in reducing DC current ripple as well as equal RMS ripple current among the inverter cells. Also, the average DC current loading of all inverter cells is the same. The reduced ripple current means less capacitance than for normal MSPWM.

The mathematical models of power semiconductor devices were presented to estimate the switching and conduction losses when SSHSM strategy is used. The analytical method is used to estimate the losses with consideration of modulation index, load power factor, switching frequency, and on-state ratio of the conducting device. It is observed that the proposed modulations leads to a significant reduction in switching loss over MSPWM in the entire range of fundamental power factor and also at any given modulation index.

Operation of the investigated modulation methods in the linear and over-modulation regions were performed to show the capability of the total utilization of the inverters. The harmonic analysis of the resulting voltage and current waveforms in entire operating regions was performed and compared, and the advantages of the proposed methods have been discussed.

To further validate the effectiveness of the proposed schemes, experimental analyses were performed on a DSP-CPLD based digital control five-level CMI. A low cost digital signal processor was used for generation of base modulation pulses. The architecture for sequential switching hybrid modulation, base MSPWM circulation and dead time control algorithms has been developed and tested using a single chip Xilinx XC95108 CPLD IC and generates SSHSM pulses for the inverter switches. All the software parts have been designed and built in such a way that they are easily expandable for higher level and multiphase inverters.

The experimental measures show that the proposed SSHSM schemes are effective in producing quality voltage and current waveforms, which is in agreement with the results obtained in the simulation studies. Furthermore, it is demonstrated that the proposed schemes achieve low switching frequency. Also, influence of sequential switching and SSHSM

circulation schemes on thermal equalization were analyzed based on experimental measures on power loss and heat sink temperature rise.

The control strategies have no restriction on the inverter level. It has been shown that the proposed modulation principles can be easily extended to higher level inverter operation in a straight forward manner. A generalized procedure was presented for designing SSHSM techniques for multiphase inverter operation. Detailed considerations were also given for five-phase CMI operation.

With SSHSM techniques, reduced switching losses, wide voltage linearity range, and high waveform quality could be obtained in a wide operating range. Considering that temperature rise and voltage stress are the main factors that decrease semiconductors life time, it is expected that higher efficiency and equal voltage stress among the power devices can contribute to increase inverter reliability. Also, these techniques could help to reduce the size of heat sink, thereby aiding design of compact power converters. In addition, these methods are simple and suitable for real time implementation due to its low computational cost, and useful for direct implementation in the existing CMI structures.

As a result, the thesis contributes the development of control methods for cascaded multilevel inverter yielding improved inverter utilization, reduced switching losses, lower harmonic distortion, DC link capacitor voltage balancing, balanced power dissipation and equal loading.

7.2 FUTURE WORK

The following research is suggested for sequential switching hybrid sinusoidal modulation techniques as a continuation of this research. These

modulations can be modified for the operation of other popular MI topologies such as DCMI and FCMI; useful findings are also to be obtained.

Investigations of these modulation strategies with adjustable speed drive systems have been carried out to reduce switching and harmonic losses, and also to reduce voltage and thermal stresses.

Investigations have to be made with SSHSM based STATCOM systems to improve the efficiency and to eliminate additional hardware for DC link capacitor voltage balancing.