Chapter 4

General Overview of Synapse Modeling
4.1 Introduction:

Modeling and simulation of the electrical activity of neuron including the synapse provides important tools for characterization and prediction of neuronal function. Such model has important applications in the field of neurobioengineering for simulation of receptor function and electrical activity of the postsynaptic cell. In the field of neuromorphology, such model may be used for simulation of agonist-receptor function of postsynaptic cell.

The electrical mechanism of synapse is shown in Fig. 4.1(a). The synaptic equivalent circuit is shown in Fig. 4.1(b), where $I$ is the total current from ionic channels of all synapses and $E_1, E_2, \ldots, E_M$ represent the chemical potentials of each corresponding ions. For example, $E_M$ may be $E_{Na}$ or may be $E_{Cl}$. The total current $I$ help to stimulate the postsynaptic neuron to initiate an action potential [1].

Fig. 4.1(c) shows the equivalent circuit of a synapse which consists of a presynaptic neuron, synaptic cleft and postsynaptic neuron. Here, $C_M$ represents the capacitance of the lipid bilayer of postsynaptic membrane. The conductance $g_{Na}$, $g_K$, $g_{Cl}$, and $g_o$ represent the membrane permeability of Sodium, Potassium, Chloride and other ions. $E_{Na}$, $E_{Cl}$, and $E_K$ are the chemical potentials of Sodium, Chloride and Potassium. $E_o$ is the resting potential.

From the Fig. 4.1(b), the total current can be written as

$$I = I_m + I_o - I_{Na} + I_{Cl} + I_K$$

(4.1)
If $V_m$ be the postsynaptic membrane potential established by the ionic and capacitive membrane current then

$$I = C\left(\frac{dV_m}{dt}\right) + g_0(V_m - E_0) - g_{Na}(V_m - E_{Na}) + g_{Cl}(V_m - E_{Cl}) + g_K(V_m - E_K)$$  \hspace{1cm} (4.2)
Fig. 4.1(b): Equivalent circuit of a presynaptic neuron

Fig. 4.1(c): Electrical equivalent circuit of synapse
4.2 Synaptic Neuron Models:

Modeling and simulation of neuron provides important tools for prediction of function of neurons at excitatory and inhibitory states. Such model has important applications in the field of neurobioengineering for simulation of receptor binding function and electrical activity of the postsynaptic cell. It is stated in literature [2] that FET is the ideal electronic element to simulate the axon membrane conductances. Theory of Metal-oxide Semiconductor Field-Effect Transistor (MOSFET) is therefore essential to understand the synaptic neuron model.

4.2.1 Theory of Metal-oxide Semiconductor Field-Effect Transistor (MOSFET):

The basic structure of Metal Oxide Semiconductor Field Effect Transistor (MOSFET) is shown in Fig. 4.2. MOSFET is a Metal Oxide Semiconductor (MOS) capacitor that has been made between two $n^+$ (i.e., heavily doped $n$-type) contact regions in a $p$-type semiconductor. The gate ($G$) (or MOS capacitor electrode) has a length $L$ and a width $Z$, as shown in Fig. 4.2.
The $n^+$ regions are called the source ($S$) and drain ($D$) regions. Their main function is to establish a low-resistance contact to the two ends of the $n^+$-type inversion layer, and a very high resistance contact to the $p$-type semiconductor substrate. Indeed the $n^+$ regions can supply electrons to the inversion layer, as is required there for conduction, but they can not supply holes to the $p$-type substrate, so they are a very poor ohmic contact to the substrate. They form $pn$ junctions with the substrate, with the polarity of bias between the source and drain regions and the substrate being such as to inhibit current flow (actually a leakage current will flow across the $n^+p$ junction at the drain, but it is very small, so the source and drain are effectively isolated when there is no inversion layer connecting them). In practice, only a negligible current can flow between the two $n^+$ regions unless a surface inversion layer is formed. This implies that current flows between source and drain only when we apply
a voltage between gate and substrate that is greater than the threshold voltage for the MOS capacitor.

The device shown in Fig. 4.2 is called an *n-channel enhancement-mode* MOSFET: a *p-channel enhancement-mode* MOSFET can be made by using $p^+$ contact regions in an $n$-type semiconductor substrate. The array of possible MOSFETs is indicated in Fig. 4.3, with the arrow indicating the direction from $p$-type to $n$-type.

*Fig. 4.3(a)(i) : Enhancement mode MOSFET structure and Circuit symbol (n-channel)*
Fig. 4.3(a)(ii) : Enhancement mode MOSFET structure and Circuit symbol (p-channel)
Fig. 4.3(b)(i): Depletion mode MOSFET structure and Circuit symbol (n-channel)
Fig. 4.3(b)(ii) : Depletion mode MOSFET structure and Circuit symbol (p-channel)
The line connecting the source and drain is continuous for depletion mode devices (channel exists for zero gate-source bias) and discontinuous for enhancement-mode devices (channel does not exist for zero gate-source bias). When MOSFETs are used as discrete devices, the substrate contact (labeled B for body in the figure) is usually connected to the source. In integrated circuits that use only one channel type, all of the transistors have a common substrate. Under these circumstances, it is common practice for a significant number of these devices to have their source terminals connected to other circuit components, not to the substrate. This connection results in complicated relationship between the gate-source voltage and drain current. Here it is assumed that, the source and substrate are connected together.

4.2.1.1 Drain Characteristics for the Enhancement-Mode MOSFET:

The basic electrical characteristics of a MOSFET can be described by a set of curves in which the drain current $I_{DS}$ is plotted as a function of the drain-source voltage $V_{DS}$ for given values of the gate-source voltage $V_{GS}$. These curves are called the drain (or output) characteristics of the MOSFET. Other curves, called input characteristics, relate the drain current $I_{DS}$ to the gate-source voltage $V_{GS}$ for given values of the drain-source voltage $V_{DS}$.

Typical output characteristics for an n-channel enhancement-mode MOSFET are shown in Fig. 4.4(a). Fig. 4.4(b) shows a typical input characteristic of a MOSFET, pointing out the regions of operation.
Fig. 4.4(a): Output Characteristics of an n-channel enhancement mode MOSFET

Fig. 4.4(b): Input Characteristics of an n-channel enhancement mode MOSFET
The drain nonsaturation characteristics are defined by the equation

\[ I_{DS} = \beta [(V_{GS} - V_{TH})V_{DS} - \frac{V_{DS}^2}{2}] \] (4.3)

The quantities \( \beta \) and \( V_{TH} \) are device parameters that must be either measured or calculated. The drain characteristics shown in Fig. 4.4(a) indicates that there are two basic regions of operation of the MOSFET, corresponding to very low \( V_{DS} \ll (V_{GS} - V_{TH}) \) (nonsaturation region) and very high \( V_{DS} \gg (V_{GS} - V_{TH}) \) (saturation region) values of the drain voltage. The basic characteristics for these two regions can be derived now. The locus of points dividing the saturation region from the nonsaturation region is defined by

\[ V_{DS} = (G_{VS} - V_{TH}) \] (4.4)

For digital applications, the MOSFET operates on both sides of the curves specified by equation (4.4). For analog applications, the MOSFET is usually operated in saturation.

Considering Fig. 4.5, a drain voltage \( V_{DS} \) is applied to MOSFET under the condition \( V_{GS} > V_{TH} \), necessary to ensure that a conducting channel has been formed between the source and drain regions, where \( x \) is the distance coordinate measured along the length of the channel from source to drain.
The application of $V_{DS}$ will cause a voltage drop along the channel which is indicated by the function $V(x)$, and whose value varies from 0 to $V_{DS}$ as it proceeds from the source to the drain. As indicated, the potential at a point $x_{ch}$, as shown in Fig. 4.5, by $V(x_{ch})$. The existence of such a potential implies that the voltage between the gate and a small section of channel placed at $x_{ch}$ is

$$V'_{GS} = V_{GS} - V(x_{ch})$$

(4.5)

The width and charge density at each point in the channel are then determined by $V'_{GS}$ and will vary along the $x$ direction as indicated in Fig. 4.5. In particular, the channel will show maximum width at the source end and minimum width at the drain end. The charge in the differential section $\Delta x$ of channel at $x_{ch}$ is then given by

$$\Delta Q_n = \Delta C_{ox} (V'_{GS} - V_{TH})$$

(4.6)
where \( \Delta C_{OX} = \varepsilon_{ox} W \frac{\Delta x}{x_o} \) \hspace{1cm} (4.7)

In equation (4.7), \( C_{ox} \) is the capacitance of oxide layer, \( \varepsilon_{ox} \) is the dielectric constant of the oxide, \( x_o \) is the oxide thickness, and \( W \) is the width of the device.

The charge \( \Delta Q_n \) can also be written in terms of \( V_{GS} \) and \( V(x_{ch}) \) by using equation (4.5) as

\[
\Delta Q_n = \Delta C_{OX} [V_{GS} - V(x_{ch}) - V_{TH}] \hspace{1cm} (4.8)
\]

To calculate the drain current that flows under these conditions, it is first noticed that the time needed for carriers (electrons) to flow across the section \( \Delta x \) at \( x_{ch} \) is

\[
\Delta t = \frac{\Delta x}{v_n} = \frac{\Delta x}{\mu_n E(x_{ch})} \hspace{1cm} (4.9)
\]

Where \( E(x_{ch}) \) is the field in the channel at \( x_{ch} \) induced by the application of \( V_{DS} \). The minus sign in equation (4.9) derives from the definition of the positive direction of \( E(x) \). Thus, the current flowing through the section \( \Delta x \) can be written as

\[
I_{DS} = \frac{\Delta Q_n}{\Delta t} \hspace{1cm} (4.10)
\]

By using equation (4.8), we can rewrite equation (4.10) in the form

\[
I_{DS} = \frac{\Delta C_{OX}[V_{GS} - V(x_{ch}) - V_{TH}]}{\Delta t} \hspace{1cm} (4.11)
\]

Using equation (4.7), we write equation (4.11) as
\[ I_{DS} = -\frac{\mu_n e_{ox} W}{x_0} [V_{GS} - V(x_{ch}) - V_{TH}] E(x_{ch}) \]  \hspace{1cm} (4.12)

Since
\[ E(x_{ch}) = -\frac{dV(x)}{dx} \bigg|_{x=x_{ch}} \]  \hspace{1cm} (4.13)

we obtain
\[ I_{DS}dx = \frac{\mu_n e_{ox} W}{x_0} [V_{GS} - V(x_{ch}) - V_{TH}] dV(x) \]  \hspace{1cm} (4.14)

Equation (4.14) represents the current \( I_{DS} \) flowing through a section of width \( \Delta x \) centered at \( x \). The channel, in its turn, is formed of a large number of such sections, all of which are connected in series, going from the source to the drain. Moreover, the same current \( I_{DS} \) must flow through each section for a given \( V_{DS} \). Therefore, the equation (4.14) can be integrated as follows:
\[ I_{DS} \int_0^L dx = \frac{\mu_n e_{ox} W}{x_0} \int_0^L [(V_{GS} - V_{TH}) - V] dV \]  \hspace{1cm} (4.15)

Carrying out the integration and dividing by the channel length \( L \), the \( I_{DS} \) current can be obtained as-
\[ I_{DS} = \frac{\mu_n e_{ox} W}{x_0 L} [(V_{GS} - V_{TH}) V_{DS} - \frac{V_{DS}^2}{2}] \]
\[ = \beta [(V_{GS} - V_{TH}) V_{DS} - \frac{V_{DS}^2}{2}] \]  \hspace{1cm} (4.16)

This is exactly equation (4.3), when \( \theta \) value is set as-
\[ \beta = \frac{\mu_n C_{ox} W}{L} \]  \hspace{1cm} (4.17)
Where $C_{ox}$ is the capacitance of the gate oxide per unit area.

In equation (4.17), $\mu_n$ is constant up to sufficiently large values of $V_{GS}$ and $\beta$ begins to decrease when $V_{GS}$ becomes large enough. Equation (4.17) states that, for a given type of channel (given $\mu$), the parameter $\beta$ can be determined directly once the gate width $W$, the gate length $L$, and oxide properties ($X_o$ and $\varepsilon_{OX}$) are known.

At low drain voltages, i.e., for $V_{DS}<(V_{GS}-V_{TH})$, the quadratic term in $V_{DS}$ in equation (4.16) can be neglected. Thus, under this assumption, we can write

$$I_{DS} = \beta(V_{GS} - V_{TH})V_{DS}$$

(4.18)

Equation (4.18) states that the low drain voltage characteristics are a series of straight lines passing through the origin, with slopes that increase as $V_{GS}$ increases. In general, each of these characteristics can be described by the equation

$$I_{DS} = G_{DS}V_{DS}$$

(4.19)

where $G_{DS}$ is called the drain-source conductance of the MOSFET. From equation (4.18) and (4.19), we have

$$G_{DS} = \beta(V_{GS} - V_{TH})$$

(4.20)

The variation in channel width with $V_{DS}$ has given the physical key to obtaining the basic MOSFET equation (equation (4.16)). However, this derivation is valid only as long as $V_{DS}<(V_{GS}-V_{TH})$, i.e., when the MOSFET is operated in the so-called nonsaturation region, because when $V_{DS}=(V_{GS}-V_{TH})$ the channel will (in principle) be reduced to zero width at the drain end. The physical situation is shown in Fig. 4.6(a): the channel is said to be pinched off.
at the drain. The drain current that flows under this condition can be calculated from equation (4.16) by substituting $V_{DS} = (V_{GS} - V_{TH})$. The result is

$$I_{DS} = \frac{\beta}{2} (V_{GS} - V_{TH})^2$$

(4.21)

By differentiating equation (4.16), it is found that the drain current has a horizontal tangent at $V_{DS} = (V_{GS} - V_{TH})$, as indicated in the drain characteristics of Fig. 4.4(a).

For the current given by equation (4.21) to flow, it is necessary that some very high velocity electrons exist in a thin region near the drain. Then, the channel is in practice not pinched down to exactly zero width, but rather to a point where there are just enough electrons to carry the drain current when each electron is traveling at its maximum velocity.

![Diagram](image)

Fig. 4.6(a): Shape of the channel width of an n-channel enhancement mode MOSFET for $V_{DS} = (V_{GS} - V_{TH})$
The presence of thin pinched-off region is more evident when $V_{DS}$ is increased beyond $(V_{GS}-V_{TH})$. When this happens, the actual channel pinch-off point, indicated by $x_{pop}$ in Fig. 4.6(b), will shift very slightly from drain toward the source. The voltage drop from source to the pinch-off point, $V(x_{pop})$, will be exactly $(V_{GS}-V_{TH})$, since this is the value needed to reduce the channel charge and width to zero. The remainder of the applied drain voltage, $[V_{DS} - (V_{GS}-V_{TH})]$, is dropped across the region from the extrapolated pinch-off point ($x_{pop}$) to the drain, and the charge in this region can be neglected.
Thus, it follows that the non-pinched-off portion of the channel behaves like a MOSFET that has a gate length \( L = x_{pop} \) and is always operated at \( V'_{DS} = (V_{GS} - V_{TH}) \). The total charge in the non-pinched-off portion of the channel and the voltage drop across it are practically fixed at the values they have when \( V_{DS} = (V_{GS} - V_{TH}) \), so to a first approximation the current \( I_{DS} \) flowing in the channel will be independent of \( V_{DS} \) for all values of \( V_{DS} > (V_{GS} - V_{TH}) \). In other words, the drain current \( I_{DS} \) saturates at its pinch-off value. As a consequence we can extend the drain current characteristics horizontally from the pinch-off point to larger values of \( V_{DS} \) (see Fig. 4.4(a)). Thus, at large drain voltages, i.e., for \( V_{DS} > (V_{GS} - V_{TH}) \), the drain current \( I_{DS} \) in this region is given by equation (4.21).

The MOSFET is said to be operated in the saturation mode. From a circuit point of view, the fact that \( I_{DS} \) can be independent of \( V_{DS} \) implies that the output current \( I_{DS} \) is controlled entirely by the input voltage \( V_{GS} \). Moreover, the output terminals of the MOSFET are therefore represented as a \( V_{GS} \)-controlled current source instead of a conductance as in the nonsaturated operation mode.

The physical phenomena just described and the corresponding electrical behavior of the MOSFET are summarized in Table 4.1.

In the preceding analysis, the channel length \( L \) can be considered as constant. In reality, \( L \) is determined by the distance between the depletion regions surrounding the source and drain. The widths of these regions are functions of the source-substrate and drain-substrate biases. The width of the drain depletion region increases with drain voltage, thereby decreasing the channel length, which increases the gradient of carrier concentration, and therefore
increases the channel current. This increase in channel current due to channel length modulation is called the Early effect. Because the dependence of $I_{DS}$ on $L$ is explicit (through the parameter $\beta$) in equations (4.16) and (4.21), we can solve directly for the drain conductance $G_{DS}$ of the MOSFET.

Table 4.1 Basic properties of an $n$-Channel Enhancement-Mode MOSFET

<table>
<thead>
<tr>
<th>Gate &amp; drain bias conditions</th>
<th>Channel conditions</th>
<th>Drain Characteristics</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{GS} \leq V_{TH}$ and $V_{DS} \geq 0$</td>
<td>No inversion layer $Q_n = 0$</td>
<td>$I_{DS} = 0$</td>
</tr>
<tr>
<td>$V_{GS} &gt; V_{TH}$ and $0 &lt; V_{DS} \leq (V_{GS} - V_{TH})$</td>
<td>Inversion layer exists $Q_n = C_n (V_{GS} - V_{TH})$</td>
<td>$I_{DS} = \beta (V_{GS} - V_{TH}) V_{DS}$</td>
</tr>
<tr>
<td>$V_{GS} &gt; V_{TH}$ and $0 &lt; V_{DS} \leq (V_{GS} - V_{TH})$</td>
<td>Inversion layer exists Decreasing channel thickness near drain</td>
<td>$I_m = \beta \left[(V_{DS} - V_m) V_m - \frac{V_m^2}{2}\right]$</td>
</tr>
<tr>
<td>$V_{GS} &gt; V_{TN}$ and $V_{DS} \geq (V_{GS} - V_{TN})$</td>
<td>Inversion layer exists pinch-off near drain</td>
<td>$I_m = \frac{\beta}{2} (V_m - V_m)$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Voltage controlled current source</td>
</tr>
</tbody>
</table>

Because the drain current is inversely proportional to $L$, the drain conductance (which manifest itself as a nonzero slope on the drain characteristics for large values of $V_{DS}$) is proportional to $I_{DS}$ and inversely proportional to $L$. Usually, this conductance is approximated by a constant depending on the given
process and device geometry. Because the conductance is proportional to $I_{DS}$, in this approximation the extrapolated drain curves all intersect the voltage axis at a single point, which is $V_{DS} = -V_0$. Thus, to take into account the channel-length modulation, the term $G_{DS} V_{DS}$ can be simply added to the expressions of the drain current just obtained [3].

4.2.2 Neuron Model for Excitation and Inhibition of Postsynaptic Membrane of Levine, Marvin et al:

The postsynaptic membrane of a single neuron can have excitatory and inhibitory transmitter-gated ion channels. Generally, excitatory channels are specific to sodium ions and inhibitory channels are specific to chloride ions. The excitatory and inhibitory ionic current control the change in membrane potential. The influx of sodium ions causes an excitatory postsynaptic membrane potential (EPSP), whereas the influx of chloride ions causes an inhibitory postsynaptic membrane potential (IPSP). When excitation predominates, the membrane potential increases. If a sufficient number of transmitter gated sodium channels are open, then the membrane potential exceeds the threshold for initiating an action potential. When inhibition predominates, the membrane potential decreases (or hyperpolarizes), and triggering of an action potential is impeded.

In the excitatory and inhibitory postsynaptic circuit model of Levine, Marvin et al, the variable conductance of the transmitter-gated ion channels is represented by MOSFET. The MOSFET is chosen because as described in MOSFET theory that it functions as a voltage controlled conductance in the linear region (equation (4.20)). For analysis, rewriting the equation (4.20):
\[ G_{DS} = \beta (V_{GS} - V_{TH}) \]  

(4.22)

Where, \( \beta = \mu_n C_{ox} \frac{W}{L} \) (from equation (4.17)). And \( G_{DS} \) is the conductance of the MOSFET, \( V_{GS} \) is the gate voltage, \( V_{TH} \) is the threshold voltage, \( C_{ox} \) is the capacitance of the gate oxide, \( \mu \) is the electron mobility constant, \( W \) is channel width, and \( L \) is the channel length.

The excitatory and inhibitory postsynaptic circuit model of Levine, Marvin et al is shown in Fig 4.7.

In this model, an NMOSFET represents the conductance of the transmitter-gated sodium channels and a PMOSFET represents the conductance of the
transmitter-gated chloride channels. $C_m$ represents the capacitance of the lipid bilayer; $V_{Na}$, $V_{Cl}$ and $V_K$ are the Nernstian membrane potentials for sodium, chloride and potassium; $G_K$ is the conductance of non-gated potassium channels; $G_{Na}$ is the conductance of transmitter-gated sodium channels; and $G_{Cl}$ is the conductance of the transmitter-gated chloride channels. $V_{gE}$ and $V_{gl}$ are the gate input voltages applied to elicit MOSFET conductances $G_{Na}$ and $G_K$ respectively.

The postsynaptic membrane potential $V_m$ is controlled by the conductance of the transmitter-gated ion channels. From Fig. 4.7, the $V_m$ is established by the ionic and capacitive membrane current, given by the following equation:

$$C \left( \frac{dV_m}{dt} \right) + (V_m - V_{Na}) G_{Na} + (V_m - V_{Cl}) G_{Cl} + (V_m - V_K) G_K = 0 \quad (4.23)$$

In SPICE simulation, the membrane potential $V_m$ is obtained as a function of the relative weighting of the ionic conductances.

The conductance of the transmitter-gated channels is controlled by transmitter-receptor binding activity. The MOSFET conductance $G_{DS}$ is controlled by the gate voltage. In the excitatory and inhibitory postsynaptic circuit model of Levine, Marvin et al, the MOSFET gate voltage functionally represents the transmitter-receptor binding activity. The simulation input voltage applied to the MOSFET gate is expressed as:

$$V_g(t) = V_o \left[ (1 - \exp (-k_1 t)) + \exp (-k_2 t) u(t-t_m) \right] \quad (4.24)$$

Where $u(t-t_m)$ is the Heaviside function, and $V_o$ is a voltage proportional to the maximum attainable conductance, when all the transmitter-gated channels for
a specific ion are open. The component values assigned in this model, for SPICE simulation, are based on the physical parameters of biologic neurons.

Fig 4.8 shows the simulated result of the excitatory and inhibitory postsynaptic circuit model of Levine, Marvin et al.

The top waveform represents the EPSP, the bottom waveform the IPSP and middle waveform the potential arising from combined excitation and inhibition. The postsynaptic membrane potential $V_m$ is established by spatial summation and temporal integration of the membrane current. The simulation output for the excitatory case illustrates an EPSP with sufficient amplitude for triggering an action potential. The output in the inhibitory case shows an EPSP that would suppress the triggering of an action potential. The output from
combined excitation and inhibition demonstrates the formation of a membrane potential based on the relative weighting of the sodium and chloride conductances.

The excitatory and inhibitory postsynaptic circuit model of Levine, Marvin et al., is a physiologically motivated model which provides a practical method for simulating the structure and function of the postsynaptic membrane. The simulation result shows the effects of excitation and inhibition on a single neuron. This model demonstrates the basic mechanism of integrative decision-making that occurs at the postsynaptic region of the neuron [4].

4.2.3 Synaptic Neuron Model of Levine, Marvin et al:

Michael D. Levine, Marvin F. Eisenberg, and Thomas L. Fare proposed a model of postsynaptic membrane at neuromuscular junction. This neuromuscular junction occurs biochemically between presynaptic membrane and postsynaptic membrane. In this circuit model of postsynaptic membrane, excitatory transmitter gated ion channels are simulated with a metal-oxide semiconductor field effect transistor (MOSFET). MOSFET is considered here because it functions as a voltage controlled resistor. Due to binding of neurotransmitter with the receptor of postsynaptic membrane, there will be influx of Sodium to the cell. If sufficient number of Sodium channels opens then membrane potential exceeds the threshold and generates an action potential.

The postsynaptic membrane basically consists of transmembrane protein ion channels and lipid bilayer. Fig. 4.9 shows the circuit model for membrane. Simulation of the model yields an output representing the overall membrane potential of the postsynaptic region [5].
In this model $C_m$ represents the capacitance of lipid bilayer. $V_{Na}$ and $V_k$ represent the Nernstian membrane potential for sodium and potassium. $G_k$ represents the conductance of non-gated potassium channel. $G_{Na1}$, $G_{Na2}$, $G_{Na3}$ represent conductance of acetylcholine-gated sodium channels. $V_{g1}$, $V_{g2}$ and $V_{g3}$ are the MOSFET gate voltages used for obtaining transmitter gated sodium conductances.

The membrane is divided into three patches to demonstrate the sodium current.

$$I_{Na} = I_1 + I_2 + I_3$$  (4.25)

Due to spatial summation of sodium current through the open acetylcholine gated channels, the membrane potential $V_m$ will be increased.
\[ C_m \left( \frac{dV_m}{dt} \right) + (V_m - V_{Na}) G_{Na} + (V_m - V_k) G_k = 0 \]  
(4.26)

Where \( G_{Na} \) is the total sodium conductance and \( G_k \) is the total potassium conductance of the postsynaptic membrane. Levine et al. [5] got the membrane potential \( V_m \) by spatial and temporal varying acetylcholine-gated sodium conductance \( G_{Na} \) and simulation is done using Personal Computer Simulation Program with Integrated Circuit Emphasis (SPICE) software.

The conductance of the acetylcholine-gated sodium channels in a patch of membrane is controlled by activity of transmitter-receptor binding [6]. Analogous to this is the MOSFET conductance \( G_{DS} \) which is controlled by the gate voltage of the MOSFET. In the Levine et al. model of the postsynaptic membrane, the MOSFET gate voltage functionally represents the transmitter-receptor binding activity. For the simplest case, binding is governed by the chemical reaction:

\[
\begin{align*}
\text{(unbound)} & \quad 2\text{ACH} + \text{ACHR} \quad \xleftrightarrow[k_1/k_2]{\text{(bound)}} \quad 2\text{ACH} - \text{ACHR} \\
\end{align*}
\]

(4.27)

Where \( K_1 \) and \( K_2 \) are the rate constant for the forward reaction and the reverse reaction respectively. These rate constants are analogous to the time constants utilized by the exponential voltage function in SPICE. The simulation input voltage applied to the MOSFET gate is expressed as

\[
V_g(t) = V_o[(1 - \exp (-k_1 t)) + \exp (-k_2 t) u(t - t_m)]
\]

(4.28)

Where \( u(t-t_m) \) is the Heaviside function, and \( V_o \) is a voltage proportional to the maximum attainable conductance of the membrane patch when all the acetylcholine-gated sodium channels are open.
The Heaviside function is generally used in the mathematics of control theory and signal processing to represent a signal that switches on at a specified time and stays switched on indefinitely. It is also used in structural mechanics together with the Dirac delta function to describe different types of structural loads. It was named after the English polymath Oliver Heaviside [7].

Fig 4.10 shows the simulated postsynaptic membrane potential of Levine et al. model of the postsynaptic membrane.

![Simulated Postsynaptic Membrane Potential of Model of Levine, Eisenberg, and Fare](image)

The top waveform represents the normal postsynaptic membrane potential and the bottom waveform represents the pathologic state postsynaptic membrane potential. The $V_m$ is established by spatial summation and temporal integration of the acetylcholine-gated sodium current. When $V_m$ exceeds a threshold value, in the -60 to -40 millivolt range, as shown in the simulation of the normal case, the voltage-gated sodium channels open causing initiation of an action potential. The simulation output in the case of
myasthenia gravis illustrates the degraded membrane potential secondary to the pathologic function of the acetylcholine-gated channels. This model is generally applicable in the field of neuropharmacology for simulation of receptor function and electrical activity of the postsynaptic cell.

4.3 References:


