CHAPTER 8

CONCLUSION AND FUTURE SCOPE

8.1 Conclusion

In the near future, the eventual end to the roadmap of semiconductors is anticipated which hinders further scaling of CMOS technology. Alternative approaches are desired to satisfy those expectations to increase in the digital applications. This research is devoted in pursing solutions to the simulation issue of single electronics that come up as Single Electron Devices (SEDs) and are increasing by involved in next generation circuit architecture design. It has been proved that the SEDs models are more appropriate for time complexity and accuracy. The research also explored the characteristics of SE-based circuits and proposed a hybrid model that could be used to estimate and analyze its output both efficiently and accurately. The new model was used at room temperature condition.

Chapter one, discusses on the background knowledge of single electronics and single electron devices. The brief introduction of single electron technology was also presented, as well as its motivation (mainly related to the concern that it is able to conquer those drawbacks of conventional devices), objectives and solution to the problems of single electron transistor.

Chapter two, explains about the literature review of Single electron transistor, hybrid CMOS-SET and reversible logic gates of SET.

Chapter three discusses advantages of single electron were explained in detail, including the small feature size and low power consumption, then the working principle of SET based devices and a short history of their experimental studies were discussed. An initial current voltage characteristic of single-electron transistor was obtained using master equation based method. To compensate the inherent drawbacks of SET, concept of hybrid single-electron transistor has been taken into consideration for its realization. Transfer
characteristic of a hybrid CMOS–SET inverter circuit was designed at using room temperature operable values. Also hybrid SET-CMOS circuit co-simulations were successfully performed by implementing the new model; and extensive simulation results showed the advantages of realizing some application circuits using SED’s new functionality works.

Chapter four narrates the design concept of hybrid SET-CMOS based half subtractor and full subtractor. The circuits are designed and simulated at room temperature and portrays the comparison of power consumption in hybrid SET-CMOS model and conventional CMOS model. The results show that hybrid technology consumes less power than conventional model.

Chapter fives shows the design concept of hybrid SET-CMOS based one bit comparator and two bit comparator. The circuits are designed and simulated at room temperature using T-Spice and simulation results are compared with the conventional model and it shows that the new design of comparator provides the good efficiency with less power consumption.

Chapter six explains the design concept of hybrid SET-CMOS based 3 to 8 decoder circuits, which will be a necessary part of a future processor. Its disadvantage, possibly slower operation, is outweighed by its advantages, such as small circuit size, simplicity and predictable operation. It is important to reiterate the analysis of our designs is based on a T-spice simulation model.

Chapter seven explains the reversible logic gates, and quantum computing made the feasibility on factoring problem. Here we will address the issues in quantum computing, that of qualitative differences between quantum and the classical models for computation and a quantum model for computation. On the other hand hybrid SET – CMOS based reversible logic Subtractor, Comparator and Decoder circuits has been implemented and its performance has been evaluated in terms of delay, power delay product, power consumption, garbage output and quantum cost.
Chapter eight shows the conclusion of the work carried out during the research and the future scope of the above work.

Finally the work explains the new basic CMOS-SET logic gates which are capable for designing Half Subtractor, Full Subtractor, one bit Comparator, two bit Comparator, and 3 to 8 Decoder circuits at room temperature. An important characteristic that was taken into account for this design was the possibility of room temperature operation. All these circuits are simulated and verified in the tanner environment. Also this module portrays the comparison of power consumption and product delay analysis in hybrid SET-CMOS model and conventional MOS model, implementation and realization of Subtractor, Comparator and Decoder are done using reversible logic gates which demonstrates its superiority than the existing designs in terms of computational complexity. The result of the proposed design shows that the circuits are more optimized in terms of delay, power consumption, and power delay product. The reversible logic gates are based on pass transistors, there is a problem occurs of loss the information after passing through a number of stages. The problem can be fixed with the Single electron Transistor. The proposed reversible Subtractor, Comparator and decoder has a high performance as compared to other reversible circuit. This proposed reversible circuit is a design using nanotechnology. The other power reduction technique is performing the less consumption in comparison of CMOS technique. All the circuits are synthesized and verified using Xilinx 10.1SE software tool – Spartan 3 AN.

8.2 Future Scope

The present work is fare enough to study the performance analysis of Hybrid SET-CMOS based logic circuits; still there are some suggestions for future work which can enhance the accuracy of the present work.

The Current development of subtractor, comparator circuit synthesis at gate level can be even improved for sequential circuits using the reversible logic synthesis design criteria for it. Also the same circuits can
be even improved using the further recent gets that provide a better reduced power dissipation and delay.

Even other circuit’s components like multipliers, shifters, etc can be implemented using reversible logic gates. Also these reversible logic circuits are used in many applications like in the area of digital image processing and communications for enabling the storage and hence to retrieve back the same and information that is being stored. As the wide range of applications of hybrid SET-CMOS reversible subtractors are laptops, wearable computers, implanted medical devices, wallet smart cards.

The hybrid SET-CMOS logic can be utilized to design arithmetic logic unit (ALU). Since ALU, is a fundamental building block of CPU, is designed with the promising technology of Hybrid SET-CMOS logic, it provides low power dissipation less than the CMOS model. Power gain improvement for SET can be evaluated under the influence of parameters ($C_G$, $R_{TD}$, $C_{TD}$, $R_{TS}$ and $C_{TS}$). The effect of source tunnel junction thickness can be the key parameter for influencing power gain and a proper stability analysis should be included in the analysis to enhance its application range.