CHAPTER – 1

MOSFET MODELS, QUANTUM MECHANICAL EFFECTS AND MODELING APPROACHES

1.0 INTRODUCTION

CMOS technology has contributed significantly to the microelectronics industry thus playing an important role in the overall development of all the countries. This is primarily due to its vast applications in every sphere and in nearly every industry. The performance and density of a CMOS chip can be improved through device scaling which is inevitable as also propounded by Moore law which says that the transistor density on a CMOS chip doubles approximately after every one and a half years [1, 2]. Continuing with the Moore law, the Gate length of the MOSFET will eventually shrink to 20 nm in 2009 [3]. This will make many new applications possible. Especially important are the commercial requirements of miniaturization such as mobile equipment etc.

Seeing the trend of down scaling, continuous improvements in the VLSI MOSFET device models are required so that the exact behavior of deep sub-micron and nanometer scaled MOSFETs can be described with accuracy.

MOSFET modeling is facing difficulties to achieve accurate description of such scaled down devices. The reason is that many complicated new phenomena are arising which are not easy to describe. One such phenomenon arising out of down scaling the MOSFET is the failure of classical physics in the at nanoscale levels in MOSFETs. As CMOS technology scales down aggressively, it approaches a point, where classical physics is not sufficient to explain the behavior of a MOSFET. At this classical physics limit, Quantum Mechanics has to be taken into account to accurately assess the overall performance of a MOSFET.

The principle objective of this work is to examine the appropriate physics and methodology to model a MOSFET device as applicable to the extremely scaled transistors by incorporating the Quantum Mechanical
Effects such as Quantum Mechanical tunneling and Energy Quantization of charge carriers.

1.1 MOSFET PHYSICS

Metal-Oxide-Silicon Field-Effect-Transistor (MOSFET) operates on the principle of creating an inversion layer using a Gate voltage giving applications in analog and digital areas. It is basically a two-dimensional device. Its input voltage is applied to the Poly Silicon Gate, Substrate and Source are generally grounded and at the drain a voltage is applied to extract the charge carriers as shown in Figure 1.1.

![Basic MOSFET Structure](image)

Fig. 1.1: Basic MOSFET Structure

1.2 SCALING REQUIREMENTS AND IMPLICATIONS

For the last six decades, the semiconductor industry has been working hard to miniaturize the structure of the MOSFET because of accommodating more transistors on a single chip, thus performing multi tasks and also resulting in the reduced cost of the chip production. The speed of the chip also improves ideally due to the less power consumption and small Gate lengths. Despite some merits of scaling down, there are some implications which need to be addressed seriously while scaling down at extremely low Gate lengths such as:
To scale down the channel length without excessive short-channel effects, the oxide thickness should be reduced. The reduction of leakage currents is the main issue in MOSFET scaling [4, 5]. For the 90 nm technology node, the thickness of silicon oxide is of the order of sub 2nm [6]. Quantum Mechanical tunneling through the Gate oxide leads to excessive power dissipation and loss of on-current density [7].

As the channel length of the MOSFETs is approaching sub 100nm and the oxide thickness of the order of sub 2nm, classical physics fails to predict the behavior of MOSFETs. This is due to the fact that Quantum Mechanical Effects such as Energy Quantization of energy levels come into picture.

The Quantum Mechanical tunneling between the source and drain also takes place for scaled down MOSFET in sub-10 nanometer regions. This will ultimately retard the scaling process of the MOSFET and will make them useless for switching purpose as the leakage currents dominate the conduction currents as also given in [8].

**1.3 MOSFET MODELS**

MOSFET models play an important part in the development of an efficient chip industry. These models have been continuously developed and improved over the past many years. These improvements resulted in the increase of the model parameters to cover additional effects. The MOSFET models are used by circuit simulators. The circuit designer’s efficiency to develop a circuit depends mainly on the device model. The accuracy and simplicity of the model has a deep influence on the designing and fabrication of the circuit. Thus device models act as a bridge between the Integrated Circuit designers and those working for Process technology development as shown in Figure 1.2.

Any device model is categorized as Numerical models and Compact models. Numerical models are based on solving the partial differential equations describing the detailed physics of the device. These models are
computationaly intensive, complex and take a lot of computation time to solve the circuits. However, Compact models describe the device in a simplified manner and hence they are fast.

Fig. 1.2: Complete Flow of the Technology, Modeling and Design

There are three types of Compact device models.

1. Analytical models
2. Empirical models
3. Table lookup models

Analytical models are physics based device models. The empirical models describe equations based on data fitting from the experimental values. The Table lookup models contain device data in the form of tables stored in the memory. The data can be accessed once the table lookup model is executed.

The accuracy of analytical device models is immense. So, main emphasis in this thesis will be to develop a Compact model of the MOSFET which will be analytical in nature.

Some industry standard Compact models are reviewed here:

a) Charge based models
b) Potential based models
c) Conductance based models.
1.3.1 The charge based MOSFET models

Charge based modeling approach is one of the basic and primitive modeling approaches. It is based on the computation of the inversion charge density in the MOSFET channel in terms of the terminal voltages i.e. Gate and drain voltages [9]. In this approach, a linear approximation is made between the surface potential and the applied drain and Gate voltages. This eliminates the surface potential and relates the input Gate voltage to the output drain current, giving a simple current-voltage equation. These models are used in the initial version of the circuit simulator SPICE. These are also called as threshold voltage based models as they are based on defining all the parameters based on threshold voltage such as, drain current, voltage, drain saturation voltage etc. The most important advantage of this approach is its simplicity and flexibility to add features resulting from technology advancements. Additional parameters are introduced to take care of shrinking technology effects. The number of model parameters, therefore, increases as technology advancement takes place. This approach explains the behavior of the MOSFET in all regions of its operation such as weak, moderate and strong inversion separately and hence, it is also called a regional approach. So, these models require smoothening parameters, these models are somewhat empirical in the interfacing regions and thus, the device behavior is not described accurately.

The prominent Charge based models for the MOSFET are divided into mainly the first, second and third generation models depending on their level of complexity.

First Generation SPICE Models

The SPICE models level 1, Level 2, Level 3 are called first generation SPICE Models [10, 11]. These were the original models developed at the University of California, Berkeley, USA.

Level 1 model is a basic SPICE model. It is primarily used for the devices having long channel lengths greater than 5um [10]. Its uses Gradual channel approximation (GCA) to model the output drain current characteristics. In GCA, it is assumed that the longitudinal electric field from
source to drain varies gradually. The only short-channel effect considered in this model is the modulation of MOSFET channel length by the drain voltage. This results in the increased drain current in the saturation mode of the MOSFET.

Level 2 model (Gate length < 5um) [10] is much more complex than Level 1 model. It includes short-channel effects, such as, mobility reduction due to high Gate fields, threshold voltage reduction due to charge sharing in the channel and velocity saturation. Sub-threshold current model is also included. The model does not give accurate results at lower geometries.

Level 3 model (Gate length <1um) [10] is more empirical in nature. The mathematical expressions observed in this model are more efficient and a more simplistic approach is followed. This model is also geometry dependent and its performance suffers due to the decrease in geometries. No additional effects as in Level 2 are added.

**Second Generation SPICE Models**

The second generation models viz. BSIM1, HSPICE level 28, BSIM2 etc. attempt to take care of the problems encountered in the first generation models [10]. They are used for sub-half micron lengths. They have separate parameters for geometry dependence which are fitted with the parameters extracted for a particular dimension. These models are more empirical in nature as compared to first generation models.

**BSIM 1 model (Gate length <1um) [10]**

In the first generation models there is a constant problem of discontinuity in the various regions from active to saturation. This problem is solved to a larger extent with the addition of some empirical parameters in the model equations.

**HSPICE level 28 (Gate lengths ranging from 0.3um-0.5um) [10]**

In this model, a minor modification of BSIM1 model has been done with respect to the mathematical expressions of some of the electrical parameters to improve the accuracy of the model.
BSIM2 (Gate length < 0.2μm) [10]

This is more improved than BSIM1 model. The main drawback is large number of parameters involved in it.

Third Generation SPICE Models

The third generation of charge based models is the advanced versions of the BSIM models. These are BSIM3, BSIM4 and BSIM5. These models are for deep sub-micron and nanometer scale MOSFETs.

BSIM 3 Model (Gate length < 0.18μm) [10]

In this model, an algorithmic approach is used to solve model equations and is faster than earlier models. BSIM 3 accounts for major physical mechanisms such as short and narrow channel effects on Threshold Voltage, Non-Uniform Doping Effects device performance, Mobility reduction due to vertical field and its effect on drain current, Carrier Velocity Saturation, Drain induced barrier lowering and Channel length modulation. The other effects considered are parasitic resistance effects, basic empirical Quantum Mechanical Charge Thickness Model and a model of Unified Flicker Noise.

BSIM 4 Model (Gate length < 0.13μm) [12]

It is an improvement over the BSIM 3 model. More physical effects have been taken in this model, such as, the inclusion of Quantum behavior of the MOSFET like Quantization of inversion layers empirically, Quantum mechanical charge-layer-thickness model for both I-V and C-V characteristics. This model also includes the accurate Gate direct tunneling model. It uses the approach of Lee and Hu [13] to model the Gate direct tunneling current. Some of the other features of BSIM 4 model are accurate modeling of MOSFET parameters for high-frequency applications and Velocity- overshoot effect. It also models well weak inversion charges, narrow width effects, retrograde doping profiles, mobility model, Improved unified flicker noise model [13] etc.
BSIM 5 Model (Gate length < 0.1um) [14]

It is for sub-100nm CMOS circuit simulation. The BSIM5 model is a recently developed continuous and accurate charge-based model which relies on the Poisson equation solution and Pao Sah current formulation. The model results in I-V and C-V equation in all the regions of operation. It is also perfectly suitable for RF/analog circuit simulation. The Poly-Silicon Gate Depletion effects and empirical model of Quantum Mechanical Effects are also included in this modeling approach.

MOS Model 9 [10, 36] is a recent modeling approach by Phillips, Netherlands. This model is applicable at deep sub-micron region and attempts have been made to include the Quantum Mechanical Effects also in this model.

Needless to say that the charge based modeling approach includes empirical relations of Quantum Mechanical Effects in the modeling approach. These are simple but not so accurate. So, the advanced models must delve into this matter while modeling the MOSFETs in the nanometer scale.

1.3.2 Potential based MOSFET model

This model approach is based on accurate MOSFET device physics and therefore it is more accurate than the charge based models. Moreover, as the scaling continues to the nanoscale region, the charge based models become even more inaccurate in lower geometries as they are Threshold voltage based and the Threshold voltage in a MOSFET cannot be scaled down beyond a certain point.

It is based on the calculation of the potential in the channel of a MOSFET to determine the I-V and C-V characteristics. Most of the potential based models developed so far yield implicit relations of surface potentials. To solve them difficult and complex iterative techniques are required. Due to these difficulties, the potential based approach to model MOSFETs has not found widespread use. Approximate solutions were also used earlier to
calculate the surface potential in terms of Gate to Source voltage. These solutions lead to inaccurate model results. Now attempts are being made to find the exact solutions using the highly advanced softwares available. Therefore, it is expected that the next generation advanced compact MOSFET models would be surface-potential-based. The challenge is to develop practical and efficient surface-potential-based models which do not suffer from the limitations traditionally associated with this approach. Some of the models based on this approach are:

**SP model, Pennsylvania State University, USA [15]**

This model was given by G. Gildenblat and T.L. Chen of Department of Electrical Engineering, Pennsylvania State University, USA. It requires up to 28 parameters. Some of the main features of this model are analytical and non-iterative evaluation of the Surface potential and Mobility modeling incorporating Coulomb scattering. Quantum Mechanical Effects and Poly-Silicon Gate Depletion effect are also included in this model. The terminal voltages and other derived parameters, such as trans-conductance, can be accurately evaluated in all regions of MOSFET operation.

**HiSIM – Hiroshima-University, STARC IGFET Model [16-18]:**

HiSIM is surface-potential MOS-Model valid down to Sub-100nm MOSFETs. This model is very simple and physical in nature. The main features of this model are reverse short-channel effects, Quantum Mechanical Effects, Poly-Silicon Gate Depletion, mobility reduction, Channel-length modulation, Velocity overshoot, Substrate current, Gate Induced Drain Leakage current (GIDL) etc. In this model, the drain current is continuously described in all the regions of operation for all applied voltages using one equation. The Gate current model in HiSIM model considers only the band to band tunneling. The number of fitting parameters is also very few in this model.
1.3.2.1 Empirical Models Dedicated to Analyze Quantum Mechanical Effects

There are some models in which some empirical corrections are made to the surface potential or the inversion charge density to account for the Quantum Mechanical Effects. Some such models are listed below:

**Hansch model [19]**

This model is highly empirical in nature and is incorporated in the standard third generation model equations. It states that due to the Energy Quantization at the nanoscale, the carrier concentration at the interface between semiconductor and oxide becomes the function of the position from the interface as given by

\[ N_c(x) = N_c \left( 1 - e^{-\frac{x-x_0}{\lambda_c}} \right) / \lambda_c^2 \]

where

- \( N_c \) = Classical concentration of charge carriers
- \( x_0 \) (Empirical parameter) = Offset to model nonzero carrier concentration at the interface (At \( x=0, N_c(0)=0 \) i.e. at the surface the carrier concentration reduces to zero, if \( x_0 \) is not included)
- \( \lambda_c \) (Empirical parameter)=Characteristic Length (Measure of how fast Quantum Effects are diminishing in the depth i.e. the Energy Quantization is restricted mainly to the surface and reduces with the depth in the semiconductor).

**Van Dort Model [19]**

Besides considering the displacement of the charge density from the surface (as in the case of Hansch model), this model assumes that the shift of the energy band gap at the interface between silicon and the oxide is directly related to the transverse electrical field. The effect of energy band broadening and the displacement of the carrier concentration from the surface is modeled directly as:
\[ \delta E_g = \beta_1 (E_s)^{2/3} G(z) \]

Where \( \delta E_g \) = Change in the Energy Band Gap with depth

\( \beta_1 \) = Physical constant

\( E_s \) = Transverse Electric field

\( G(z) \) = Decaying Function in depth \( z \) in the substrate

**Hybrid Model [19]**

This model combines the features of Hansch model and Van Dort model. The Energy band gap expression is changed to avoid any problem at zero surface electrical field i.e. at the surface (interface between silicon and the silicon oxide).

The change in the Energy Gap is given by:

\[ \delta E_g = E_s^2 / \{ A \exp(-E_s^2/X_c^2) + E_s^{4/3} \} \]

Where

\( \delta E_g \) = Shift in Energy Gap

\( A \) is a constant

**Inversion Charge Model [20]**

It is a model based on the inversion electron concentration calculation involving the solution of surface potential in the channel. The salient features of the model are Poly Silicon Gate Depletion and Quantum Mechanical Effects. The Energy Quantization is empirically added in the inversion electron concentration.

\[ n_i^{QM} = n_i^{CT} \exp(-\delta E_g/2kT) \]

Where

\( n_i^{QM} \) = Inversion Electron Concentration including Energy Quantization

\( n_i^{CT} \) = Classical Inversion Electron Concentration

\( \delta E_g \) = Shift in Energy Gap
1.3.3 Conductance based MOSFET model

This modeling approach is suitable for low power, low geometry applications for analog design. It is known as EKV (Enz-Krummenacher-Vittoz) model [21] which has been developed by the Swiss Federal Institute of Technology, Switzerland. This model keeps substrate as the reference rather than the source as observed in the potential based and the charge based models. Reasonable accuracy of I-V characteristic, transconductance, output-conductance and capacitances can be obtained. It is also computationally efficient as it uses very few model parameters. The other main features include non-uniform substrate doping profile, Mobility reduction due to vertical field, Carrier velocity saturation and short and narrow-channel effects.

In all the approaches mentioned above, attempts have been made to include the Quantum Mechanical Effects in the MOSFET models. But most of the models that have come up are either empirical or semi empirical in nature. Therefore, there is a need for more physics based approach to accurately explain the behavior of the device, which takes into account the Quantum Mechanical Effects in all the regions of operation.

It is therefore, clear that there is a need for developing suitable device models to account for Quantum Mechanical Effects occurring at sub 100nm Gate lengths.

1.4 COMPARISON OF VARIOUS MOSFET MODELS

Table 1.1 shows the comparison summary of some of the advanced models discussed above. The table clearly shows that though most of the industry standard models include the Quantum Mechanical Effects, yet these models are not capable of predicting the complete model at the sub 100nm. This is because the models include Quantum Mechanical Effects empirically or semi-empirically.
Table 1.1: Comparison of Various Compact MOSFET Models

<table>
<thead>
<tr>
<th>PROPERTY</th>
<th>BSIM4</th>
<th>BSIM5</th>
<th>MM9</th>
<th>EKV</th>
<th>SP</th>
</tr>
</thead>
<tbody>
<tr>
<td>Modeling Method</td>
<td>Analytical</td>
<td>Analytical</td>
<td>Analytical</td>
<td>Analytical</td>
<td>Analytical</td>
</tr>
<tr>
<td>Channel Inversion Voltage-based</td>
<td>Threshold Voltage-based</td>
<td>Threshold Voltage-based</td>
<td>Both Surface Potential and Threshold Voltage-based</td>
<td>Surface Potential-based</td>
<td></td>
</tr>
<tr>
<td>Model Core Reference</td>
<td>Source</td>
<td>Source</td>
<td>Source</td>
<td>Bulk</td>
<td>Bulk</td>
</tr>
<tr>
<td>Quantum Mechanical Effects</td>
<td>Yes, An empirical Inclusion of effective Gate oxide</td>
<td>Yes, Based on the correction of surface Potential</td>
<td>No</td>
<td>Yes Linearization of band gap widening with the charge</td>
<td>Yes Linearization of band gap widening with the surface potential</td>
</tr>
</tbody>
</table>


1.5 QUANTUM MECHANICAL EFFECTS

The major effects occurring in a MOSFET at deep sub-micron and the nanometer scales which are to be modeled in this work are:

1. The Quantum Mechanical tunneling from source to drain in the channel at sub 10nm
2. The Quantum Mechanical tunneling from source to ultra thin Gate Oxide
3. The Quantization of the Energy bands in the channel
4. Displacement of inversion charge density into the bulk
5. Poly-Silicon Gate depletion and Poly-Silicon Gate Quantization
6. Threshold Voltage and Drain saturation voltage shift

1.5.1 The Quantum Mechanical Tunneling from Source to Drain in the Substrate

In sub 10nm channel length, the charge carriers are no longer restricted in the source potential well but start tunneling Quantum Mechanically through the barrier between the Source and Drain [23]. So, the Gate voltage has no control over the MOSFET operation. This process is very important to model so as to continue with the scaling down process beyond 10nm Gate lengths.

1.5.2 The Quantum Mechanical Tunneling from Source to Gate oxide

Due to aggressive technology scaling, the Gate oxide thickness will be only around 2 nm in nanometer scale devices and thus called as ultra thin oxides. In the ultra thin oxide MOSFETs, the electrical field will be very high. Hence, the charge carriers in the channel will directly tunnel through the interface barrier to the Gate oxide [24, 25]. The tunneling into the Gate oxide is Quantum Mechanical in nature and needs to be properly modeled in the overall MOSFET behavior.

1.5.3 Energy Quantization in the Substrate

As the MOSFET dimensions approach deep sub-micron and nanometer regions, the classical movement of the charge carriers is greatly affected by the non-classical behavior of electrons in the MOSFET. Due to aggressive scaling of the MOSFETs, the Gate oxides are also scaled to nanometer regions. Also, the substrate doping is increased tremendously to negate the short channel effects at the deep sub-micrometer or nanometer scales. This results in very high electric fields in the Silicon/Silicon Oxide interface and hence the potential at the interface becomes steep. This results in a potential
well between the oxide field and the silicon potentials. During the inversion condition, the electrons are confined in this potential well. Due to confinement, the electron energies are quantized and hence the electrons occupy only the discrete energy levels. This results in the electrons residing in some discrete energy levels which are above the classical energy level by some fixed value of energy as shown in Figure 1.3.

![Energy Quantization in the Substrate](image1.3.png)

**Fig. 1.3: Energy Quantization in the Substrate**

**1.5.4 Displacement of inversion charge density into the bulk**

Due to Energy Quantization, charge carrier density at the surface becomes less than the one expected from the classical analysis. This is more important as the oxide thickness becomes smaller with each technology generation.

![Electron Concentration Distribution in the Silicon Substrate in Classical and Quantum Mechanical Cases](image1.4.png)

**Fig. 1.4: Electron Concentration Distribution in the Silicon Substrate in Classical and Quantum Mechanical Cases**
The charge distribution in case of classical charge distribution and Quantum Mechanical Charge distribution is shown in Figure 1.4. The charge displacement in the bulk needs to be analytically modeled

1.5.4 Poly-Silicon Gate Depletion and Poly-Silicon Gate Energy Quantization

The depletion in the Poly-Silicon Gate will cause a change in the effective oxide thickness and hence the effective Gate Capacitance [26]. The depletion region at the oxide/Gate interface is also of Quantum Mechanical in nature and here also, the energy bands are split up or Quantized [27].

1.5.5 Threshold Voltage and Drain Saturation Voltage shift

The shift in the surface potential due to the Quantum Mechanical Effects changes the threshold voltage as the effective oxide thickness increases. Operating the MOSFET at such a low dimension will cause Energy Quantization in the oxide/substrate interface and also at the Oxide/ Poly-Silicon Gate interface. The confining of the charged carriers in the potential well will raise the energy of the electrons because of the Quantization of energy and electrons will occupy much higher energy levels for which a different potential is required to turn on the transistor. So the threshold voltage needs to be calculated in an entirely new manner to take care of these effects.

The Energy Quantization process will decrease the drain current also. The drain to source saturation voltage will fall under such conditions. So, it needs to be modeled.

It is therefore, important to account for the Quantum-Mechanical Effects in the design of nanometer scale MOSFETs. In this region, classical models are inadequate and lead to erroneous and misleading predictions of critical electrical behavior parameters, such as, the physical oxide thickness, threshold voltage, drive current, Gate Capacitance, etc.
1.6 QUANTUM MECHANICAL MOSFET MODELING APPROACHES

Accurate modeling of Energy Quantization in MOSFETs requires the solution of the Schrödinger and Poisson equations. One of the approaches to model the Quantum Mechanical problem is use approximations in solving these equations. These equations upon solving give the energies and the surface potentials which are caused by the Energy Quantization process in the substrate. These are then used to obtain the inversion charge densities further giving the accurate analytical equations for C-V and I-V analysis in sub 100nm MOSFETs. Furthermore, analytical solutions are preferable because of their simplicity and fast computational speed. With these analytical solutions, it becomes easier to predict device scalability and circuit performance for future technology generations.

The other approach to tackle Energy Quantization problem is the numerical approach which deals with the actual self-consistent solution (i.e. compatible to a large extent with the solution of each other or with a minimum error in solution matching) of the Poisson's and the Schrödinger's equations. These can be solved in both one dimension and two dimensions.

The one-dimensional modeling primarily involves the analysis of the Quantization of the energy levels and the variation of the surface potential only in the transverse direction i.e. along the depth of the channel or normal to the oxide/silicon interface. In this, the Poisson's and the Schrödinger's equations are solved only in one dimension. Traditional modeling approaches have been of one dimension self-consistent solving of Poisson's - Schrödinger's equations. This type of modeling approach is not sufficient to analyze the MOSFET at high drain voltages at which the two dimensional short channel effects such as drain induced barrier lowering etc. are prominent. Only very low drain voltages analysis can be done using one dimension modeling [28].

The two-dimensional modeling approach which is more complex, considers the Quantization of the energy levels and the variation of the potential in the transverse as well as in the longitudinal directions. In this,
the Poisson’s and the Schrödinger’s equations are solved in the direction normal to the oxide/silicon interface and also along the channel. Numerical solutions are obtained by solving Schrödinger equation and the Poisson equation using iterations. It is not used as an approach in standard circuit simulators because of its complexity and more computationally intensive due to iterative solutions but used as a reference because of its high accuracy.

As far as Quantum Mechanical oxide tunneling is concerned, the models available are either complex, numerical or lack theoretical details. The Quantum Mechanical direct source to drain tunneling in effective in sub-10nm MOSFETs has never been modeled analytically previously as per the standard literature available. So, far only numerical models are available.

1.7 SCOPE AND ORGANIZATION

The Quantum Mechanical Effects are a big obstacle in the scaling down of the MOSFETs. Therefore, it is critical to analyze them analytically so that the possible solutions may be given to assist in the scaling down of the MOSFETs to nanoscale. The model developed in the thesis provides an idea how a nanoscaled MOSFET would perform under the influence of QMEs.

The thesis is organized into five chapters. Each chapter is independent and gives full justification to the development of the model based on the Quantum Mechanical Effects.

Chapter 2 is divided into various sections and sub sections. Section 2.1 introduces the basic theory of tunneling through Gate oxides including Fowler Nordhiem and Direct tunneling and its implication over the MOSFET performance. In Section 2.2, various existing tunneling models and the Gate tunneling effect (Electron and Hole) on a MOSFET. The Gate tunneling equations are derived from the solution of the Schrödinger equation using the Wentzel-Krammers-Brillouin (WKB) approach is estimated using analytical model. In Section 2.3, the tunneling currents in case of Poly Silicon Gate depletion and without Poly Silicon Gate depletion are compared. Section 2.4 examines the tunneling current in a MOSFET with a high-
permittivity Gate dielectric expected to be used in future technology generations. The conclusion is given in Section 2.5.

The Chapter 3 is organized as sections and sub sections. Section 3.1 deals with the detailed description of Energy Quantization and the models available in the literature. Section 3.2 deals with the two approaches namely Triangular well approach and the Variation approach to solve the Schrödinger’s equation, inclusion of the shift in the surface potential due to Quantum Mechanical approach in explicit surface potentials and the comparisons drawn to conclude the approach best suited for describing the Energy Quantization Effects in the MOSFET. In Section 3.3, the entire Quantum Mechanical problem has been revisited in view of the Poly Silicon Gate depletion. Next section 3.4 deals with increased complexity in the Poly-Silicon Gate by considering Energy Quantization in it also and then reviewing the effect on the Quantum Mechanical surface potentials and the inversion charge densities in the substrate. Section 3.5 deals with analytical modeling of the inversion layer Centroid. Section 3.6 concludes the chapter.

Chapter 4 has been divided as follows: Section 4.1 describes the C-V analysis in the presence of charge inversion and Energy Quantization in the Substrate. In Section 4.2 C-V analysis has been done in the presence of Poly-Silicon Gate Depletion and Energy Quantization in the substrate. In section 4.3, the Threshold voltage model for the MOSFET has been developed. Section 4.4 describes the Drain voltage and Drain current analysis of the MOSFET at 80nm channel length using the charge sheet model approximations. Some short-channel effects have also been taken. Section 4.5 deals with the saturated drain voltage model at the nano meter scale. Section 4.6 deals with the use of strained silicon technology in 80nm channel length MOSFETs. Conclusion is given in section 4.7.

Chapter 5 has been organized in following sections and sub sections:-

Section 5.1 describes the basic existing models and the physics of tunneling to study Quantum Mechanical tunneling from source to drain. Section 5.2 describes the concept of tunneling including DIBL. In Section 5.3, the tunneling current density is found in the presence of drain voltage
using the WKB analysis. In Section 5.4, tunneling current density is found in the presence of drain voltage and the Gate voltage and including the Energy Quantization. Section 5.5 explains the Band Gap Narrowing Effect. Section 5.6 gives the conclusion of the chapter.

Chapter 6 summarizes the findings of this research and suggests possible areas for further investigation.