7.1 INTRODUCTION

The total system has been designed to comprise of the following blocks -

1) Twelve units of Intelligent local seismic networks (ILSNs) deployed all over the Indian subcontinent at different places as mentioned earlier.

2) National seismic data centre (NSDC).

3) Satellite based communication links between each ILSN and NSDC.

4) Voice data communication link between ILSNs and NSDC.

Hardware configuration of a single "Intelligent local seismic network array" (ILSN) has been shown in fig.(7.1). All the twelve ILSNs are identical in composition and in their function. Each ILSN has been designed around the following sub systems.

(i) One intelligent base station.

(ii) Eight number of identical remote seismic stations (RSS) installed over an area of 10,000 sq km approximately.

(iii) Eight Digital radio telemetry links between Base-station and each remote seismic station.

The intelligent base station has been designed around the following building blocks.

(i) IBM compatible simple PC/XT alongwith Hard disk and
FIG. 7.1
other standard peripherals.

(ii) Intelligent Front End Hardware (IFEH) module.

(iii) Interface controller (IC) module.

(iv) Interfaces between- a) PC/XT and IFEH module b) PC/XT and IC module and c) PC/XT and satellite.

(v) Seismic timing clock capable of being synchronized with ATA time reference signal transmitted by NPL-New Delhi.

7.2 SEISMIC REMOTE STATION OF AN ILSN

All the eight seismic remote stations of every one ILSN are identical in composition and operation. Each remote
station has been designed around the following main components as shown in the fig.(7.2).

(i) 3- components short period seismometers.
(ii) Analog processor card.
(iii) digital processor card.
(iv) Transmitter set alongwith antenna.
(v) Rechargable batteries and solar power panel.

7.2.1. Analog processor card

It consists of three identical signal conditioner circuit blocks as shown in fig. (7.2). One block serves exclusively to one seismometer only. The signal conditioner consists of -a) preamplifier, b) programmable filters and, c) a gain ranging amplifier. The gain ranging amplifier is controlled by the digital processor card which selects any one of the four channels of analog multiplexor switch (for the change of feedback resistance used in the amplifier) in accordance with the input signal received from the seismometer. All the components incorporated on this card are C-MOS Technology based.

7.2.2. Digital processor card

It comprises of a three channels multiplexor, 12 bit analog to digital converter and fairly complex combinational logic circuits as shown in fig. (7.2). It does the following - a) realization of SYNCH- WORD, b) data formatter, c) data serializer, d) generation of stable system clock at a rate of 4800 Hz per second, e) auto gain ranging, and f) control logic for the over all coordinated function of the remote
station.

The serialized output of the card is fed to the transmitter to produce the radiated output. All the components mounted on the card are C-MOS technology based.

7.3. INTELLIGENT BASE STATION OF AN ILSN

One complete intelligent seismic local network comprises of only one Base station (BS) whereas the remote stations (RS) in it are eight in number. The base station which is the heart of the local network is shown in the in the fig.(7.3). It has been designed around a simple PC/XT and some specially designed electronic modules which are -

a) Intelligent Front End Hardware (IFEH) module,
b) Intelligent controller module, and
c) Interfaces cards.

![System Integration of Base Station Diagram](image-url)
7.3.1 Intelligent front end hardware module (IFEH)

The IFEH module contains eight identical processor cards. Each processor card is dedicated exclusively to only one remote station via receiver set for receiving the digital data transmitted from it as shown in the fig.(7.1).

Each processor card has been provided with "Data recovery logic" circuit as shown in the fig.(7.4) to decode the transmitted serial digital data back into the same form as it has been produced by the "Data Formatter" which is the part of every remote station.

Each Processor card as shown in the fig.(7.5), has been designed around Intel 8085 microprocessor and its compatible programmable input/output devices.
It has been provided with 24 k byte of storage. Out of this, 20 k byte is RAM which is used for storing - a) programmable length of Pre-event data, b) values of programmable variables for computation of trigger algorithm, c) clock data and header information, d) intermediate processing results, and e) some FLAGS set either initially or subsequently as and when need arises. The remaining 4 k byte is EPROM which has been used to store the "System software" developed to carry out the desired functions.

Three pieces of Intel 8255 (programmable peripheral input/output devices) have also been incorporated on the processor card to manage the bidirectional flow of the data/commands. For this purpose the different ports of these devices have been arranged as output ports and input ports as explained and described under "Software design".

Logic "AND" gates designated as "L" and "N" have been incorporated to enable a set of pulses issued by the "Data recovery logic" and "Seismic clock" to interrupt the microprocessor at RST-7.5 and RST-6.5 respectively. The interrupt RST-6.5 has been used to store the clock data into the processor memory after every one second. The interrupt at RST-7.5 has been used to take in and store the data sample (16 bits) which is received after every 3.3 mili seconds from the remote station. Whereas "OR" gate designated as "Z" permits the interrupt pulses which are meant either for "Programming the variables for remote stations" or for "Verification of the programmed data" to interrupt the microprocessor at RST-5.5.
7.3.2 Interface controller module (IC)

Unlike the IFEH module, the IC module contains only a single processor card designed around Intel 8085 microprocessor and its compatible devices as shown in the fig.(7.6).

This card consists of 24 k bytes of memory storage. Out of this, 20 k byte is RAM which is used to store the data of 4 seconds duration received from all the remote station. This data for all the eight remote stations is of the order of 19.2 k bytes. The remaining 800 bytes are used for storing intermediate results and some flags. The remaining 4 k bytes is the EPROM mounted on the card to store "Operational Software".

Logic designated as "M" shown in the fig.(7.6), has been incorporated to enable the pulses from the processor cards to interrupt the micro processor at RST-7.5. The micro processor of Interface controller can be interrupted at its RST-7.5 only when there is no true event detected at network level. When the interrupt pulse is received through this logic, the microprocessor is interrupted and only one of the two unique codes, is sent to the memory of IC module by each processor card. These codes sent by all eight processor cards of the IFEH module, are processed further by the IC module to find out the occurrence of true event at local network level. Similarly a logic "X" has been incorporated for enabling a pulse to interrupt the micro processor at RST-6.5 for taking in the fresh data samples (one from each
card) after every 3.3 milli seconds from the circular memory of each processor card. This process of lifting data from all eight processor cards is enabled only after the detection of true event. This process is continued till the acquisition of data pertaining to Pre-event and Post-event is not over.

Three 8255s (PPI) of M/s Intel have been incorporated to control the bidirectional flow of data/commands. The identification of various ports of these devices as output ports and input ports has been done as per worked out design. It has been described under "Software design". (Chapter-8).

7.4. PC/XT- INTERFACES CARDS

Two electronic cards have been designed for this purpose i.e.

a) Card for interfacing PC/XT with IC and IFEH modules

This card shown in the fig.(7.7) basically comprises of two intel 8255- PPIs. It has been designed as a "Plug in card" fitted in the additional slot of PC/XT. All the ports of these devices have been programmed as per design requirement. This arrangement of port assignment has been explained in detail under "Software design". (Chapter-8) This card through identified ports establishes bidirectional flow of data/commands in either direction sometime between PC/XT and IFEH module and sometime also between PC/XT and IC module as per functional requirement.
b) Card for interfacing PC/XT with satellite

This card comprises of combinational logic circuits for receiving

commands from PC/XT about the status of network in regard with whether event is running or not etc.

7.5. SEISMIC TIMING CLOCK

The clock has been realized around a stable crystal and combinational logic circuits as shown in the fig.(7.8).
The clock produces timing in BCD form after every second. One byte contains information on second. The next byte which is made available on the data output port just after 200 microsecond from the previous byte, contains the information on minute and so on. The clock module has been provided with the logic circuit required to synchronize the clock with the ATA time reference signal transmitted by National Physical Laboratioy (NPL)-New Delhi. Also, there is a logic circuit to produce a burst of five pulses after every second in coordination with the timing information available in five bytes. The burst acts as the interrupt pulses at RST-7.5 of IC module as explained earlier.