CHAPTER - III

RC OSCILLATORS WITH GROUNDED CAPACITORS [56][57]

3.1 Introduction:

Sinusoidal oscillators play an essential role in most of the existing electronic systems. These oscillators are used in communication, instrumentation, biomedical instruments etc. The conventional Wein bridge oscillator [10] uses one operational amplifier in conjunction with two capacitors, of which one is ungrounded. The conventional quadrature oscillator circuit [8], uses two operational amplifiers in conjunction with three capacitors, out of which two are ungrounded. Although these networks are uncomplicated, the approach can be troublesome if a very large time constant is needed. Section 3.2 of the present chapter describes a quadrature oscillator and 3.3 an ultra low distortion oscillator. In the configuration presented, the timing components are scaled by a resistance ratio, so it is easy to obtain long time periods. Besides this the circuit offers some additional advantages because of grounded capacitors [66]. In hybrid IC technology thin-film techniques are used for fabricating frequency selective components in which case, it is desirable to have all the capacitors grounded. The grounding of the capacitor eliminates the etching process and reduces the number of gold contacts and thereby increases the circuit reliability. The use of voltage
variables resistor for controlling the frequency is an attractive feature for many applications. The requirement of an additional op. amp. in the present configuration is not a disadvantage because it does not significantly increase the cost in these days of large and very large scale integration.

The intersil 8038 integrated function generator is useful for realizing a voltage-controlled oscillator with a sinewave output, because of its wider sweep capability. But because of the limitations of the 8038's integrated current sources, its frequency versus voltage characteristics is nonlinear over a considerable part of its sweep range. The VCO based on field effect transistors suffers from harmonic distortion and nonlinearity in voltage-to-frequency conversion limitations inherent in FETs.

Section 3.4 of the present chapter describes a sinusoidal oscillator where frequency of oscillation is scaled by a parameter $K$ which bears a linear relation with the controlling voltage $V_x$. Thus the oscillator results in a linear voltage-to-frequency converter with sinewave output. The basic oscillator circuit is realized with operational amplifiers (op. amps) and four quadrant analog multipliers (AMs) in conjunction with an RC network in which all capacitors are grounded. The positive and negative feedback path of the basic configuration are carefully balanced to attain and sustain low distortion operation. The balance is achieved by use of some type of Automatic gain control (AGC) arrangement. Here the mechanism is an AM, which maintains desired gain to constrain the natural
frequencies of the circuit on the imaginary axis of the complex frequency plane (s-plane).

3.2 Quadrature oscillators with extended time period:

3.2.1 Basic configuration:

Consider the configuration Fig. 3.1 which yields the following second order transfer function:

\[ \frac{V_o(s)}{V_i(s)} = \frac{K_x K_y}{m T_1 T_2 s^2 + (a - K_x K_y) m T_2 s - K_x K_0} \]  \hspace{1cm} \text{(3.1)}

Let \( K_x K_0 = -b^2 \) where \( b \) is a real constant. For sustained oscillations the denominator of (3.1) will be zero, if the input \( V_i \) is grounded and the damping is set to zero i.e.,

\[ \begin{align*}
V_i(s) &= 0 \\
K_x K_y &= a
\end{align*} \hspace{1cm} \text{(3.2)}

The denominator of (3.1) reduces to the form

\[ m T_1 T_2 s^2 + b^2 = 0 \]  \hspace{1cm} \text{(3.3)}

From (3.3) the frequency of oscillation is given by

\[ \omega_0 = \frac{b}{\sqrt{(m T_1 T_2)}} \]  \hspace{1cm} \text{(3.4)}

The output \( V_o \) will be in quadrature with \( V_y \). The frequency of oscillation can be controlled by varying \( m \) or \( K_0 \), keeping \( T_1 \) and \( T_2 \) invariant. The configuration of Fig. 3.1 will be realized with
the following consideration:

Case 1 $K_x > 0$, $K_y > 0$, $K_0 < 0$

Case 2 $K_x < 0$, $K_y < 0$, $K_0 > 0$

3.2 Basic Building Blocks

(a) Integrator

Consider the network of fig. 3.2 which realizes an integrator whose input - output relations are given by

$$V_u(t) = \frac{1}{mT_s} V_y(t) \quad \ldots \ldots (3.5)$$

Provided

$$1 \left( A + R_0 \right) = 1 + \frac{R_0}{R} \quad \ldots \ldots (3.6)$$

A straight-forward analysis of fig. 3.2 yields

$$m = \left( 1 + n \right) \left( A + \frac{R_e}{R_0} \right) \left( 1 + \frac{R_0}{R_e + R_d} \right) \quad \ldots \ldots (3.7)$$

If one assumes that

$$A \gg (1 + R_d/R_e) \quad \ldots \ldots (3.8)$$

then from (3.1) one gets

$$R_d/R_e \gg R_0 \quad \ldots \ldots (3.9)$$

Inspection of (3.7) shows that the multiplicative constant $m$ can be controlled by a single resistance $nR$. Choosing $nR \gg R_0$, one can see that the scale factor $m$ can be made very high. Thus the capacitance required will be of low value even for higher value.
of mT. For example, mT = 10 ms. requires C = 1000 pF with
R = nR = 10k and Ro = 10

The requirement of low value grounded capacitor is a desir­
able feature for monolithic IC fabrication

(b) First-order network

The network of Fig 3.3 (a) realizes

\[ K_X V_X(s) = \frac{1}{1 + sT_X} V_Y(s) \quad \text{...... (3.10)} \]

where

\[ T_X = R_C C_X \]

Considering the network of Fig 3.3 (b) one gets the following relations.

\[ V_X(s) = -\left( \frac{2 + A}{A} \right) C_X R_1 V_Y(s) \left[ \frac{2 + A}{A} + \frac{(1 + A) R_1}{R_3} \right] \quad \text{...... (3.11)} \]

If it is assumed that A \(\gg\) 2, then (3.11) reduces to

\[ V_X(s) = - (T_X + a) V_Y(s) \quad \text{...... (3.12)} \]

where

\[ T_X = C_X R_1, \quad a = (1 + R_1/R_3) \quad \text{...... (3.13)} \]

3.3 Summer

Consider the network of Fig 3.4 which yields

\[ V_X(s) = K_b V_Y(s) + K_a V_Y(s) + K_f V_Y(s) \quad \text{...... (3.14)} \]

one can easily find

\[ K_b = \frac{R_b}{R_o} \left( \frac{R_o + R_1}{R_o + R_3} \right), \quad K_a = \frac{R_a}{R_o} \left( \frac{R_o + R_1}{R_o + R_3} \right), \quad K_f = \frac{-R_f}{R_o} \quad \text{...... (3.15)} \]

3.2.3 Realization and design of oscillator

(a) Case II \( K_1 = K'_b, K'_a, K_0 = K_f \)
With the above assignments, the oscillator is realized as shown in Fig 3.5. In this circuit \( a = 1 \) and \( K_x \) is chosen to be unity. From (3.2) one requires that \( K_y = 1 \). For simplicity open can choose \( K_o = 1 \). These gain requirements can easily be obtained by choosing \( R_a = R_b = R_c = R_i \).

A practical oscillator was designed and fabricated with the following element values:

\[ C_1 = C_2 = 1000 \text{ p.F}, \quad R_1 = R_z = 10 \text{ k}\Omega, \]
\[ R_0 = 10 \text{ \Omega}, \quad R_c = 9.8 \text{ k}\Omega, \quad R_o = R_0 = 10 \text{ k}\Omega. \]

(Operational amplifiers used as CA741CT)

The frequency of oscillations was controlled by a single resistance \( nR_2 \). Frequency versus \( nR_2 \) is plotted and shown in Fig 3.6

(b) Case 2

\[ K_y = K_0, \quad K_o = K_n, \quad K_i = K_b \]

With this choice, the oscillator is realized as shown in Fig 3.7. In this network \( K_x = -1 \) and \( a = 1 + R_y/R_x \), then \( K_y = -2 \) which requires that \( R_f = 2R_c \). Here

\[ b^4 = -K_oK_x = \frac{3R_o}{R_o + R_b} \]

Since \( R_o \) is grounded, it will be convenient to use this resistance for controlling the frequency. A practical circuit was designed and fabricated with the following element values:

\[ R_b = R_1 = R_2 = R_3 = R_c = 10 \text{ k}\Omega, \quad R_t = 20 \text{ k}\Omega + 100 \text{ \Omega}, \]
\[ R_o = 10 \text{ \Omega}, \quad C_1 = 1000 \text{ p.F}, \quad C_2 = 220 \text{ p.F}. \]
The frequency was controlled by $R_a$. The experimental results are shown in Fig 3.8.

A voltage controlled oscillator (VCO) can easily be realized from the configuration of Fig. 3.7. This can be achieved by replacing the resistor $R_a$ by a FET as a voltage variable resistor.

### 3.2.4 Temperature compensation:

In monolithic or hybrid IC-fabrication, the resistor ratios are relatively independent of temperature. The frequency drift with respect to temperature can be expressed as

$$\frac{\Delta \omega_o}{\omega_o} = \sum_{i=1}^{2} S_{R_i} \frac{\Delta R_i}{R_i} + \sum_{j=1}^{2} S_{C_j} \frac{\Delta C_j}{C_j} \hspace{1cm}(3.16)$$

It can be assumed that in monolithic or hybrid IC technology, all the resistances and capacitances will have the same temperature coefficient. That is

$$\frac{\Delta R_i}{R_i} = \frac{\Delta R}{R}, \hspace{1cm} i = 1, 2 \hspace{1cm} \text{and} \hspace{1cm} \frac{\Delta C_j}{C_j} = \frac{\Delta C}{C}, \hspace{1cm} j = 1, 2 \hspace{1cm}(3.17)$$

Then

$$\frac{\Delta \omega_o}{\omega_o} = \frac{\Delta \omega}{\omega} \sum_{i=1}^{2} S_{R_i} \omega + \frac{\Delta C}{C} \sum_{j=1}^{2} S_{C_j} \omega \omega_o \hspace{1cm}(3.18)$$
Also it can be shown that

$$\sum_{i=1}^{2} \varepsilon_{R_i} \tau_{s} = \sum_{j=1}^{2} \varepsilon_{C_j} \tau_{s} = -1 \quad \ldots \ldots (3.19)$$

Then

$$\frac{\Delta \omega_0}{\omega_0} = \frac{\Delta R}{R} + \frac{\Delta C}{C} \quad \ldots \ldots (3.20)$$

In thin-film technology, it is possible to realize resistors having temperature coefficient equal but opposite to that of capacitors. Then (3.20) reduces to $[29] \ [32]$

$$\frac{\Delta \omega_0}{\omega_0} = 0 \quad \ldots \ldots (3.21)$$

Thus with hybrid IC technology, the effect of temperature on the frequency of oscillation can be compensated.

3.2.5 Quadrature error

It is obvious that $V_y$ will be in quadrature with $V_0$ if the integrator remains ideal at all frequencies. Unfortunately, the situation is not so simple because of the finite gain-bandwidth product of the practical operational amplifier. The gain of an operational amplifier can be expressed as

$$A = \frac{A_p}{s + \frac{P_0}{A_p}} \quad \ldots \ldots (3.22)$$
where $s$ is the complex frequency, $A_0$ is the DC gain and $P_0$ is the band width of the operational amplifier. Using the above gain expression it is possible to get the following relations.

\[
\frac{V_o}{V_T} = \delta s \left[ \frac{mT\delta s}{A_0P_0} + \frac{mT\delta}{1 + \delta} + \frac{1 + \delta}{A_0P_0} \right]
\]

where $\delta = R_0/R$. In deducing the above expression it is assumed that $A_0 \gg (1 + \delta)$.

The frequency response will be obtained by substituting $s = j\omega_0$ in the above expression. Thus the quadrature error can be obtained as

\[
\epsilon = -\tan^{-1} \frac{mT\delta (1 + \delta)}{A_0P_0mT\delta + (1 + \delta)^2}
\]

which indicates that the quadrature error depends upon the gain-bandwidth product of the operational amplifier. The error decreases with the increase of $A_0P_0$. Thus an amplifier having large gain-bandwidth product will be suitable for high frequency operation. The experimental results, as shown in Fig 3.6 and Fig 3.8, were obtained with CA741CT. The error is less than 0.6% over a frequency range of 10 kHz. It is obvious that the error can be reduced by selecting an operational amplifier having $A_0P_0$ larger than that of CA741CT.

3.2.6 Amplitude stability

Like other sine wave oscillators the amplitude varies with
the variation of frequency. The amplitude variations of the present oscillators are shown in Fig 3.6 and Fig 3.8. The percentage variation is calculated with respect to amplitude at 1 kHz.

A good amplitude stability can be obtained by incorporating an automatic gain control (AGC) unit as shown in Fig 3.9. In the AGC circuit, the mechanism is the variable channel resistance of the FET. The feedback signal is obtained by rectifying and filtering the output signal. The output voltage is regulated by adjusting the current through $R_z$. Thus $R_z$ and $V_f$ serve the purpose of reference. The AGC loop tracks this reference to maintain the output peak voltage at a constant level.

Note that the oscillation condition, in this case, will be given by

$$K_x K_y \left(1 + \frac{RF}{RD_S}\right) = a \quad \ldots \ldots \ldots (3.25)$$

here $RD_S$ is the drain-source resistance of the FET.

All other equations will remain the same as that of the basic configuration. Thus the design procedure will remain unaltered. With this modified circuit it is possible to get an amplitude variation of less than 0.1%

3.3 Low distortion sinusoidal oscillator

This section presents a configuration which makes it easy
to obtain a tunable oscillator with ultra-low distortion output. The frequency of oscillation can be controlled by a single resistor.

3.3.1 The Oscillator Circuits

Consider the general feedback configuration of Fig 3.10 which yields the following transfer function:

$$\frac{V_0(s)}{V_1(s)} = \frac{mK_0 K_1 \omega_0^2}{s^2 + s(2 - \omega_1 K_1) \omega_0 + (1 - K_1 \omega_1 + m_0 K_0 K_1 \omega_0^2)}$$  \hspace{1cm} (3.26)

with $m_1 K_1 = 2$

the natural frequencies of (3.26) are obtained on jw-axis. As these are the short circuit natural frequencies, they will be physically realized if $V_1 = 0$. Thus the frequency of oscillation becomes

$$\omega_0 = \omega_0 \quad m_0 K_0 K_1 = 1 \quad \ldots \ldots \quad (3.27)$$

The experimental result is shown in Fig 3.12. The following observations can be made from the experimental results:

1. The amplitude of oscillation remains fairly constant at low frequencies. At higher frequencies the amplitude variation increases as indicated in Fig 3.12.

2. The harmonic distortion is less than 0.02% at lower frequencies and it increases significantly as frequency exceeds 1 KHz.
The above discrepancies are due to the fact that the required loop gain as given in (3.27) is not maintained at higher frequencies because the op. amp. gains are frequency dependent. As in other sinewave oscillators, the positive and negative feedback paths must be carefully balanced to attain low distortion sustained oscillations. The balance is achieved by use of automatic gain control arrangements discussed below. The oscillator with automatic gain control (AGC) arrangement is shown in fig. 3.13. In this AGC circuit the mechanism is the variable channel resistance of field-effect transistor (FET).

The AGC circuit comprises an integrator $A_4$ which filters and smoothens the rectified output to provide a dc control voltage for the gate of the FET. Low ripple on this control the output. The high dc gain of the integrator automatically adjusts the loop to the required d.c. bias for the FET inspite of parameter variations. A local feedback path around the FET is provided through $R_4$ and $R_5$ to reduce distortion drastically below that of straight forward connection. In operation, the total harmonic distortion at the output is of the order of 0.02%. The amplitude variation was found to be less than 0.1%. The basic configuration Fig. 3.10 is implemented as shown in Fig. 3.11 which yields the following relations:

$$w_0 = \frac{1}{RC_1} = \frac{1}{R_2C_2} \quad \ldots \ldots (3.28)$$

$$K_1 = 1, \quad K_0 = 1 + \frac{R_C}{R_p} \quad \ldots \ldots (3.29)$$

$$m_i = 1, \quad m_0 = m_1 = 2$$
The condition of (3.27) is found to be satisfied with the values assigned to $K_1$ and $m_1$ as given in (3.29). Consequently the frequency of oscillation becomes
\[ \omega_0 = \omega_0 \left[ 1 + \frac{2R_c}{R_p} \right]^{1/2} \] \hspace{1cm} (3.30)
which shows that the oscillator can be tuned to a desired frequency by varying the resistance ratio ($R_c/R_p$). Since $R_p$ is grounded, it will be convenient to vary $R_c$ for a desired frequency of oscillation.

A practical oscillator was fabricated and tested with the parameter values:

\begin{align*}
R_1 &= R_2 = R_a = R_b = R_c = 10 \text{ K} \\
C_1 &= C_2 = 0.01 \mu\text{F}
\end{align*}

and op. amps. CA 741

$R_p$ was varied to tune the oscillator at different frequencies.

### 3.4 Electronically Tunable RC Oscillator

#### 3.4.1 Basic Configuration

Consider the block diagram of Fig 3.14. The transfer function of the system is given by
\[ \frac{V_o(s)}{V_1(s)} = \frac{K_1 K_2}{s^2 T_1 T_2 + s (T_1 + T_2 - K_1 m_1 T_2) + K_1 m_1 - K_1 K_2 m_0} \] \hspace{1cm} (3.31)

The condition of oscillation is $V_1 = 0$ and
\[ K_1 m_1 = \frac{T_1 + T_2}{T_2} \] \hspace{1cm} (3.32)
The frequency of oscillation is given by
\[ w_0 = \left( \frac{1 - K_1 m_1 + K_2 m_0}{T_1 T_2} \right)^{1/2} \]  \hspace{1cm} \ldots \ldots (3.22)
from (3.31) and (3.32) if \( T_1 = T_2 = T \)

\[ w_0 = \frac{1}{T} \left( K_1 K_2 m_0 - 1 \right)^{1/2} \]  \hspace{1cm} \ldots \ldots (3.23)

where
\[ K_1 = \alpha_1 V_1, \quad K_2 = \alpha_2 V_1 \]  \hspace{1cm} \ldots \ldots (3.24)
so
\[ w_0 = \frac{1}{T} \left( \alpha_1 \alpha_2 V_1^2 - 1 \right) \]  \hspace{1cm} \ldots \ldots (3.25)

The frequency of oscillation can be varied by varying \( \alpha_1 \) and \( \alpha_2 \) are scale factors of multipliers.

Fig. 3.15 shows the circuit realization of Fig. 3.14. In reference to Fig. 3.15
\[ T_1 = R_1 C_1, \quad T_2 = R_2 C_2 \]  \hspace{1cm} \ldots \ldots (3.26)
\[ m_1 = \frac{R_b}{R_a R_b} \alpha_3 V_x \]  \hspace{1cm} \ldots \ldots (3.27)

3.4.2 Oscillator with AGC loop

An AGC loop is incorporated in the basic configuration as shown in Fig. 3.6. The AGC circuit involves a diode \( D_1 \) a capacitor \( C_0 \), resistances \( R_3 \) s and \( R_4 \) s in conjunction with two op. amps \( (A_4 \text{ and } A_5) \). \( A_4 \) in conjunction with \( R_3 \) and \( R_4 \) forms a difference amplifier and \( A_5 \) realizes a unity gain buffer. The diode \( D_1 \) rectifies the oscillator output and \( C_0 \) filters out the ripple. Because of high input impedance of the buffer \( C_0 \), even with low value, is capable
of rejecting the ripple to a high degree. The dc voltage $V_x$ which is fed by the AGC circuit to $AM_1$ is given by

$$V_x = \frac{R_3}{R_4} \left( V_R - V_m \right) \quad \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots (3.28)$$

where $V_m$ is the peak output voltage of the oscillator and $V_R$ is a reference voltage. The loop gain is automatically adjusted to the required d.c. level $V_x$ for $AM_1$ inspite of parameter variations. Thus reducing the distortion level. The AGC loop tracks the reference voltage $V_R$ to maintain the output voltage at nearly constant level.

3.4.3 Experimental Circuit;

A practical oscillator based on Fig. 3.16 is built using three operational multipliers (XR2208) and a quad op. amp. (LM324). Each of XR 2208 combines a four quadrant analog multiplier (AM) is a buffer circuit and an op. amp. in a monolithic IC-chip. The AM section is cascaded to the buffer to obtain very low output impedance. Three such XR 2208 chips are used for practical realization of $AM_1/A_1$, $AM_2/A_2$ and $AM_3/A_3$. The AGC loop involving $A_4$ and $A_5$ is realized by a dual op. amp. (LM747). The RC element values are chosen as $R_a = R_b = R_1 = R_2 = R_3 = R_4 = R = 10K$ \(C = C_0 = 0.01 \, \mu F\)

The reference voltage $V_R$ is set to +12V and the S.F $\alpha_1$
is adjusted so that the oscillator starts to oscillate with minimum harmonic distortion. It is then kept unchanged throughout the tuning process. The oscillator is tuned to different frequencies by controlling the voltage $V_T$. 
FIG. 3.1 BASIC CONFIGURATION

FIG. 3.2 NON INVERTING INTEGRATOR
FIG: 3.3 FIRST ORDER NETWORK
(a) NON INVERTING TYPE
(b) INVERTING TYPE

FIG: 3.4 SUMMER
FIG. 3.5 QUADRATURE OSCILLATOR CIRCUIT (CASE -1)
FIG 3.7 QUADRATURE OSCILLATOR CIRCUIT (CASE -2)
FIG 3.8

- Frequency Response
- Quadrature Error
- Amplitude Variation

- $nR_2 = 1\,k\Omega$
- $nR_2 = 10\,k\Omega$
FIG. 3.9 AUTOMATIC GAIN CONTROL UNIT
FIG. 3.10 BASIC CONFIGURATION

FIG. 3.11 IMPLEMENTATION OF BASIC CONFIGURATION
FIG. 3.12 FREQUENCY VERSUS \( R_p \)

- FREQUENCY RESPONSE
- AMPLITUDE RESPONSE WITH AGC
- AMPLITUDE RESPONSE WITHOUT AGC

\[ V_o \text{ (VOLTS)} \]

\[ \text{FREQUENCY (KHz)} \]
FIG. 3.13 OSCILLATOR WITH AGC

- Diagram of an oscillator circuit with AGC.
FIG. 3.14 BASIC CONFIGURATION
FIG. 3.15 RC OSCILLATOR CIRCUIT WITHOUT AGC
FIG. 3.16 OSCILLATOR CIRCUIT WITH AGC