ABSTRACT

Low power and low area are the two significant requirements of FIR filter used in wireless mobile communication systems and Digital Signal Processors. In the first paper the novel optimized FIR filter architecture called CSM (Constant Shift Method) is proposed. The proposed architecture will operate in different filter coefficient word length. This novel FIR filter can be efficiently implemented by using Binary Sub expression Elimination algorithm. The proposed architectures will be implemented and tested on Spartan 3, Field-Programmable Gate Array and synthesized using Xilinx ISE and ModelSim. The proposed schemes provide good area and power reduction compared to the existing FIR filter.

In the second paper, an architectural approach to the design of reconfigurable finite impulse response (FIR) filter is proposed. FIR digital filters are used in DSP by the virtue of its, linear phase, fewer finite precision error, stability and efficient implementation. The proposed architectures offer Low power and area reductions and are compared to the best existing reconfigurable FIR filter implementations in the literature. Also these proposed architectures have been synthesized, implemented and tested on Spartan-3 field-programmable gate array (FPGA). The results from the simulation and synthesis processes prove the efficiency of the proposed work.

In the third paper, another architectural approach to design High throughput and less delay reconfigurable finite impulse response (FIR) filter is proposed. New reconfigurable architectures of low complexity FIR filters are proposed, namely MCSD (Multiplier Control Signal Decision) window technique using Vedic multiplier. The proposed architectures offer delay reductions compared to the best existing reconfigurable FIR filter implementations in the literature. The proposed Schemes have been implemented and tested on Spartan-3 FPGA similar to the previous research work.
The fourth paper presents an architectural approach to the design of Low power and high speed Reconfigurable finite impulse response (FIR) filter. In this proposed architecture, a pipeline Technique to obtain high throughput and less delay to increase the performance of the FIR filter is introduced. The proposed architectures provide Low power and high speed compared to the best conventional reconfigurable FIR filter. Simulation, synthesis and implementation of the proposed architectures have been achieved and tested on Spartan-3 xc3s200-5pq208 field-programmable gate array (FPGA).

Keywords— Channelizer, high speed filter, Reconfigurability, binary sub expression elimination, MCSD (Multiplier Control Signal Decision window) technique.