4. TIQ Flash Analog to Digital Converter

4.1 Introduction

This chapter focuses on the proposed TIQ flash ADC which is the basic building block of the ADC including its major circuit components. Also important characteristics of the CMOS inverter [7] and its use in TIQ comparator are introduced for simulation and analysis of the TIQ flash ADC. A traditional n-bit flash ADC architecture uses $2^n$ resistors and $2^n-1$ comparators to convert an analog signal to digital. This architecture has drawbacks like large input signal driving, high reference accuracy, high driving reference voltage and circuit complexity [74] [75].

The proposed flash ADC features the threshold inverter quantization (TIQ) technique using CMOS inverters for high speed and low power using standard CMOS technology that is compatible with microprocessor fabrication. Figure 4.1 shows the block diagram of the TIQ flash ADC. The use of two cascading inverters as a voltage comparator is the reason for the technique's name [9]. The voltage comparators compare the input voltage with internal reference voltages, which are determined by the transistor sizes of the inverters. Hence, we do not need the resistor ladder circuit used in a conventional flash ADC. The CMOS inverters used play the role of resistor ladders and comparators thus saving most of the power of ADC.

![Figure 4.1 Block diagram of the TIQ flash ADC [9]](image)
The gain boosters make sharper thresholds for comparator outputs and provide full digital output voltage swing. The comparator outputs - the thermometer code - are converted to a binary code in two steps through the ‘01’ generator and the encoder as shown in figure 4.1. Thus a differential comparator is replaced by digital comparators for analog voltage switching.

4.2 TIQ Comparator

TIQ comparator comprises of two cascaded inverters. Advantage of low power consumption of CMOS inverter and considerable higher speed achieved by inverters is utilized here. The comparator is the most important component in the ADC architecture. Its role is to convert an input voltage \( V_{\text{in}} \) into a logic ‘1’ or ‘0’ by comparing a reference voltage \( V_{\text{ref}} \) with the \( V_{\text{in}} \). If \( V_{\text{in}} \) is greater than \( V_{\text{ref}} \), the output of the comparator is ‘1’, otherwise ‘0’. Commonly used comparator structures in CMOS ADC design are the fully differential latch comparator [3] and dynamic comparator [56] [70]. The former is sometimes called a “clocked comparator,” and the latter is called a “auto-zero comparator or chopper comparator.” To achieve high speed, such comparators are usually implemented with bipolar transistor technology. For SoC implementation in this case, BiCMOS technology would be necessary to integrate both a high speed ADC and a digital signal process on the same substrate. The TIQ comparator uses two cascading CMOS inverters as a comparator for high speed and low power consumption. Many researchers have used this TIQ comparator for implementing a high speed flash ADC [53]. The proposed TIQ comparator that is described in this thesis has been developed not only for higher speed but also for higher resolution.

4.2.1 Traditional comparator Vs TIQ comparator

![Comparison of Traditional and TIQ Comparator](image)

*Figure 4.2 The similarity and difference between differential input voltage [22]*
Figure 4.2 shows the similarity and difference between a differential input voltage comparator and an inverter based comparator. A CMOS inverter is a very basic and simplest possible circuit which can be replaced by resistor ladder and differential input voltage comparator. The inverter circuit is inherently faster than the differential input voltage comparator circuit. Advantages of using CMOS Inverter are [7]:

- Steady state Power dissipation of CMOS inverter is virtually negligible.
- VTC exhibits full output voltage swing between 0V to VDD.
- The VTC transition is usually very sharp.

In a conventional flash analog to digital converter, the differential input voltage comparators are used and the reference voltage $V_r$ is generated by the resistor ladder circuit. On the other hand, the TIQ technique uses a digital inverter circuit as a voltage comparator [12]. With the inverter comparator, the inverter switching threshold voltage $V_m$ is internal to the inverter, fixed by the transistor sizes [53]. The inverter switching threshold voltage $V_m$ is defined at $V_{in} = V_{out}$ point on the voltage transfer characteristic curve of an inverter as shown in figure 4.3.

![Figure 4.3 Two cascaded inverters as a TIQ comparator and its VTC Characteristics [12]](image)

We have obtained the equally spaced inverter switching threshold voltages between maximum $V_m$ (comparators 63 in case of 6 bit ADC) and minimum $V_m$ (comparator 1 in case of 6 bit ADC) by systematically changing the transistor sizes [22].

In a conventional flash analog to digital converter, the $2^n$ voltage comparators are identical, using the resistor ladder circuit to generate $2^n$ reference voltages to compare. In the TIQ based flash analog to digital converter, the $2^n$ voltage comparators are different and the $2^n$ reference voltages are built-in to the comparators. Designing the $2^n$ different voltage
comparators can be a difficult task; however, the authors were able to design and redesign many times without difficulty using the modern VLSI CAD tools.

The TIQ technique has many advantages:

- Simpler voltage comparator circuit.
- Faster voltage comparison speed.
- Elimination of resistor ladder circuit.
- Does not require switches, clock signal, or coupling capacitors for the voltage comparison.
- Suitable for the standard CMOS technology, ideal for the SOC implementation.
- Highly adaptable to future CMOS technology development, going to smaller feature size and lower supply voltage.

A programmable logic threshold inverter is also of interest in analog applications, to be used as a voltage comparator. Instead of using a whole analog block (as an A/D or opamp) to determine if a signal is above or below a given reference, the proposed variable logic threshold inverter can be programmed to a voltage being the reference voltage required for each application. The inverter has the advantage of a significant area reduction given its simplicity and the reduced number of transistors required. Additionally, a comparator requires two inputs, while a programmable logic threshold buffer used as a comparator would only require a single package pin [24].

4.2.2 Transistor sizing in CMOS

Transistor sizing is the operation of enlarging (or reducing) the width of the channel of a transistor. It is an effective technique to improve the delay of a CMOS circuit. When the width of the channel is increased, the current drive capability of the transistor increases which reduces the signal rise/fall times at the gate output. The active area, i.e., the area occupied by active devices (e.g., transistors) increases with increased transistor sizes, and the layout area may increase [12].

It is known that for a simple CMOS inverter, both the static and dynamic characteristics of the circuit are dependent on the transistor properties $\beta$ (transconductance) and threshold voltage $V_t$. It is therefore clear that designers must take care to control these parameters to ensure that circuits work well. In practice, there is only a limited amount of control available to the designer [5]. The threshold voltage cannot (or should not) be modified at will by the designer. $V_t$ is strongly dependent on the doping of the substrate material, the thickness of gate oxide and the potential in the substrate. The doping in the substrate and

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the oxide thickness are physical parameters that are determined by the process designers, hence the circuit designer is unable to modify them. The substrate potential can be varied at will by the designer, and this will influence $V_t$ via a mechanism called as body effect. It is unwise to tamper with the substrate potential and for digital design the bulk connection is always shorted to $V_{SS}$ for NMOS and $V_{DD}$ for NMOS.

For the equation of $\beta$ (transconductance) as mentioned in Equation 4.1:

$$\beta = \frac{\mu \varepsilon_{ox} W}{t_{ox} L}$$

(4.1)

Where $\mu = \text{carrier mobility (} \mu_n \text{ or } \mu_p\text{)}, \varepsilon_{ox} = \text{dielectric constant (which is a fixed physical parameter)}$ and $t_{ox} = \text{thickness of the oxide layer (which is set by process)}. W$ is the gate width and $L$ is the length.

From equation 4.1 we can see that the VLSI designer has no control over the pre-factor ($\mu \varepsilon_{ox}/t_{ox}$) since the carrier mobility ($\mu_n$ or $\mu_p$) is a fixed property of the semiconductor (affected by process), $\varepsilon_{ox}$ is a fixed physical parameter and $t_{ox}$ is set by process. The designer is therefore left with the two dimensional parameters $W$ and $L$. In principle both $W$ and $L$ can be varied at will by the chip designer, provided they stay within the design rules for the minimum size of any feature. However, the smaller the $L$, the larger the $\beta$ and smaller the gate capacitance, hence quicker the circuit, so with few exceptions designers always use the smallest possible $L$ available in the process. For example, in a 0.25µm process the gate length will be 0.25 µm for virtually every single transistor on the chip.

The PMOS/NMOS width ratio ($\beta$) and $W/L$ ratio of NMOS device is an important ratio in the design of digital logic cells using conventional CMOS logic design style. The appropriate selection of $W/L$ ratio of NMOS device and MOS/NMOS width ratio makes the digital design faster and reduces the power consumption [63].

To conclude, the only parameter that the circuit designer can manipulate at will is the transistor gate width $W$, and minimum value of $L$ is chosen keeping it constant.

### 4.2.3 Controlling threshold voltage in an inverter

The threshold voltage of a CMOS inverter is given by the equation 4.2 [68]:

$$V_t = V_{DD} \left(1 - \frac{t_{ox}}{d_{ox}}\right)$$

(4.2)
Where \( W_p = \) PMOS width, \( W_n = \) NMOS width, \( V_{DD} = \) supply voltage, \( V_{Tn} = \) NMOS threshold voltage, \( V_{Tp} = \) PMOS threshold voltage, \( \mu_n = \) electron mobility, \( \mu_p = \) hole mobility, assuming that PMOS length = NMOS length.

It has to be noted that the threshold voltage is very sensitive to \( V_{DD} \). For this reason considerable effort is expended in large designs in making sure that \( V_{DD} \) is same across the whole chip. This is not as simple as we are thinking, but in this discussion we will assume that \( V_{DD} \) is well controlled. We will also ignore the effect of variation in \( V_{Tp} \) and \( V_{Tn} \). In practice these values will vary between every transistor on a chip, but it is the job of the process manager to keep the spread in values to within acceptable tolerance. A designer should use the expected tolerance band to simulate best and worst case scenarios for a design but we will assume \( V_{Tp} \) and \( V_{Tn} \) as fixed values. We next consider the ratio \( \beta_n / \beta_p \).

The equation for \( \beta \) can be written for PMOS and NMOS as

\[
V_m = \frac{\mu_p W_p}{\mu_n W_n} \left( V_{DD} - |V_{Tn}| \right) + V_{Tn} \quad (4.2)
\]

\[
1 + \frac{\mu_p W_p}{\mu_n W_n}
\]

as \( L_n = L_p \) we have

\[
\frac{\beta_n}{\beta_p} = \frac{\mu_n W_n}{\mu_p W_p} \quad (4.3)
\]

\[
\beta_n = \frac{\mu_n e_{ox}}{t_{ox}} \frac{W_n}{L_n} \quad \text{and} \quad \beta_p = \frac{\mu_p e_{ox}}{t_{ox}} \frac{W_p}{L_p} \quad (4.4)
\]

Typically \( \mu_n = 1200 \text{ cm}^2/\text{Vs} \) and \( \mu_p = 450 \text{ cm}^2/\text{Vs} \) for silicon hence \( \mu_n/\mu_p = 2.7 \).

If we keep \( W_p = W_n \) then the threshold voltage of the inverter is less than ideal \((V_{DD}/2)\). The reason for this is that the more mobile electrons in the NMOSFET enable the NMOSFET to operate at lower \( V_{DS} \) than the PMOSFET for the same \( I_{DS} \) hence pulling \( V_{out} \) (equal to \( V_{in} \) at threshold) low. The threshold voltage can be increased by increasing the width of PMOSFET (hence \( W_p/W_n \)) so that \( V_{DS} \) of PMOSFET falls. In fact, if the ratio \( W_p/W_n = \mu_n/\mu_p = 2.7 \) is achieved then a threshold voltage of \( V_{DD}/2 \) is obtained [5].

This trick of making the PMOSFET larger to compensate for the lower hole mobility is universally used in silicon designs. Figure 4.4 shows threshold voltage of a CMOS inverter as a function of \( W_p/W_n \).
4.3 CMOS Inverter as a Comparator

The inverter threshold \( V_m \) is defined as the \( V_{in} = V_{out} \) in the VTC of an inverter. Mathematically,

\[
V_m = \frac{r \left( V_{DD} - |V_{TP}| \right) + V_{TN}}{1 + r} \quad \text{with} \quad r = \sqrt{\frac{k_p}{k_n}} \tag{4.5}
\]

Where \( V_{TP} \) and \( V_{TN} \) represent the threshold voltages of the PMOS and NMOS devices, respectively.

Figure 4.5 shows the schematic of an inverter and its VTC from the simulation. At the first inverter, the analog input signal quantization level is set by \( V_m \) depending on the \( W/L \) ratios of PMOS and NMOS. The second inverter is used to increase voltage gain and to prevent an unbalanced propagation delay. In figure 4.5, the slope of \( V_{out} \) is shown larger than the one of \( V_{out1} \). The inverter threshold depends on the transistor sizes. The inverter VTC \( V_a \) and \( V_b \) show the difference from the VTC of \( V_{out} \). With a fixed length of the PMOS and NMOS devices, we can get desired values of \( V_a \) and \( V_b \) by increasing only the width of the PMOS and NMOS transistors, respectively.
This result can be confirmed by the following equation of the inverter threshold [47].

\[
V_m = \frac{\frac{\mu_p W_p}{\mu_n W_n} (V_{DD} - |V_{TP}|) + V_{TN}}{1 + \sqrt{\frac{\mu_p W_p}{\mu_n W_n}}}
\]  

(4.6)

where \(\mu_p\) and \(\mu_n\) are the electron and hole mobility, respectively of the devices. To derive equation 4.6, we assume that both transistors are in the active region, the gate oxide thickness \((C_{ox})\) for both transistors is the same, and the lengths of both transistors \((L_p\) and \(L_n\)) are also the same. Also the value of \(V_m\) is shifted depending the transistor width ratio \((W_p/W_n)\). That is, increasing \(W_p\) makes \(V_m\) larger, and increasing \(W_n\) results in \(V_m\) being smaller on the VTC.

This changing of the widths of the PMOS and NMOS devices with a fixed transistor length is the idea behind the TIQ comparator. We can use the inverter threshold voltage as an internal reference voltage to compare the input voltage. However, to use the CMOS inverter as a voltage comparator, we should check the sensitivity of \(V_m\) to other parameters, which are ignored in equation 4.6, for correct operation of the TIQ flash ADC.

In a mixed-signal design, the ignored parameters - threshold voltages of both transistors, electron and hole mobility, and power supply voltage - are not fixed at a constant value.

The following sections will discuss the sensitivity to process, temperature, and power supply voltage.
4.3.1 Sensitivity to Process

For implementing the TIQ comparator, the MOS transistor model using EDA tools that includes many parameters to define a transistor behavior is used. However in reality, there are many parameters. We cannot be sure that the simulation results with such transistor model will be exactly matched with the measurement results. Therefore, we need a more complete transistor model for the inverter threshold sensitivity to reduce the gap between the simulation results and the measurement results. This will again increase the analysis of transistor and its behavior for its different physical parameters.

Moreover, if we apply another transistor model that was not used in our ADC design, the inverter threshold sensitivity will be critical in the TIQ comparator. Since process parameters change from one fabrication to another fabrication, the inverter threshold voltage will change [69]. This situation is especially one of major problems for linearity errors of the TIQ comparator that uses $V_m$ as a reference voltage.

4.3.2 Sensitivity to Temperature

The inverter threshold voltage also depends on temperature according to the following partial differential equation:

$$
\frac{\partial m}{\partial T} = \frac{1}{1 + \frac{\mu_p W_p}{\mu_n W_n}} \left( \frac{dV_{T_n}}{dT} - \frac{\sqrt{\frac{\mu_p W_p}{\mu_n W_n}} dV_{T_p}}{dT} \right)
$$

(4.7)

If the temperature is changed, then the effective mobility, channel length, and threshold voltage of the PMOS ($V_{T_p}$) and NMOS ($V_{T_n}$) devices will be affected. Therefore, the inverter threshold will be also changed [26]. The inverter threshold variation with Equation 4.7 has been simulated by many researchers. The simulation results show that large ratio of $W_p/W_n$ is more sensitive to temperature variation. For temperature variation simulation, the range of temperature - from $-40^\circ C$ to $85^\circ C$ is observed by researchers.

4.3.3 Sensitivity to Power Supply Voltage

Since the CMOS inverter has a single-ended input, it is more susceptible to power supply voltage noise than the differential comparator. This is reported to be one of the major issues in designing the inverters and in turn comparators. The partial differential equation for power supply voltage can be expressed by
Like equation 4.6, the lengths of PMOS and NMOS devices are assumed to be equal. This equation also shows that the larger ratio of the $W_p/W_n$ the more sensitive $V_m$ is to power supply voltage variation. This fact has been proved by simulation. Generally, a ±5% power supply range is used in a commercial chip. This rejection ratio will be used in the power supply voltage variation simulation.

4.4 Comparator Generation and Selection Method

The basic requirement of a TIQ flash ADC is $2^n - 1$ different size comparators and we need to effectively find their sizes to correctly implement the TIQ comparators. The size of each transistor in comparator design matters as it decides the switching voltage of the comparator. However, choosing the needed $V_m$ from many candidates for comparators and generating the selected comparators with a custom layout are difficult jobs. For example, a 8-bit flash ADC would need 255 TIQ comparators, too many for manual layout designs, while other ADCs use a single comparator design and simply duplicate it for $2^n - 1$ times. In TIQ method all comparators are designed with systematically varying the sizes of the transistors. The generation of the TIQ comparators with an optimal selection approach is important while designing such comparators.

A CMOS inverter consists of one PMOS and one NMOS transistor, with the inverter switching threshold voltage depending upon the transistor sizes. If one fixes the length of both the PMOS and NMOS transistors at a constant size, one can obtain different inverter threshold voltages by simply varying the transistors' widths. Figure 4.6 shows the 3-D plot of $V_m$ as the function of PMOS and NMOS transistor widths.

To design an n-bit ADC, we need $2^n - 1$ equal quantization voltages, and we must decide on the maximum $V_m$ and the minimum $V_m$. This is a band of voltage within which the comparator switching voltage lies.

After deciding the maximum $V_m$ and minimum $V_m$, we compute the LSB voltage step ($V_{LSB}$) by $(\text{max. } V_m - \text{min. } V_m)/(2^n - 2)$.

$$\frac{\partial V_m}{\partial V_{DD}} = \frac{1}{1 + \frac{\mu_n W_n}{\sqrt{\mu_p W_p}}}$$ (4.8)
There are two different design methods for the TIQ comparator for the $V_m$ values shown in Figure 4.6. One method, called the random size variation (RSV) technique [25], can obtain the $2^n - 1$ reference voltages by selecting the inverter width from the full range of the 3-D surface without considering the relation of adjacent comparators. This method is named zero DNL design method. The other method, called the systematic size variation (SSV) technique [25], considers the relation of comparators in selection of the inverter size. This method is named non-zero DNL design method. Detailed descriptions are given in the following sections. Systematic size variation (SSV) technique is more preferred as it gives uniform switching between the comparators and it is easy to calculate the voltage step.

4.4.1 Random Size Variation (RSV) Technique

The Random Size Variation (RSV) technique simply chooses the $V_m$ from the full range of the 3-D plot (around 2 million points). This algorithm selects the actual $V_m$ that is the closest to the ideal $V_m$, theoretical points that are exactly spaced by $V_{LSB}$, regardless of the transistor size relationship with other comparators. This method needs much time to find a $V_m$, because it checks all points of the 3-D plot. As a result, all of the internal reference voltages of the $2^n - 1$ comparators are almost equally divided by $V_{LSB}$. Hence, the DNL (defined by $((V'_{i+1} - V_i)/V_{LSB}) - 1$) of this approach is almost zero. The increase or decrease of the transistor size is not systematic.

4.4.2 Systematic Size Variation (SSV) Technique

In the case of the Systematic Size Variation (SSV) technique, the $V_m$ is selected from a reduced-range of the 3-D plot. The diagonal line shown in figure 4.6 is the ideal line for
this approach. This approach keeps the systematic increasing/decreasing order of transistor sizes. But, the values along the diagonal line are in too small range to find proper \( 2^n - 1 \) reference voltages. Therefore, the range is expanded around the diagonal line.

We obtain the systematic increasing/decreasing comparator transistor sizes by considering the relation of adjacent comparators. The SSV algorithm determines the best fit \( V_m \) values around the diagonal line in figure 4.6, keeping an increasing/decreasing order of transistor sizes. The algorithm also enforces the incremental transistor size step to a certain minimum width (\( \Delta W \)), which is initially given, for the maximum resolution of the given CMOS technology. The SSV technique uses the following four steps to generate the \( 2^n - 1 \) TIQ comparators:

**Step 1:** Generating a set of inverter sizes roughly following the diagonal line. The maximum \( V_{m_{max}} \), minimum \( V_{m_{min}} \), and \( \Delta W \) are needed for this step.

**Step 2:** Finding \( V_m \) of each inverter produced in Step 1 through simulation. This step takes much more time.

**Step 3:** Selecting a set of \( 2^n - 1 \) inverters, among the inverters generated in Step 1, whose \( V_m \) voltages are the nearest to the ideal one, satisfying the following conditions simultaneously:

- Does each comparator keep the order of increasing/decreasing transistor sizes?
- Does the differences between two adjacent comparators keep at least the \( \Delta W \)?

**Step 4:** Generating a cell design of the TIQ comparators based on the selected set of inverters in Step 3.

Figure 4.7 shows an example of how the SSV technique generates a set of transistor sizes and chooses the best fit (optimal) ones among them. From every possible combination of PMOS and NMOS transistor sizes, they are first arranged along the diagonal line. Next, the optimal combinations are selected by looking up the \( V_m \) values of each combination resulted from the simulation. The filled black dots are the selected combination of PMOS and NMOS transistor sizes for the TIQ inverters.

**4.5 Gain Booster**

These are the circuits used after the TIQ comparators and are cascaded with the comparator. Each gain booster consists of two cascading inverters with the same circuit as the comparator, but the transistor sizes of each gain booster are small and identical. The gain booster is used to increase voltage gain of the output of a comparator so that it
provides a full digital output voltage swing. A complete structure of a TIQ comparator along with gain booster is shown in figure 4.8.

![Figure 4.8](image-url) A complete structure of a TIQ comparator along with gain booster.

Figure 4.7 An example of the SSV technique [22]

Figure 4.9 and figure 4.10 respectively show the voltage gain of the gain booster and propagation delay over transistor length variation. The propagation delay's trend is almost exponentially proportional to the transistor length, but the voltage gain follows a logarithm function.

![Figure 4.9](image-url) An example of the SSV technique [22]
Therefore both propagation delay and voltage gain should be considered together when we choose the size of the gain booster.

**Figure 4.9** Gain booster voltage gain result vs. gate length

**Figure 4.10** Propagation delay result vs. gate length

### 4.6 TC-to-BC Encoder

After the comparators produce a thermometer code (TC), the thermometer code to binary code (TC-to-BC) encoder generally converts it to a binary code (BC) in two steps. The TC is converted to the 1-out-of-n code, using XOR logic. This code is then converted to binary code. The two steps for TC-to-BC encoder are shown in figure 4.11. The most common implementation of the TC-to-BC encoder has been the ROM/PLA circuits; however, the TC-to-BC encoder is often the bottle neck of high sampling rate flash ADCs. Alternate
encoder designs such as a Wallace tree encoder for 1 GHz sampling rate flash ADC implemented with gallium arsenide (GaAs) technology, a XOR encoder for a higher data rate ADC implementation with silicon-germanium (SiGe) bipolar technology, and a pipeline encoder for a higher data rate ADC implemented with the Josephson-junction super-conduction technology have been used. Thermometer-to-binary decoder can be implemented by various approaches, e.g., a ROM, Wallace-tree (or ones-counter), multiplexer-based decoder, fat-tree decoder and logic-based decoder [71].

At the highest input frequencies, however, errors in the thermometer code, related to timing and meta-stability problems, become a serious concern. They show up as bubbles, i.e. zeros surrounded by ones or vice-versa. If bubbles are present in the thermometer code, two or more rows of the ROM may be selected resulting in a wrong output code, i.e. a glitch of the A/D converters output [69].

The following sections describe three encoders: a ROM type encoder, a fat tree encoder and Wallace tree encoder. The ROM type encoder is generally used in a flash ADC architecture. To increase the speed of the flash ADC, we propose a new TC-to-BC encoder, the fat tree encoder that is highly suitable for a high speed and low power CMOS flash ADC and a Wallace tree encoder.

The design of multiplexer-based thermometer-to-binary decoder is also discussed by some researchers. This decoder is based on 2-to-1 multiplexers connected as a tree. Each level of the tree divides the input thermometer scale in two and calculates one of the bits in the binary output. In comparison with the Wallace tree decoder the length of the critical path is approximately reduced to one third. The amount of hardware is also reduced, which will translate to a power saving, compared with the Wallace tree decoder [62].

Figure 4.11 Two stage fat tree TC to BC converter
4.6.1 ROM Type Encoder

To convert a 1-out-of-n code to a BC, a ROM can be used. An optimized, with respect to transistor sizes, NOR ROM circuit was developed to achieve high speed conversion as shown in figure 4.12. In the TIQ flash ADC, the ROM speed is the predominant factor of the overall ADC speed because the signal delay of the ROM is algorithmically \(O(N)\), where \(N\) is the number of ROM inputs. Therefore, we need to improve the speed of the encoder with an alternative design, non-ROM type such as Fat tree encoder and Wallace tree encoder.

![Figure 4.12 ROM type encoder of a 3-bit ADC [26]](image)

4.6.2 Fat Tree Encoder

We propose the fat tree encoder to improve the encoder speed that is the bottle neck of a flash ADC speed. The main advantage of the fat tree encoder over the other encoders is its high encoding speed and low power consumption. Figure 4.13 shows an example of the 3-bit fat tree encoder and figure 4.14 gives an idea about fat tree encoder for 4-bit flash ADC. The 1-out-of-8 code, which is the output of the '01' generator, is presented at the leaf nodes (from a7 to a0) of the tree.
The 3-bit binary output ($d_2$, $d_1$, and $d_0$) is located at the root of the tree. The output is obtained by a logical OR ing of the leaf nodes depending on the truth table shown on the right in figure 4.13. When using only 2-input OR gates, 6 OR gate results go to the parent nodes, then finally 4 OR gate results ($d_u$, $d_2$, $d_1$, $d_0$) are obtained. One of those 4 results, $d_u$, will be used for the next level of the tree. As shown in the tree, the number of edges increases from leaf to root. So, this new encoder type is named the fat tree encoder. The fat tree encoder's signal delay is $O(\log_2 N)$ because of its tree architecture. Therefore, it is much faster than the ROM type encoder; for example, there are only 2 OR gate delays in case of 3-bit encoding. Also, all multiple OR gates can be changed to NOR and NAND gates for more efficient implementation. Moreover, the fat tree encoder can be easily pipelined at each height in the tree.

Even though it has an advantage in terms of speed of the ADC, it is much more difficult to design and automatically generate than the ROM type encoder. Because the fat tree is 3-dimensional, design automation of the fat tree encoder is one of the challenges for an improved implementation of the TIQ flash ADC.
Wallace tree (or ones counter) takes the outputs of comparator block directly (in the thermometer code format) and processes it. This structure simply counts the number of 1’s appeared at its inputs and decodes them into binary format. This technique offers global error correction/suppression unlike the FAT-tree and ROM-Table where bubble errors are usually handled locally using 3-or-higher-input NAND gates.

\[ \text{bit0} = a_0 + a_1 + a_2 + a_3 + a_4 + a_5 + a_6 + a_7 = 1 \]
\[ \text{bit1} = b_0 + b_1 + b_2 + b_3 = 0 \]
\[ \text{bit2} = c_0 + c_1 = 0 \]
\[ \text{bit3} = d_0 = 1 \]

Figure 4.14 Fat tree encoder for 4 bit ADC case
To conclude, TIQ comparator with CMOS inverters can be used as a basic building block of flash ADC. CMOS inverters have almost negligible power consumption in static mode. Systematic size Variation (SSV) is used for comparator switching. This is supported by TC to BC converter next phase. Fat tree encoder outperforms the ROM encoder for power and speed. Many researchers have used and proved fat tree encoder to be best for high speed ADC design.

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