Chapter 2

Literature Review of IA

2.1 Introduction

Instrumentation amplifiers are important circuits in the number of sensor readout systems, where it is required to amplify small differential signals in presence of large common mode interference. For the application like EIT, it is necessary to measure bioimpedance over a wide frequency range, and for portable application. Hence, it is needed to design an IA of small size, wide band and with low power consumption. The important parameters of IA, which affect the performance of front end systems are CMRR, bandwidth, input common mode range (ICMR), power consumption and area of chip. Different topologies used to design IA are three op-amp IA and current feedback IA.

The published research work in standard publications like IEEE Journals of solid-state devices, IEEE symposiums and many more conferences, Springer Science international journals and transactions in relation to the design of CMOS monolithic IA are surveyed and studied with the help of vast reference literature. Review of literature along with their methodologies of implementation and set benchmarks are discussed for reference in this chapter.

2.2 Conventional Three Op-amp IA with Resistive Feedback

The three op-amp topology became most popular topology for designing the instrumentation amplifier. The classic 3-op amp IA circuit is a clever modification of the buffered subtractor circuit [16] [17]. Because of the symmetry of this configuration, common-mode errors in the input amplifiers, if they track, tend to be canceled out by the output stage subtractor. This includes errors such as common-mode rejection versus frequency. These features make this configuration popular.

Two alternatives are available for constructing 3-op amp instrumentation amplifiers: using bipolar or FET based operational amplifiers. FET input op amps have very low bias currents and are generally well suited for use with very high (>10^6 Ω) source impedances. FET amplifiers usually have lower CMRR, higher offset voltage, and higher offset drift
than bipolar amplifiers. They also may provide a higher slew rate for a given amount of power.

All the papers reviewed in this section are based on three op-amp topology IA with resistive feedback.

Manish Goswami et al. [18] presented a paper on “DC Suppressed High Gain Active CMOS Instrumentation Amplifier for Biomedical Application” in 2011. A three op-amp active resistance IA with high gain and dc suppression was proposed in this paper. High gain is achieved by careful selection of aspect ratio of op-amps and by efficient design of passive resistors by active MOS transistors. The proposed circuit has many interesting characteristics regarding low noise and simple design, while preserving common mode rejection ratio (CMRR) and high input impedance characteristics of the classical three op-amps IA. The instrumentation amplifier is simulated using Cadence Spectre 500nm CMOS technology. The simulated results observed an input-referred noise voltage of $22nV/\sqrt{Hz}$, Gain of 45dB, Bandwidth of 5.8 KHz, CMRR in the range of 75dB and power consumption about 280µW, which is very good for biomedical signal processing application.

Chih-Jen Yen et al. [19] published a paper on “Micro-Power Low-Offset Instrumentation Amplifier IC Design for Biomedical System Applications” in 2004. This paper describes a micro-power low-offset CMOS IA integrated circuit with a large operating range for biomedical system applications. With the wide-swing cascode bias circuit design, this amplifier realizes a very high power-supply rejection ratio (PSRR). It is fabricated using 0.5µm double-poly double-metal (2P2M) n–well CMOS technology, and occupies a die area of 0.2 mm$^2$. This amplifier achieves 0.05% gain linearity, PSRR>102-dB, an input-referred rms noise voltage of 45 µV and a current consumption of 61 µA at a low supply voltage of 2.5 V. The proposed circuit can be used to analyze the input electrocardiogram signal of a patient monitoring system and other portable biomedical devices.

A Low-Power, Single-Supply, CMOS instrumentation amplifiers INA332 by Texas Instruments are commercially available [20]. INA332 has features like high gain accuracy 0.07% and 2ppm/°C at Gain = 5V/V and it can be set by external resistors for > 5V/V. It also has high CMRR 73db at DC and 50 dB at 45 kHz, slew rate 5V/µs, low quiescent
current 490μA maximum/channel. This IA is used as a front-end amplifier for the industrial sensors like bridge, RTD, thermocouple, position and physiological amplifiers like ECG, EEG, EMG.

AD8221 Precision Instrumentation Amplifier by Analog Devices is based on the classical 3-op amp topology [9]. The AD8221 is a gain programmable, high performance instrumentation amplifier that delivers the industry’s highest CMRR over frequency in its class. The AD8221 maintains a minimum CMRR of 80 dB to 10 kHz for all grades at Gain = 1. High CMRR over frequency allows the AD8221 to reject wideband interference and line harmonics, greatly simplifying filter requirements. A single resistor sets the gain from 1 to 1000. The AD8221 operates on dual power supplies and is well suited for applications where ±10 V input voltages are encountered. Chip area occupied by the IC is 3.51mm².

2.3 Current Feedback Monolithic IA

The current feedback IA typically consists of an input operational transconductance amplifier (i.e. voltage-to-current converter), an output operational transconductance amplifier and one or more high gain feedback loops using active-feedback network. The current feedback IA may employ single feedback loop around both transconductors. In the direct current feedback IA, the two transconductors are stacked in a single branch and this limits the input common-mode voltage range and the maximum output voltage swing. In indirect current feedback IA, the two transconductors form two separate loops. In addition, the output voltage is feedback to the input of a second stage operational transconductor in contrast with direct current feedback IA. As compared to the conventional resistive feedback approach, the current feedback IA design approach offers higher operating bandwidth. In addition, these circuits can achieve higher CMRR performance by using both isolation and balancing techniques in the feedback loop.

Review of all the papers mentioned below have employed direct or indirect current feedback IA.

The first single chip monolithic indirect current feedback IA was presented in 1971 by H. Krabbe using Bipolar Junction Technology (BJT) [21]. This amplifier used a two-amplifier system providing forced current feedback around single loop to achieve high input impedances at both the inputs and single resistor closed loop gain selection 1-1000. This
amplifier achieved a CMRR of 106 db with bandwidth 100 Hz. Further CMRR holds up to 86 dB with bandwidth 2.5 kHz and gain 1000. With supply voltage ±15V, the output swing achieved ±10V. The required operating power is 120mW.

The first single chip monolithic indirect current feedback IA, presented in 1971 by H. Krabbe, was rearranged in 1975 by A. Paul Brokaw [22]. It eliminated a requirement to include one close loop amplifier within feedback path of second amplifier. This eases the frequency compensation problem, which can be severe due to multiple loop variable gain feedback system. In addition, it has an improved input amplifier settling time. The amplifier input impedance has made artificially high using feedback. The CMRR achieved by this circuit was 120dB with gain set to 1000. The output voltage swing was ±11.5V with 1KΩ load and dual power supply ±15V. The power dissipation of the circuit was 75mW with power supply current 2.5mA. The dimension of the chip for this circuit was 71mm x 110mm.

Michel S. J. Steyaert et al developed a micro power low-noise monolithic Instrumentation Amplifier using CMOS technology [23] first time in 1987. The conventional three-op-amp structure requires op amps with a low output impedance to drive the resistors of the IA network. This results in op amps with a large power drain with CMOS design. To overcome this problem, an IA has been designed based on the current feedback technique and using only single stage operational transconductance amplifiers (OTA’S) in the low-frequency feedback loop. This IA circuit used direct current feedback configuration with both transconductors stacked in single branch. The gain values of the IA are set by software control in four ranges (14/20/26/40 dB). The CMRR achieved by this circuit was 90 dB with bandwidth of 100 Hz. The circuit was operated with dual power supply ±2.5V, and total current drawn was 30µA, thus power consumption of circuit became 150 µW. The total ICMR is given by ICMR+ - ICMR- comes out to be 1.9 V, which is low due to direct current feedback topology. The total area of the IA measures 1000 X 1200 µm².

Rui Martins et al. presented [24] monolithic implementation of IA for portable EEG acquisition system in 1998, which gives more freedom of movements to the patient and allows small leads between electrodes and input amplifiers. The small leads are important for systems acquiring very low-level signals in noisy environment. The portability requires very low power consumption to guarantee battery life. This IA circuit used indirect current
feedback and was CMOS variation of BJT IA [22]. The PMOS transistors used at input reduce the flicker noise. Input transistors were made to work in moderate inversion to improve CMRR and reduce power consumption. This IA has designed for fixed gain of 500 and CMRR is 99 dB at 50 Hz. This circuit has dual power supply ±4.5 V, and total current drawn was 33µA, thus power consumption of circuit 297µW. The active area of chip measures 1.5 mm². The ICMR came out to be 5.3 V.

Refet Firat Yazicioglu et al. in their paper [26] on “Effect of electrode offset on the CMRR of the current balancing instrumentation amplifiers (CBIA)” presented new CMOS IA in July 2005. The architecture of CBIA of [23] was modified with a technique to improve CMRR under the electrode offset. The drain voltages of input MOSFETs are adjusted with the help of two source followers and a current mirror source load. The measured CMRR obtained with offset voltage of ±50mV was 157 dB at 50Hz with gain set to 10V/V. The circuit consumed 110 µA from a 3V power supply, and bias current of the input transistors was fixed at 12 µA each. The circuit was simulated with 0.5-µm CMOS technology.

The work published by Maryam Shojaei-Baghini et al. in 2005 on Analog front-end amplifier for electrocardiogram (ECG) monitoring consists of ultra low power IA [27]. The analog front-end amplifier designed was CMOS instrumentation amplifiers based on current balancing technique with low power consumption, compact and lightweight. The distinguished features of the presented design are using CMOS instrumentation amplifiers based on current balancing technique for ECG signal conditioning and programmable high-pass filter included. The circuit was implemented in 0.35 µm TSMC mixed-mode CMOS process and occupies 0.2-mm² area. The CMRR of the circuit was achieved to 100 dB at 60 Hz and ICMR of the circuit measures 0.3 to 2.3V. This chip draws 66 µA from a 3.3V Lithium-ion battery restricting power dissipation to 218 µW.

Refet Firat Yazicioglu et al. [28] have implemented a new design in 2007 namely 60 µW 60 nV/√Hz readout front-end for portable bio-potential acquisition systems. They implemented a low power low noise readout front end with configurable characteristic for EEG, ECG and EMG signals. The low power current feedback IA is a key performer in the system, which uses a direct current feedback. The CMRR achieved was 120 dB with a bandwidth limited to 40 Hz and input referred noise density 57 nV/√Hz. The consumption of IA IC was 11.1 µA from 3V power supply. Thus, it is capable to operate more than 3
years from 2 AA batteries. Input common mode range comes out to be 1.05V to 1.7V. The core area of IA chip measured less than 2 mm$^2$.

In paper [25] titled Design of an integrated low power high CMRR instrumentation amplifier for biomedical applications, Cesar Augusto Prior et al. implemented a monolithic IA using Trapezoidal Association of Transistors (TAT) in 2008 and published in Springer AICSP Journal. The schematic of IA used miller OTA amplifiers and current subtractor. The amplifier was simulated with Mentor Graphics IC station tool. The extracted circuits were simulated with Eldo simulator using the model BSIM3V3 provided by MOSIS. The technology used was 1.5µm. The power consumption came out to be 110 µW with a gain 64 dB. The bandwidth measured 127 Hz at CMRR of 110 dB. The out voltage swing was measured ± 1.4 V with power supply 2.5 V. The full die area of chip measured 2.2 mm x 2.2 mm.

Johan F. Witte et al. in 2008 presented their work on a current feedback IA [29] with 5 µV offset for bidirectional high side current sensing using 0.8 µm Bi-CMOS process. In this work chopper offset-stabilization techniques used in op-amp are extended to current feedback IA. The indirect current feedback approach is adopted to avail the advantage of gain accuracy and linearity. The die area of IA chip was 2.5-mm$^2$.The supply voltage $V_{DD}$ can range from 2.8 to 5.5V, where as being indirect feedback input common mode voltage can independently range from 2 to 30V. The CMRR achieved was 143 dB at DC and falls to 108 dB at 10 KHz. The power dissipation of IC came out to be 3.57 mW.

Chinmayee Nanda et al. proposed a CMOS IA [30] with low voltage and low noise for portable ECG monitoring systems in 2008 at IEEE international symposium ICSE 2008, Johor Bahru, Malaysia. The circuit based on current feedback topology has been implemented using folded cascode structure as an input stage. The folded cascode stage supports very low input common mode voltage and increases output voltage swing but with increased device count and power dissipation. The circuit was simulated in 0.18µm standard CMOS process. A high CMRR of 127 dB has been achieved at 50 Hz. The circuit was operated at very low supply voltage of 1V and power dissipation was 165 µW. The input common mode range is -50 mV to 650 mV.
Apisak Worapishet et al. designed a CMOS IA with 90 dB CMRR at 2 MHz using capacitive neutralization in 2011 [31]. The circuit is intended for wide band bio impedance spectroscopy application in medical imaging. The IA used indirect current feedback with two isolated local feedback loops, one around input transconductor and the other around output transconductor. It is also known as local current feedback. In this paper, the mismatch mechanisms that affect CMRR performance from low to high frequencies are analyzed. The systematic mechanism that affected CMRR over useful frequency range was capacitive mismatch due to current mirror load at input stage. This mismatch was minimized using a capacitive neutralization at input stage. This local current feedback IA was designed, simulated and fabricated using the 0.35 µm austriamicrosystems CMOS process technology. The two resistors set the differential gain of 50 V/V and the supply voltage was taken 3V. The bulk terminal of all NMOS devices was connected to most negative voltage (0V) in the circuit and that of PMOS devices was connected to its source terminal. The current consumption of the total circuit including output buffer was 3.3mA hence power dissipation 9.9 mW. The CMRR of 83 dB was obtained with bandwidth of 2 MHz and ICMR measured 1.6V. The active area of the circuit on chip is 0.068 mm².

D. Susheel Kumar et al. have presented a paper [32] on a high CMRR analog front-end IC for wearable physiological monitoring in 2012. This paper is based on current balancing technique. The IA consist of transconductance stage, transimpedance stage, integrated high pass and low pass filters get bandwidth 0.05- 125 Hz and driven right leg circuitry to minimize common mode noise. The cascode current mirror load used instead of single transistor mirror yields better output resistance and CMRR get increased. The patient’s body acts as an antenna that picks up electromagnetic interference, especially 50/60 Hz from power lines. The driven right leg circuitry is used to eliminate this interference noise. The 0.18µm CMOS process technology is used to fabricate the circuit of IA. The IA gain was set to 10. The designed IA achieved a CMRR of 122 dB with bandwidth 0.05-125 Hz and ICMR is 0-1.65V. The power consumption of total circuit is 132 µW with 3.3 V supply. The active area of implemented IC is 0.019 mm².

Wei-Chih Huang et al. implemented CMOS low noise readout front-end for portable bio-potential signal acquisition [33] and published at Biomedical Circuits and Systems...
Conference (BioCAS), IEEE in Nov 2012. The block diagram of the analog front-end included the fully differential chopper current balancing IA as an input stage to measure signals in µV level and in presence of low frequency noises such as flicker noise. The current balanced IA uses transconductance and transimpedance stage. The transconductance stage converts the input signal voltage to a current passing through the input resistor and then copying it to the output resistor of transimpedance stage. Thus, the voltage gain of the current-balancing IA is given by ratio of two resistors. To achieve high CMRR, the high swing cascode current mirror was used in the current balancing IA to increase the output resistance of the current mirror. The current balancing IA achieved CMRR of 104 dB with bandwidth 0 to 256 Hz. Being portable power supply selected was 1V and current consumed 26.56 µA. The chip area was 1 x 1 mm².

Federico Butti et al. published a paper [34] on “A compact instrumentation amplifier for MEMS thermal sensor interfacing” at Springer AICSP journal in June 2011. A work consists of compact CMOS IA based on second order Gm-C low pass filter. The simulations performed using the electrical simulator ELDO of Mentor Graphics. The technology used was 0.32 µm with 3.3V power supply. The power consumption of IC came out to 4 mW with gain of 200. The bandwidth achieved was 200 Hz and chip area 0.13 mm².

Andreas Demosthenous et al. in their paper titled “An Integrated Amplifier with Passive Neutralization of Myoelectric Interference from Neural Recording Tripoles” [35] in September 2013 at IEEE sensors journal described an Integrated Amplifier for Neural recording from tripolar electrode books connected quasi-tripole arrangement. The amplifier is compatible with stimulation. The bladder control was the targeted application but other applications like reaching and grasping for C5/C6 spinal cord injured or stroke patients, treatment of obstructive sleep apnea can be achieved. The front end circuit employs IA with current feedback to achieve high CMRR. The IA circuit consists of two resistive degenerated transconductors: 1. An input transconductor with local feedback loop. 2. An output transconductor with local feedback loop. Both feedback loops are isolated from each other. Due to current feedback the drain current of input MOSFETs in input transconductor are forced to be same and thus input stage acts as a unity gain buffer. Similarly, the use of current feedback forces the drain currents of MOSFETs in the output
transconductor. The first order low pass filter using operational transconductance amplifier (OTA) and a capacitor is inserted between output and the input of output transconductance to create desired lower cut off frequency. The chip operates from a power supply of 3V with supply current drawn 310µA. The circuit implementation was fabricated in the austriamicrosystems 0.35 µm C35 CMOS technology. The worst case CMRR achieved was 99dB at 1kHz and 90dB at 10kHz respectively. The area of chip is 0.08mm².

Behzad Razavi [3] proposes a new design of cascode single ended op-amp theoretically in his book on “Design of Analog CMOS Integrated Circuits”. In the schematic of indirect current feedback IA, output loop includes single ended differential amplifier. This amplifier is desired to have very high gain. Hence, it is implemented as a single ended cascode op-amp. The single ended cascode op-amp is loaded by cascode current mirror source to avail high gain. This cascode load limits the maximum value of output voltage, as it wastes threshold voltage of one MOSFET. To resolve this problem two of the load’s MOSFETs in the same branch are biased at the edge of triode region.

Gray, Hurst, Lewis and Meyer [36] in their book on “Analysis and Design of Analog Integrated Circuits” discussed that the inter electrode capacitance of MOSFET is higher when operated in saturation region than triode region. Some of the MOSFETs in signal path of high gain amplifier can be operated in triode instead of saturation region. By operating MOSFETs in triode region will lead to reduced gain but increased higher cut off frequency thus increased bandwidth.

2.4 Summary and Concluding Remarks

A meticulous review of literature points towards design of CMOS IA using three different techniques. Reviewed literature is from the standard publications and of last 32 years. Outline of review is as given below.

- In many biomedical measurement systems, the performance of system is limited due to the analog front-end circuit used for signal conditioning. The CMOS IA is a common front-end circuit with high CMRR and high bandwidth at reasonable power dissipation and size for portability. Researchers are investigating new design techniques for CMOS IA in order to reduce power consumption, increase CMRR, bandwidth and decrease area on the chip.
Many techniques are used to improve the CMRR and bandwidth to measure the weaker biomedical signals in presence of common mode noise.

A conventional three op-amp topology of IA uses resistive feedback. The CMRR here is limited by degree of matching of resistors.

A current feedback technique is used to improve the CMRR. Here high CMRR is achieved because of isolation and balancing techniques. In direct current feedback, two MOSFETs in same branch carry unequal currents, thus become source of nonlinearity, and decrease the input common mode voltage range. In indirect current feedback, MOSFETs on input and output side carry equal currents hence eliminate nonlinearity. In addition, the input common mode voltage range is increased but at the cost of increase current dissipation.

The extensive Literature survey carried out is itself an indication of research path.

The work done so far in the area of CMOS IA reveals that the architecture designed using indirect current feedback (ICF) with CMOS devices will increase CMRR, bandwidth and reduce power to a considerable extent. Hence, author decided to use this method for further optimization of CMRR and bandwidth with improved techniques suggested theoretically to operate the MOSFET in triode region.

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