Chapter 1
Introduction

1.1 Moore’s Law

Complementary Metal-Oxide Semiconductor (CMOS) technology is continuously downscaling to increase the number of Metal-Oxide-Semiconductor Field Effect Transistors (MOSFET) to be integrated in a single chip. Gordon E. Moore, co-founder of Intel suggested the trend in 1965, which is known as Moore’s Law, that the number of transistors per chip doubles roughly every 2 years [1]. Along with this integration level trend, the overall cost is decreased and thus economic productivity and in effect overall quality of life are significantly improved through evolution of computers, communication, and other industrial and consumer electronics [2]. This downscaling trend however cannot be continued forever. The downscaling becomes difficult with semiconductors and the trend of integration would not continue with Moore’s law anymore. Fig. 1.1 shows how the International Technology Roadmap for Semiconductor (ITRS) draws the CMOS technology roadmap for the next decades.

![CMOS Technology Roadmap](image-url)
In order to fulfill the requirements in the economy growth and improving the quality of life despite the scaling limits according to Moore’s Law, the ITRS has addressed a new concept of research target called “Moore’s Law and More”. This concept is based on the three sub-sets of focus area – scaling, functional diversification, and beyond CMOS. Scaling refers to not only the continued downscaling of transistors but also includes fabrication process techniques such as study of new materials that affect the electrical performance of the chip, as well as design technologies that enable high performance, low power, high reliability, low cost, and high design productivity. Functional diversification provides an additional value to non-digital functionalities (e.g. RF communication), to be transferred from the system board level into package-level (system-in-package, SiP) or chip-level (System-on-Chip, SoC). Beyond CMOS focuses on new switching devices that can provide substantial functional scaling beyond that attained by ultimately scaled CMOS technology.

1.2 Level of Design

Design and Analysis of monolithic circuits often require abstraction at different levels. The complex circuits are studied at different levels such as Physics level, transistor (circuit) level, architecture level or system level depending on the effect or quantity of interest [3]. In device level the behavior of individual device is considered in terms of internal electric fields and charge transport (Fig. 1.2 (a)). In circuit level the interaction of group of devices according to their electrical characteristics is considered (Fig. 1.2 (b)). While in architecture level the function of several building blocks operating as a unit is considered (Fig. 1.2 (c)). The performance of system in terms of its constituent subsystems is considered in system level (Fig. 1.2 (d)). To understand the operation and optimization of overall performance, the switching between levels of abstraction becomes necessary. In this thesis, we concentrated on the complex circuit level abstractions.
1.3 Analog Design Octagon

The important aspects of analog circuit are gain, speed, power dissipation, supply voltage, linearity, noise and maximum voltage swing. In addition, the input and output impedances determine how the circuit interacts with preceding and subsequent stages. Always, most of these parameters trade with each other, making the design a multidimensional optimization problem. Such trade-offs present many challenges in design of high performance analog circuits as shown in Analog Design Octagon (Fig. 1.3). It requires intuition and experience to arrive at an acceptable compromise the design.
1.4 Background and Motivation

In clinical applications the use of bio impedance imaging, also known as electrical impedance tomography (EIT) (Fig. 1.4), offers advantages over other medical imaging techniques [4]. Unlike computerized tomography (CT scan) and X-rays, EIT does not emit ionizing radiations, and unlike magnetic resonance imagining (MRI), EIT is silent, highly portable, and inexpensive. EIT works by reconstructing the differences in electrical conductivity inside a body [5]. In a typical bio impedance measurement system, a differential alternating current (less than 1mA) at 10-200 kHz is applied through a pair of surface electrodes to the body tissue and the resulting voltages are picked up by another electrode pairs and amplified for further processing. The most common error occurring is common mode error signal which is due to changes in stray capacitance and electrode impedance mismatches. The practical result shows that the common mode signal is reduced by 85%, 75 %, 70% and 65 % at 10 kHz, 50 kHz, 100 kHz and 200 kHz respectively. Hence, the front-end amplifier is required to have very high input impedance to avoid part of the injected current shunted into the recording electrodes [6] [7]. This causes errors in the measurement thus there is a requirement for an Instrumentation Amplifier (IA).

![Figure 1.4. Simple EIT injection / recording system](image)

The main common-mode interference in bio impedance measurements occurs at the working frequency and is produced by the current injected into the body to make the measurements. In the case of EIT, the differential signal measured between adjacent pair of electrodes can be as small as a few tenths of micro volts whereas the common-mode
interference can be in the hundreds of milli volt (mV) range. For imaging of cancer biomarkers, it is necessary to measure bio impedance over a wide frequency range (10 kHz to 1MHz) and in multi frequency mode (bio impedance spectroscopy). The need for detection of weak signal in presence of strong common mode noise over wide bandwidth (BW) operation dictates that the IA should have high common-mode rejection ratio (CMRR) at high frequencies. CMRR is defined as the ratio of the differential gain over the common-mode gain [8]. To obtain good accuracy in the measurement, the IA requires a minimum CMRR of 80 dB over the frequency 2 MHz (3 dB BW). However, neither off-the-shelf monolithic IAs nor those reported in the literature meet this specification. The CMRR of high-performance IAs such as the AD8221 [9] is 80dB only up to about 100 kHz. Although commercial high-speed differential receiver amplifiers such as the AD8129/AD8130 [10] feature high CMRR at high frequencies, their current consumption is very high (>10 mA).

The conventional IA based on three operational amplifiers (op amps) is probably the most well known structure able to extract and amplify low-amplitude differential signals. In this topology, two op-amps are used to implement a fully differential buffer, which is followed by a single op amp configured as a differential amplifier [13]. However, this structure is not suitable when low power, low cost, and high CMRR are simultaneously required. Indeed, this conventional topology needs op amps with low output impedance to drive the feedback resistors, which implies high currents and large power consumption. In addition, precisely matched resistors are needed to achieve the high CMRR performance necessary in this application. This matching usually requires laser trimming of resistors, which is an expensive technique not available in standard CMOS technology. Hence, it is needed to have a single chip monolithic CMOS IA.

1.5 Research Objectives and Thesis Outline

The naturally occurring signals are analog and some times of microscopic level. These signals are often accompanied by unwanted interferences. In one of the applications of bioimpedance measurements for imaging of cancer biomarkers, it is desired to measure a weak signal in presence of strong common mode interference at very high frequencies. This dictates the requirement of high CMRR, high frequency and being portable low power IA.
The objectives of this thesis are to explore the circuit techniques for design and realization of a current feedback instrumentation amplifier with high bandwidth, acceptable CMRR, low-power and small-area for biomedical sensor signal-processing applications [12].

The proposed IA consist of Input Operational Transconductance Amplifier (OTA), Balanced Differential Amplifier, Output operational transconductance amplifier, Telescopic cascode op amp and source follower as level shifter.

The input stage OTA serves also purpose of unity gain buffer making input voltage to drop across a resistor. This is done by providing the current feedback through balanced differential amplifier and adjusting current through resistor. Same current is copied in transimpedance amplifier and there output voltage is forced to drop across another resistor which decides voltage gain of IA together with resistor on input side. The Telescopic cascode op amp serves the purpose of very high gain differential amplifier. The source follower is used to shift the dc level of output voltage.

1.6 Aims and Objectives

The research aims at proposing a circuit that targets the reduced power consumption, improved CMRR and bandwidth for an Instrumentation Amplifier. To accomplish these aims, the following objectives have been set.

Global objectives:

➢ To study the schematic and analysis of monolithic CMOS IA with improved CMRR.
➢ To focus design efforts for application of IA at higher frequencies (MHz).
➢ To estimate performance parameters like CMRR, Bandwidth, size and power.
➢ To prepare layout of IA to fulfill the dimensions.
➢ To explore different EDA tools like Tanner and Cadence for simulating and successful design of IA.
➢ To compare the obtained parameter values with benchmark design available.

Detailed objectives:

The scope of the research is:

➢ To understand the designing, optimization and testing of IA.
To improve the performance of CMOS IA by using improved operational transconductance, transimpedance amplifiers and current sources.

To improve the performance of balanced differential amplifier by using active loads.

To search for any other technique which can improve the performance of balanced differential amplifier.

To achieve the highest gain from CS single stage amplifier by using telescopic cascode configuration.

To build and test MOS current mirror, Cascode current mirror, Wilson current mirror sources.

To build and test source followers to implement the last stage a level shifter.

To improve bandwidth of IA using feedback through Operational Transconductance Amplifier (OTA) and biasing some MOSFET in triode region.

To form a complete instrumentation amplifier using improved blocks developed so far and simulated using Tanner and Cadence EDA tools.

1.7 Organization of Thesis

Following this introduction, the subsequent chapters are organized as follows.

Chapter 2 - Literature Review of IA – Literature survey based on previous research and development work by people worldwide published in IEEE, Springer, IET journals and reputed conferences is synoptically presented in this chapter. Through an exhaustive search the benchmarks results have been pointed out.

Chapter 3 - Consists of different instrumentation amplifiers architectures and reasons why to go for indirect current feedback IA. It is followed by discussion on important parameters of IA and scheme of the IA being implemented.

Chapter 4 - CMOS Cascode Amplifiers - This chapter starts gain stage that is basic common source amplifier and configuration to improve this gain. The telescopic cascode and folded cascode amplifiers are dealt in detail.
Chapter 5 - Operational Amplifiers (op amp) and Source followers – The single ended and double-ended differential amplifiers are treated in detail being basic of the op amp. The other blocks in the IA, the op amp and source followers are given detailed treatment in this chapter. The proposed circuits of these stages are designed and simulated.

Chapter 6 - Design, Simulation and Measurements of Parameters – This chapter describes about the EDA tools used for simulation of various blocks of IA. The different blocks of IA are simulated using EDA tool Tanner and Cadence and experimental results are verified with expected results. The layout is prepared of the final IA with Cadence. The results are compared with benchmark paper.

Chapter 7 - This chapter discusses the conclusions drawn on the experimentations, results obtained, contributions of author, limitations and future directions to the topic.

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