4.1 INTRODUCTION

Differential phase shift keying is the modification of binary phase shift keying and it avoids the need of coherent reference signal at the receiver. For DPSK, the data is not in the phase of transmitted signal but it is encoded in the phase difference between two adjacent symbol intervals. DPSK eliminates performance degradation due to phase differences between the carrier signal and receiver’s local reference signal when the differences are constant over two symbol intervals [29]. The channels with rapid frequency variation for moving stations, channels with fading and channels of burst communication systems produce a random frequency shift into the carrier. It is very difficult and almost impossible to estimate it on the basis of previous history of process. For such case, differential detection is used which is sensitive to frequency variation in the carrier. The differential detector is shifted and if it is large, it affects appreciably the system error probability. The above problem can be removed by using second order difference phase process [30]. The second order differential encoding have been studied extensively in 1970’s by various authors [31-40]. D^2PSK modulation and detection is found to attenuate the performance degradation effects of phase and frequency uncertainties. When the reference signals are noisy, for asynchronous carrier such an attenuation is achieved at the expense of performance. It has been observed that in the absence of frequency offset the performance degradation with a second order differentially coherent can exceed 4 dB as compared to differentially coherent DPSK system [41-43]. The binary D^2PSK gives better performance than binary DPSK in AWGN [44].

The (+1, -1) system is suitable in digital signal processing [45]. It is an alternate to two’s complement representation. In section-2, the brief review of
(+1, -1) representation has been introduced. Section-3 contains the principle and hardware realization of 1st order differential phase shift keying. In section - 4, the details of second order differential phase shift modulation and detection have been included. The numerical computation of probability of error is being discussed in section-5. Finally, the conclusion of the chapter is given in which the (+1, -1) system has been compared with the conventional binary system.

4.2 BRIEF REVIEW OF (+1, -1) REPRESENTATION

Following the notation due to Pekmestzi [45], (+1, –1) representation is given by the equation for integers

\[ A = \sum_{i=0}^{n-1} (a_i) 2^i \]

where \( (a_i) = +1 \) or \(-1 \).

For fractional numbers

\[ A = \sum_{i=1}^{n} (a_i) 2^{-i} \]

The invert of \( (a_i) \) is given as

\[ \overline{(-1)} = +1 \text{ and } \overline{(1)} = -1 \]

Here logic "0" is replaced by logic (–1).

The digit \( (a_i) \) and \( a_i \) (0, 1) system is related by

\[ (a_i) = 2a_i - 1 \]

In this representation, the two states are +1 and –1 and hence it is binary representation and zero level is ignored. The positive and negative odd numbers can be represented in unified way. Zero is not representable. Quantizer
characteristic lies in the range + (1–2\(^{-b}\)) to –(1–2\(^{-b}\)) and step size is 2\(^{-b+1}\). The quantization noise is \(2^{-2b}/3\).

Truncation and rounding in this system are equivalent. Half adder is not possible and so, only full addition is possible. In full addition, we always require an extra carry bit, but taking carry bits +1 and –1 alternatively, its effect can be nullified.

This representation is different from bipolar and duobinary signals because the duobinary signals have three levels (+2, 0, –2), whereas, the bipolar signals have two levels (+V for logic 1 and –V for logic 0).

4.3 FIRST ORDER DIFFERENTIAL PHASE SHIFT KEYING

4.3.1 DPSK Modulator:

The logic circuit diagram of DPSK modulator is shown in fig. (4.1). The differential encoding of data is achieved by using XNOR operation in (+1, -1) system. The truth table for XNOR and XOR gates is shown in table 4.1. Data bit \(d(k)\) is applied to one input of XNOR gate. The output bit of XNOR gate \(b(k)\) is delayed by one bit using digital filter of first order and inverted, then feedback to other input of XNOR gate. The output bit of XNOR gate is given by

\[
b(k) = d(k) \otimes \bar{b}(k - 1) \quad \ldots \ldots (1)
\]

Since \(b(0)\) can not be derived from equation (1), therefore it is assumed either +1 or –1. When \(b(0) = -1\), the value of \(b(k)\) is inverted as compared to \(b(0) = +1\).

To clarify the idea we take an example.

Let the data bits be
\[ d(k) = 1\overline{1}1\overline{1}1\overline{1}1 \]

where \( \overline{1} = (-1) \)

Let us assume \( b(0) = +1 \),

From equation (1), we have

\[ b(k) = 1\overline{1}\overline{1}\overline{1}\overline{1}\overline{1} \]

If we consider \( b(0) = -1 \),

then \( b(k) = \overline{1}\overline{1}\overline{1}\overline{1}\overline{1}\overline{1} \)

Thus, all the bits get inverted.

The carrier wave is generated by digital oscillator. The digital carrier wave is multiplied by the \( b(k) \) by a sequential multiplier. The output of multiplier directly produces the digital modulated wave \( b(k)\cos(\Omega_0 n) \), where \( \Omega_0 = \omega_0 T_b \), \( \omega_0 \) is the frequency of carrier wave, \( T_b \) is the bit period and \( n \) is the integer given by 1,2,3 etc.

### 4.3.2 First Order Digital Filter:

The first order filter is realized by

\[ y(n) = x(n) + ay(n-1) \quad \ldots (2) \]

Where \( x(n) \) is the real data and \( ay(n-1) \) is the real data with additional bits.

To clarify the idea we take an example.

Let \[ x(n) = \frac{-3}{16} = 0.\overline{1}1\overline{1} \]

and \[ ay(n-1) = \frac{+59}{128} = 0.1\overline{1}1 \overline{1} \]
Here bits 111 are the additional bits which are to be truncated and its value is 3/128.

\[
x(n) = \begin{array}{c} 0.\overline{1}111 \\
+ ay(n-1) = +0.1\overline{1}11 \overline{1}11 \overline{1}11 \\
1.1111 \overline{1}111
\end{array}
\]

So,

\[
y(n) = 0.1\overline{1}11 = \frac{5}{16}
\]

Here the truncated bits are \(\overline{1}11 = \frac{-5}{128}\).

The MSB of truncated value is taken as input carry bit and its value is 1/16. The carry bit will not produce any error because

\[
\frac{1}{16} - \frac{5}{128} = \frac{3}{128}
\]

### 4.3.3 Complex Digital Oscillator:

The complex digital oscillator generates a cosine wave sequence and a sine wave sequence with same frequency and same amplitude [46]. It is derived from recursive digital filter structure. The basic direct form digital oscillator structure is shown in fig. (4.2).

Following the notation [46] the characteristic equation of the discrete time linear system is given by

\[
x_2(n+2) = \alpha x_2(n+1) - x_2(n)
\]

Where, \(x_1(n)\) and \(x_2(n)\) are two state variables which are related by
\[ x_1(n) = x_2(n + 1) \quad \text{.....(4)} \]

Z-transform of equation (3) is given by

\[ X_2(z) = \frac{(z^2 - \alpha z)x_2(0) + zx_1(0)}{z^2 - \alpha z + 1} \quad \text{.....(5)} \]

Where \( x_1(0) \) and \( x_2(0) \) are initial values of state variable.

From the fig. (4.2), if we select

\[ \alpha = 2 \cos \Omega_0, \quad \Omega_0 = \omega_0 T_b \quad \text{where} \quad \omega_0 \quad \text{is the frequency of oscillator.} \]

and \( x_1(0) = \sin \Omega_0, \quad x_2(0) = 0, \)

From eqn. (5), we get

\[ X_2(z) = Y(z) = \frac{z \sin \Omega_0}{z^2 - 2 \cos \Omega_0 + 1} \quad \text{.....(6)} \]

Which generates discrete time sinusoidal function as output signal.

When we select \( x_1(0) = \cos \Omega_0 \) and \( x_2(0) = 1 \)

\[ Y(z) = \frac{z^2 - \cos \Omega_0 z}{z^2 - 2 \cos \Omega_0 z + 1} \quad \text{.....(7)} \]

which produces discrete cosine function \( \cos (\Omega_0 n) \) as output signal.

### 4.3.4 DPSK Detector:

DPSK detector circuit is depicted in fig. (4.3). The input of detector circuit is \( b(k) \cos (\Omega_0 n) \). Let us select \( \Omega_0 = 2 \pi \), then \( b(k) \cos(\Omega_0 n) = b(k) \).

Thus, the carrier is suppressed. The modulated signal \( b(k) \) is delayed by one bit and inverted and finally given to one of input of XNOR gate. \( b(k) \) is applied directly to the other input of XNOR gate. The output of XNOR gate produces the required data \( d(k) \). This can be made clear with the example:
Let $b(k) = \overline{11111111}$

so, $b(k-1) = \overline{11111111}$

and $\overline{b}(k-1) = \overline{11111111}$

Now, $d(k) = b(k) \odot \overline{b}(k-1) = \overline{11111111}$

### 4.4 SECOND ORDER DIFFERENTIAL PHASE SHIFT KEYING

#### 4.4.1 D$^2$PSK Modulator:

The circuit diagram of D$^2$PSK modulator is shown in fig. (4.4). The first order differential encoded signal again differentiated in the same way to get the second order differentially encoded signal.

Let us consider the same data

$$d(k) = \overline{11111111}$$

The differentially encoded data is given by

$$b'(k) = \overline{11111111}$$

where $b'(0) = +1$.

The second order differentially encoded data is derived by the relation

$$b(k) = b'(k) \odot \overline{b}(k-1) \quad \text{......(8)}$$

It is given by

$$b(k) = \overline{11111111} \quad \text{where } b(0) = 1$$

When $b'(0) = -1,$

$$b'(k) = \overline{11111111}$$

and $b(k) = \overline{11111111}$
The second order differentially encoded signal is modulated with carrier as DPSK.

### 4.4.2 D²PSK Detector:

The circuit diagram of D²PSK detector is shown in fig. (4.5). Firstly, the carrier is suppressed by selecting $\Omega_0 = 2\pi$. The modulated signal $b(k)$ is converted to other signal $d'(k)$ by using the method DPSK detector in the first stage. The signal $d'(k)$ is converted to $\bar{d}(k)$ by using the same method in the second stage. The data $\bar{d}(k)$ is inverted to get the input data $d(k)$. To clarify this idea, we take an example.

Here, $b(k) = 1\bar{1}\bar{1}\bar{1}\bar{1}\bar{1}\bar{1}\bar{1}\bar{1}\bar{1}$

using the relation

$$d'(k) = b(k) \odot b(k-1),$$

we have $d'(k) = \bar{1}\bar{1}\bar{1}\bar{1}\bar{1}\bar{1}\bar{1}\bar{1}\bar{1}$

using the relation

$$\bar{d}(k) = d'(k) \odot d'(k-1),$$

we have

$$\bar{d}(k) = \bar{1}\bar{1}\bar{1}\bar{1}\bar{1}\bar{1}\bar{1}\bar{1}\bar{1}$$

so, $d(k) = \bar{d}(k) = 1\bar{1}\bar{1}\bar{1}\bar{1}\bar{1}\bar{1}\bar{1}\bar{1}$

This is the required data.

for $b(k) = \bar{1}\bar{1}\bar{1}\bar{1}\bar{1}\bar{1}\bar{1}\bar{1}\bar{1}$, Processing in similar manner, we have

$$d'(k) = 1\bar{1}\bar{1}\bar{1}\bar{1}\bar{1}\bar{1}\bar{1}\bar{1}\bar{1}$$

$$\bar{d}(k) = \bar{1}\bar{1}\bar{1}\bar{1}\bar{1}\bar{1}\bar{1}\bar{1}\bar{1}$$
so, \( d(k) = 11111111 \)

This is the required data.

4.5 PROBABILITY OF ERROR

Following [44] the conditional probability of error for \( D^2 \text{PSK} \) in presence of AWGN is given by

\[
p_2(\gamma_b) = \frac{1}{2} \text{erfc}\left( \sqrt{\frac{E}{N_0}} \cos (2 \eta_2 - \eta_1) \right)
\]

\[ ......(9) \]

Where \( \eta_1 \) and \( \eta_2 \) are phase angles and \( \text{erfc}(\cdot) \) is the complimentary error function for slowly Rayleigh fading channel [17]. The conditional probability is given by

\[
p_2 = \int_0^\infty p_2(\gamma_b) p(\gamma_b) d\gamma_b
\]

where \( p(\gamma_b) = \frac{1}{\gamma_b} e^{\gamma_b/\gamma_s} \)

\[ ......(10) \]

Here, \( \gamma_b = \frac{E}{N_0} E(\alpha^2) \)

where \( E(\alpha^2) \) is the average value of \( \alpha^2 \) and \( \alpha \) is an attenuation factor due to fading.

Substituting eqn. (9) into eqn. (10) and on integration we have,

\[
p_2 = \frac{1}{\sqrt{\pi}} \frac{1}{\cos(2 \eta_2 - \eta_1)} \frac{1}{2 \cos(2 \eta_2 - \eta_1)} \frac{1}{\sqrt{\pi} \cos^2(2 \eta_2 - \eta_1)} \gamma_b^2
\]

\[ ......(11) \]

The average probability of error is given by

\[
p_e = \frac{1}{2} \int_{-\pi}^{+\pi} \int_{-\pi}^{+\pi} \left[ 1 - \text{erf}\left( \frac{E}{N_0} \cos (2 \eta_2 - \eta_1) \right) \right] p(\eta_1, \eta_2) d\eta_1 d\eta_2
\]

\[ ......(12) \]

Now, \( p(\eta_1, \eta_2) = p(\eta_1) p(\eta_2) \)

\[ ......(13) \]

and
\[ p(\eta_i) = \frac{e^{-E/N_0}}{2\pi} + \frac{1}{2} \sqrt{\frac{E}{\pi N_0}} \cos(\eta_i) \exp\left(\frac{E \sin^2(\eta_i)}{-N_0}\right) \left(1 + \text{erf}\left(\frac{E}{\sqrt{N_0}} \cos(\eta_i)\right)\right) \]

\[
\ldots..(14)
\]

Here \( i = 1, 2. \)

Using equations (12), (13) & (14) and after solving the integral, we get

\[ p_e = \frac{1}{2} e^{-2E/N_0} \]

\[
\ldots..(15)
\]

All remaining integrals will vanish because the integrands contain the periodic function of \( \eta_1 \) and \( \eta_2 \) with period \( 2\pi \) and the functional dependence on \( \eta_1 \) and \( \eta_2 \) satisfy the condition

\[ g(\eta_1 + \pi) = -g(\eta_1) \quad \text{for all } \eta_1 \]

\[ g(\eta_2 + \pi) = -g(\eta_2) \quad \text{for all } \eta_2 \]

The average value of any such function over one complete period is zero.

The conditional probability of error \( p_2 \) for different average value of channel attenuation factor \( \alpha \) is shown in the fig. (4.6). From the figure it is obvious that the probability of error decreases with the increase of energy to noise ratio and it decreases sharply with the increase of \( \alpha \).

The average probability of error \( p_e(\gamma_b) \) with signal to noise ratio \( \gamma_b \) for slowly Rayleigh fading channel for DPSK and D^2PSK is illustrated in fig. (4.7). The probability of error in D^2PSK decrease with \( \gamma_b \). The average probability of error with energy to noise ratio is shown in fig. (4.8). The broken line indicates the variation of \( \log(p_e) \) with \( E/N_0 \) [44].

To improve the performance of D^2PSK, two bit delay in the second stage of modulator and two bit delay in the first stage of detector can be used [41]. The circuit diagram of encoder and decoder are shown in fig. (4.9) and fig. (4.10).
Such type of delay eliminates the high noise correlation in the receiver due to sharing of common noise. The process of encoding and decoding can be clarified with the following examples.

(1) Encoder with two bit delay:

Let \( d(k) = 11111111 \)

and \( b'(k) = 11111111 \)

Now, using the relation \( b(k) = b'(k) \odot \bar{b}(k - 2) \),

we get \( b(k) = 11111111 \)

where \( b(0) = \bar{1} \) and \( b(1) = \bar{1} \) are assumed because they cannot be calculated. There are other options for \( b(0) \) and \( b(1) \) and they are

\[
\begin{align*}
[b(0) = \bar{1}, b(1) = 1], & \quad [b(0) = 1, b(1) = 1] \quad \text{and} \quad [b(0) = 1, b(1) = \bar{1}] \\
\end{align*}
\]

For \( b(0) = \bar{1}, b(1) = 1; \)

\( b(k) = 1111111111 \)

For \( b(0) = 1, b(1) = 1; \)

\( b(k) = 1111111 \)

For \( b(0) = 1, b(1) = \bar{1}; \)

\( b(k) = 1111111111 \)

(2) Decoder with two bit delay:

We first obtain \( d'(k) \) using the relation

\( d'(k) = b(k) \odot b(k - 2) \)

Let \( b(k) = 11111111 \)

so, \( d'(k) = 11111111 \)
Using the relation
\[ d(k) = d'(k) \oplus d(k-1) \]
we get
\[ d(k) = 1\bar{1}1\bar{1} \bar{1}1\bar{1}. \]

4.6 CONCLUSION

The (+1, -1) system is well suited for differential phase shift keying (DPSK) and doubly differential phase shift keying (D²PSK). The (+1, -1) system is an alternate of two’s complement representation of (0, 1) system. In this system, there is no need of extra hardware for conversion. The positive and negative quantities are represented in a unified way. Quantizer characteristic is symmetrical, the truncation and rounding are equivalent and hence the filtering process becomes simple. The hardware realization of DPSK and D²PSK modulator and detector are simple and straight. They are completely digital. The modulator is realized by XNOR, invert first order digital filter, digital oscillator and a simple digital multiplier. In conventional system an XOR gate, a delay circuit, a level shifter and a balanced modulator which contains two multipliers, a local oscillator, a 90° phase shifter and an adder are required. Therefore, it is a combination of digital and analog circuits. On the other hand (+1, -1) system being only digital the hardware are reduced much. The process of modulation becomes fast and the possibility of error becomes low.

The detector circuit in this system is realized by first order filter and XNOR gate. In conventional binary system, it requires a delay circuit, a multiplier circuit, an integrator and a bit synchronizer. Thus, in (+1, -1) system, detector circuit is very simple and the number of hardware are reduced much. The circuit is totally digital. The carrier is suppressed by selecting the phase angle.
The processing and implementation of DPSK and $D^3$PSK is digital and hence, it is better from the point of view of space and time as compared to conventional binary system.
Table 4.1: Truth Table for XNOR and XOR Gates in (+1, –1) Representation

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>B</td>
</tr>
<tr>
<td>( \overline{1} )</td>
<td>( \overline{1} )</td>
</tr>
<tr>
<td>( \overline{1} )</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>( \overline{1} )</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>
Fig. (4.1): Logic Circuit Diagram of DPSK Modulator
Fig. (4.2): Basic Circuit Diagram of Direct form Digital Oscillator Structure
$b(k) \cos(\Omega_c n)$

**Phase Selector**

$\Omega_c = 2\pi$

1 bit delay

$d(k)$

**Fig. (4.3): Logic Circuit Diagram of DPSK Detector**
Fig. (4.4): Logic Circuit Diagram of D²PSK Modulator
Fig. (4.5): Logic Circuit Diagram of D²PSK Detector
Fig. (4.6): The Variation of Conditional Probability of Error with Energy to Noise Ratio for Different Channel Attenuation ($\alpha$)
Fig. (4.7): Average Probability of Error Versus Signal to Noise Ratio for Slowly Rayleigh Fading Channel for DPSK and $D^2$PSK
Fig. (4.8) : The Variation of Logarithm of Average Probability of Error with Energy to Noise Ratio for $D^2$PSK
Fig. (4.9) : Data Encoding of D$^3$PSK using 1 Bit and 2 Bit Delay at Modulator
Fig. (4.10) : Decoding of Data at Receiver using 2 Bit and 1 Bit Delay