Chapter 3
ELECTRICAL CHARACTERISATION OF THE GROWN CdTe CRYSTALS

3.1 Introduction
Cadmium Telluride, as a material, finds its applications in various electrical and opto-electronic fields. All these applications find their base in the electrical and optical properties of the material. Therefore, it becomes absolutely necessary to characterise the grown CdTe crystals for these properties.

The investigation on the electrical properties of the grown CdTe crystals is presented in this chapter and various electrical characterisation methods are discussed in brief. The results of these characterisations of the grown crystals are covered. Back ohmic contact of CdTe crystal with tungsten has been discussed in the latter part of the present chapter.

3.2 Electrical Characterisation
The study of the variation of electrical resistance with the temperature of the material gives an idea of the dominant conduction mechanism of charge carriers involved with in the material. The evaluation of the band gap energy will provide a clue whether the material can be made use for various applications. Hence in present investigations, the electrical characterisation of the grown CdTe crystals has been carried out. The electrical characteristics of the CdTe crystals were investigated using the following techniques.

1. van der Pauw method
2. Low temperature resistivity measurement by four-probe method using silver contacts and
3. High temperature resistivity measurement by four-probe method using pressure contacts.

The room temperature electrical behaviour of the crystals was studied through van der Pauw method and Hall effect measurement.
3.2-1 van der Pauw method

The semiconducting crystals having irregular dimensions and larger size can be investigated for their electrical behaviour through this method. The basic requirements for this method are -

a. the contacts should be at the circumference of the sample.
b. the size of the contacts should be negligibly small as compared to that of the characterising sample.
c. the contacts should be ohmic in nature.
d. the sample should be very thin as compared to its area.
e. the surface of the sample should be singly connected, i.e., the sample should be free from steps and discontinuities.
f. the sample should be flat so that the sample surface and contacts lie in the same plane and
g. the applied field should be low so that the breakdown does not occur.

If the contacts are not taken perfectly the observed results may be associated with some error. This error will be proportional to the dimensions of the contact and can be given as,

\[ \frac{\Delta \rho}{\rho} = \frac{d^2}{D^2}, \]

where \( d \) is the size of the contact and \( D \) is the size of the sample. The extent of this error depends upon,

1. the distance of contact from the circumference
2. the extension of contact on the surface and
3. the distance between successive contacts

The general circuit diagram used to measure the resistivity of the semiconducting samples along their basal plane using this method has been shown in the figure 3.1.

\[ R_{AB,CD} = R_1, \]

\[ R_1 = \frac{\text{Potential between the contacts D and C}}{\text{Current through contacts A and B}} \]

3.1
Figure 3.1 Circuit connections to the sample for the measurement of resistivity through van der Pauw method

Figure 3.2 Relationship between $f(R_1/R_2)$ and $R_1/R_2$
where $R_j$ is the potential difference $V_d - V_c$ per unit current flowing between contacts A and B. Here, the current enters the sample through contact A and leaves the sample through contact B.

Similarly, the resistance $R_{BC, DA} = R_2$ is defined as,

$$R_2 = \frac{\text{Potential between the contacts A and D}}{\text{Current through contacts B and C}}$$ \hspace{1cm} (3.2)

where, $R_i$ is the potential difference $V_A - V_D$ per unit current flowing between contacts B and C. Here, the current enters the sample through contact B and leaves the sample through contact C.

It is observed that the equation,

$$\exp\left(-\frac{\pi R_1 d}{\rho}\right) + \exp\left(-\frac{\pi R_2 d}{\rho}\right) = 1$$ \hspace{1cm} (3.3)

holds good for the semiconductors. Here $\rho$ is the specific resistivity of the semiconducting material and $d$ is the thickness of the sample. Simplification of the above equation gives,

$$\rho = \frac{\pi d}{2 \ln(2)} \left( R_1 + R_2 \right) \times f\left( R_1 / R_2 \right)$$ \hspace{1cm} (3.4)

where $f\left( R_1 / R_2 \right)$ is referred to as van der Pauw function which can be mathematically expressed as $^{11}$,

$$f\left( R_1 / R_2 \right) = 1 - \left[ \frac{R_1 - R_2}{R_1 + R_2} \right]^2 \frac{\ln(2)}{2} - \left\{ \left( \frac{R_1 - R_2}{R_1 + R_2} \right)^4 \left( \frac{\ln(2)}{2} \right)^2 - \frac{\left( \ln(2) \right)^3}{12} \right\}$$ \hspace{1cm} (3.5)

The variation of $f\left( R_1 / R_2 \right)$ with $R_1 / R_2$ has been shown graphically in the figure 3.2.

For the van der Pauw resistivity measurements, the contacts on CdTe crystals were taken as shown in the figure 3.1 using highly conducting silver paste. The current was passed between A and B, and the potential difference was measured between the terminals D and C and the resistance, $R_1$, was calculated. Thereafter resistance $R_2$ was measured by passing the current between B and C and the voltage measured between A and D. These two values of resistances were considered for the calculation of the resistivity of the
sample and this value of the resistivity was later on used to study the effect of magnetic field on the conduction behaviour through Hall effect experiment.

3.2-1.1 Results

The electrical resistivity of the CdTe crystal was carried out on a sample of thickness around 0.014 cm. The results of the measurement are presented in the table 3.1.

**Table 3.1 – Results of van der Pauw resistivity measurement**

<table>
<thead>
<tr>
<th>R_1 = R_{abcd} (kΩ)</th>
<th>R_2 = R_{boda} (kΩ)</th>
<th>R_1 / R_2</th>
<th>f(R_1 / R_2)</th>
<th>ρ x 10^3 (Ω cm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>108.00</td>
<td>56.00</td>
<td>1.929</td>
<td>0.990</td>
<td>5.151</td>
</tr>
<tr>
<td>100.67</td>
<td>50.00</td>
<td>2.013</td>
<td>0.985</td>
<td>4.708</td>
</tr>
<tr>
<td>105.71</td>
<td>45.71</td>
<td>2.313</td>
<td>0.967</td>
<td>4.645</td>
</tr>
<tr>
<td>106.25</td>
<td>42.50</td>
<td>2.500</td>
<td>0.956</td>
<td>4.509</td>
</tr>
<tr>
<td>104.44</td>
<td>40.00</td>
<td>2.611</td>
<td>0.949</td>
<td>4.347</td>
</tr>
<tr>
<td>102.00</td>
<td>38.00</td>
<td>2.684</td>
<td>0.945</td>
<td>4.194</td>
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<td>101.82</td>
<td>36.36</td>
<td>2.800</td>
<td>0.938</td>
<td>4.109</td>
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<td>103.33</td>
<td>35.00</td>
<td>2.952</td>
<td>0.929</td>
<td>4.074</td>
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<td>103.08</td>
<td>33.85</td>
<td>3.045</td>
<td>0.923</td>
<td>4.009</td>
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<td>102.86</td>
<td>32.86</td>
<td>3.130</td>
<td>0.918</td>
<td>3.953</td>
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<td>104.00</td>
<td>32.00</td>
<td>3.250</td>
<td>0.912</td>
<td>3.932</td>
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<td>103.75</td>
<td>31.25</td>
<td>3.320</td>
<td>0.908</td>
<td>3.886</td>
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<td>102.35</td>
<td>30.59</td>
<td>3.346</td>
<td>0.906</td>
<td>3.820</td>
</tr>
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<td>103.33</td>
<td>30.00</td>
<td>3.444</td>
<td>0.901</td>
<td>3.809</td>
</tr>
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<td>104.21</td>
<td>29.47</td>
<td>3.536</td>
<td>0.896</td>
<td>3.798</td>
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<td>105.00</td>
<td>29.00</td>
<td>3.621</td>
<td>0.891</td>
<td>3.787</td>
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<td>104.76</td>
<td>28.57</td>
<td>3.667</td>
<td>0.888</td>
<td>3.758</td>
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<td>104.54</td>
<td>28.18</td>
<td>3.710</td>
<td>0.887</td>
<td>3.732</td>
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<td>103.48</td>
<td>27.83</td>
<td>3.719</td>
<td>0.886</td>
<td>3.690</td>
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<td>104.17</td>
<td>27.50</td>
<td>3.788</td>
<td>0.883</td>
<td>3.685</td>
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<td>104.80</td>
<td>27.20</td>
<td>3.853</td>
<td>0.879</td>
<td>3.680</td>
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<td>104.62</td>
<td>26.92</td>
<td>3.886</td>
<td>0.878</td>
<td>3.660</td>
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<td>104.81</td>
<td>26.67</td>
<td>3.931</td>
<td>0.875</td>
<td>3.649</td>
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<td>105.71</td>
<td>26.43</td>
<td>4.000</td>
<td>0.872</td>
<td>3.653</td>
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<td>106.90</td>
<td>26.21</td>
<td>4.079</td>
<td>0.868</td>
<td>3.663</td>
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<tr>
<td>106.66</td>
<td>26.00</td>
<td>4.103</td>
<td>0.867</td>
<td>3.646</td>
</tr>
<tr>
<td>106.45</td>
<td>25.81</td>
<td>4.125</td>
<td>0.866</td>
<td>3.630</td>
</tr>
<tr>
<td>105.88</td>
<td>24.12</td>
<td>4.390</td>
<td>0.853</td>
<td>3.516</td>
</tr>
<tr>
<td>106.00</td>
<td>24.00</td>
<td>4.417</td>
<td>0.852</td>
<td>3.511</td>
</tr>
<tr>
<td>105.95</td>
<td>23.24</td>
<td>4.558</td>
<td>0.845</td>
<td>3.463</td>
</tr>
<tr>
<td>104.50</td>
<td>22.00</td>
<td>4.750</td>
<td>0.837</td>
<td>3.357</td>
</tr>
</tbody>
</table>

Average ρ = 3.954 x 10^3 Ω cm
Using the values of $R_1$ and $R_2$ and equation 3.4, the resistivity of the sample was calculated and also given in same table. The average value of the resistivity was found to be $3.954 \times 10^3 \ \Omega \ \text{cm}$.

### 3.2-2 Hall Effect Measurement

Hall Effect measurement is a tool for the estimation of mobility and concentration of the majority charge carriers within the semiconducting sample. When a current carrying semiconductor is placed in a transverse magnetic field, an electric field called the Hall field $E_H$ appears in a direction perpendicular to both the magnetic field and the current flow. This phenomenon appears in both semiconductors as well as conductors. The Hall effect phenomenon has been studied here using the standard van der Pauw technique $^{11}$.

For the Hall effect investigations, a slight modification of the circuit in figure 3.2, is made as shown in figure 3.3(a), to facilitate the measurement of voltage across and the current between the diagonally opposite contacts $^{11}$. The sample for this measurement was kept between the two poles of a magnet and the known magnetic field was applied using an electromagnet (type EMPS - 5, Omega Electronics, Jaipur). This magnetic field modifies the path of electrons in the sample thereby producing the voltage known as Hall voltage. The result obtained through these measurements can be further used to find out the values of carrier concentration, Hall mobility, and the Hall coefficient using the relations -

$$\mu = \frac{t}{\Delta B} \times \frac{\Delta R}{\rho},$$ 3.6

$$\eta = \frac{1}{R_H \times e},$$ 3.7

and

$$R_H = \mu \times \rho$$ 3.8.

### 3.2-2.1 Results

The parameters like mobility of the carriers, carrier concentration, and conductivity of the sample were evaluated for the CdTe samples using the modified van der Pauw technique.
Figure 3.3(a) Circuit connections for Hall effect measurement

Figure 3.3(b) Hall effect apparatus
Figure 3.4 Variation of Hall voltage with current for $B = 7.75$ kG

Figure 3.5 Variation of Hall voltage with current for $B = 10.51$ kG
Table 3.2: Results of Hall effect measurement carried out on CdTe sample

<table>
<thead>
<tr>
<th>Magnetic field (kG)</th>
<th>$R_H$ (cm$^3$/Coulomb)</th>
<th>Carrier Concentration $\eta$ (cm$^{-3}$)</th>
<th>Mobility $(\text{cm}^2/\text{V sec})$</th>
<th>Conductivity $(\Omega \text{cm})^{-1}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>7.75</td>
<td>566.617</td>
<td>$1.103 \times 10^{16}$</td>
<td>0.143</td>
<td>$2.529 \times 10^{-4}$</td>
</tr>
<tr>
<td>10.51</td>
<td>438.520</td>
<td>$1.425 \times 10^{16}$</td>
<td>0.110</td>
<td>$2.529 \times 10^{-4}$</td>
</tr>
<tr>
<td>11.79</td>
<td>373.370</td>
<td>$1.425 \times 10^{16}$</td>
<td>0.094</td>
<td>$2.529 \times 10^{-4}$</td>
</tr>
</tbody>
</table>

Figure 3.6 Variation of Hall voltage with current for $B = 11.79$ kG

Resistivity, $\rho = 3.954 \times 10^3 \Omega \text{ cm}$

Thickness $= 0.057 \text{ cm}$. 

\[ 60 \]
discussed above. The schematic diagram of the Hall effect measurement setup is shown in figure 3. 3(b). The measurement is carried out for the sample of thickness 0.057 cm by varying the current passing through the sample and measuring the Hall voltage for different applied magnetic field. Plotting graphs for the different applied magnetic fields, between the current passed through the sample and the measured Hall voltage, the various parameters of the grown CdTe crystal were found out (figure 3. 4, 3. 5 and 3. 6). The results of the Hall effect experiment carried out for the grown CdTe sample have been given in the table 3. 2. These results agree well with the reported values /3-5/. The conductivity of the sample measured supports the results of van der Pauw measurements.

3. 2-3 Variation of Resistance with Temperature
The resistance measurements would give an insight into the electronic distribution of the material and enable us an understanding on the band gap and activation energies. These two properties would enable us to make use of them for different electrical, optoelectrical and optoelectronic applications. Besides, the one-dimensional or three dimensional charge transport mechanisms involved in the samples can also be investigated through these kinds of measurements. The resistance measurements at both low and high temperatures were carried out using four-probe method. Four-probe method for surface resistivity measurement was chosen in present investigation so that the potential gets spread through out the surface of the crystal.

3. 2-3.1 Low Temperature Resistance Measurement
The variation of the electrical resistance of CdTe crystals with temperature below room temperature, in a range from 173K to 293K was investigated in present case using the standard four-probe method. The experimental setup for the same has been discussed here.

3. 2-3.2 Experimental Setup
The cryostat LN – DP used for the measurement was designed for temperatures of the range from 173K to 293K. This portable cryostat consists of a sample chamber and a
Figure 3.7 The cryostat LN - OP, for low temperature resistivity measurements

Figure 3.8 Sample holder
Figure 3.9 Schematic diagram of low temperature resistance measurement setup
sample holder as shown in figure 3. 7. It was designed to fit directly into any of the standard liquid nitrogen storage containers. The system was supplied with a standard half inch valve for introducing the exchange gas, vacuum gauge etc. The sample holder consisted of a gold-plated copper assembly, mounted with a standard platinum thermometer (Pt-100), and a heater, which was used for temperature control. Electrical leads for the thermometer and the heater were brought at the top of the cryostat at a D-25 type pin connector. The samples were mounted on the sample holder with a low temperature conducting Apiezone-N grease which would enable thermal heating of the samples, as shown in the figure 3. 8. Sixteen permanent electrical points were available for the experiments at the D-type 25 connector.

The four probe contacts were taken using silver paste. As excessive heating may damage the sample holder, electrical insulation from pin to pin may break down, only a low power 10W soldering iron has to be used. The various samples could be selected using the sample changer SMC-4. A constant current source CCS-10 was thought to be ideal for providing power for a wide range of transducers and other four probe resistivity measurements where a stable but variable constant current is the basic requirement. The heater power supply CCH-1000 was used as a heater supply for a 30-40 Ω heater, which was capable of supplying a maximum power of 25W to the heater and was capable for cryogenic purposes.

The samples were mounted on the sample holder and the electrical connections were taken properly. After cleaning the ‘O’ ring joint at the top of the cryostat, the sample holder was inserted in the sample chamber and the clamp was tightened gently. The pumping valve was closed after evacuating the sample chamber to a vacuum of around $1 \times 10^{-2}$ Torr using a rotary vacuum pump. The entire assembly was inserted and fixed in a liquid nitrogen container. The sample holder takes only a few minutes to reach 77 K. At a time, four different specimens were mounted on the sample holder. A constant current was passed through the outer leads of the specimen and the developing voltage across the inner leads was measured. The schematic diagram of the experimental setup has been shown in figure 3. 9. After the completion of the experiment, the entire assembly was
Figure 3.10(a1) Variation of \( \ln (R / R_0) \) with \( 1/T \) for CdTe sample - 1

Figure 3.10(a2) Variation of \( \ln (R / R_0) \) with \( 1/T \) for CdTe sample - 1
Figure 3.10(b1) Variation of Ln (R / R₀) with 1/T for CdTe sample - 2

Figure 3.10(b2) Variation of Ln (R / R₀) with 1/T for CdTe sample - 2
Figure 3. 10(C1) Variation of $\ln \left( \frac{R}{R_0} \right)$ with $1/T$ for CdTe sample - 3

Figure 3. 10(C2) Variation of $\ln \left( \frac{R}{R_0} \right)$ with $1/T$ for CdTe sample - 3
Figure 3.10(d1) Variation of Ln (R / R₀) with 1/T for CdTe sample - 4

Figure 3.10(d2) Variation of Ln (R / R₀) with 1/T for CdTe sample - 4
pulled out and the system was allowed to cool to the room temperature before the sample chamber was opened.

3.2-3.3 Results
The variation in the resistance of the CdTe samples was investigated over a temperature range of 173K to 293K. The investigations were carried out on four different samples. Graph of Ln \((R/R_0)\) vs. \(1/T (K^{-1})\) were plotted for all the samples. The graphs of different samples were found to be linear and are shown in figure 3.10 (a)-(d). From the slopes of the linear plots, the activation energies of all the samples were calculated and the value of the activation energy of the grown CdTe over the temperature range 173K to 293K was found to be around 0.06 eV for all the samples.

3.2-4 High Temperature Resistivity Measurement
Since CdTe is generally known to be a semiconducting material, its resistivity is supposed to decrease with increasing temperature. To confirm this in present case, a four-probe method was employed, wherein the pressure contacts were used to facilitate the application of current and the measurement of voltage over a wide range of temperature, from 303 K to 973 K. The experimental setup used for these measurements is discussed below.

3.2-4.1 Experimental Setup
A variable temperature resistivity measurement system, model VTRM – 408, Scientific Solutions, Mumbai, was specially designed for the measurement by which we could go up to 700°C. The schematic diagram of the variable temperature resistivity measurement system (VTM – 408) is shown in figure 3.11.

The high temperature resistivity measurement setup consists of the following five units:
1. Sample holder
2. Furnace
3. Furnace controller
4. Constant current source and
5. Data acquisition source
Figure 3.11 Schematic diagram of high temperature resistivity measurement setup
Figure 3.12(a) Block diagram of power supply for high temperature resistivity measurement setup

Figure 3.12(b) Programmable furnace controller block diagram
Figure 3.13 Sample holder assembly

Figure 3.14 Sample holder
The temperature range over which the VTRM - 408 could carry out the measurements was between 25°C to 700°C with a stability of ±1°C. The power of the furnace for 700°C was 250W.

The sample under measurement was sandwiched between two flat alumina plates. Four parallel stainless steel wires which were properly positioned on the sample act as four probes. Sample holder encased by a quartz tube was placed inside a tubular furnace. Provisions were kept in the VTRM - 408 instrument to conduct experiments in air, low vacuum or flowing gas. Voltage and current leads were brought out of the furnace in a D-type 9-pin connector for further connections.

Sample temperature was controlled within ±1°C in the specified range for the time periods from few minutes to days using the matched furnace controller supplied with the system. The furnace controller was a programmable digital PID type temperature controller with 10 second PWM output for furnace power supply. A ‘Heater LED’ on the front panel could indicate the status of the furnace. The temperature inside the furnace was monitored using thermocouple TC1. Block diagrams of the furnace controller and the flowchart of the programmable furnace controller are shown in figure 3.12(a) and (b). The e.m.f. generated from the thermocouple was compensated for room temperature correction and was converted to practical unit °C by digital conversion technique. The target temperature to be set and the other control parameters were to be entered via the panel keyboard. A 3-range voltmeter was also coupled to the controller. The sensor temperature, set temperature and voltmeter readings were displayed on an alphanumeric display unit.

The furnace controller could be operated in two different modes – Step Mode and Sweep Mode. In the Step Mode, the temperature of the furnace was controlled to any desired temperature value within ±1°C, when proper PID values are selected. In the Sweep Mode, the furnace temperature was continuously incremented to any temperature from the lowest (25°C) to the maximum temperature (700°C) at different sweep rates, say, 1°C per minute to 10°C per minute.
The sample holder assembly consisted of two parts—a quartz tube and the sample holder as shown in the figure 3.13. Sample holder was inserted from right end of the quartz tube and could be clamped to it using a NW - 40QC clamp. The thermocouple was inserted from the other end through a nylon neck of the tube. A gas flow or vacuum could be handled through this end.

The sample holder assembly was made up of stainless steel tubes flanges, which could easily withstand 700°C. Thin (40 SWG) stainless steel wires were used as electrical probes. They were brought near the sample through a dual hole ceramic tubes located inside the supporting stainless steel tubes.

The stainless steel wires were properly positioned and aligned on the lower alumina plate. Over this arrangement, the semiconductor sample was placed. This sample was then sandwiched between the lower and upper alumina plates using a spring-loaded plunger (figure 3.14). The constant current was passed through the outer leads while the voltage was measured between the inner leads with change in temperature. All the four electrical leads were brought out of the sample holder in a D-type 9-pin connector. Connections to the current source and the voltmeter were made by extending electrical wires from this connector. A 3 ½ digit, 3 range built-in voltmeter in the furnace controller unit measured the voltages from 20 mV to 2000 mV with 10μV resolution for the lowest range. The measurement range can be selected from the front panel switch. Reading on the voltmeter was available on the remote data acquisition personal computer via RS – 232 interface lines, which contained information about the sensor temperature, set temperature, percentage power, voltmeter reading and whether the controller action is off or on.

Setting proper PID values in the menu, the furnace was heated and the temperature was increased in accordance with the selected sweep rates. A Q-Basic program directly converted the measured values of voltages within the inner terminals in terms of resistance values.
3.2-4.2 Results

The variation of electrical resistivity of CdTe crystals (grown in the present investigations) with temperature was investigated using the above discussed setup in the temperature range 300K to 835K. It is a well-known fact that the electrical resistivity of semiconductors depends on the temperature T according to the following relation:

\[ \rho = \rho_0 \exp\left(\frac{E_g}{2k_B T}\right), \]

where \( \rho_0 \) is the resistivity at 0 K, \( E_g \) is the band gap energy of the material and \( k_B \) is the Boltzmann constant. Therefore, if we plot the graph of \( \ln\left(\frac{\rho}{\rho_0}\right) \) vs. \( \frac{1}{T} \), we can evaluate the value of the band gap of the material. In case of the grown CdTe, the graph \( \ln\left(\frac{\rho}{\rho_0}\right) \) vs. \( \frac{1}{T} \) was plotted for the above mentioned temperature range and is shown in figure 3.15. The nature of the graph clearly gives an indication that CdTe investigated here possesses semiconducting nature. Using the slope of the variation in high temperature region of figure 3.16 (706K - 720K), the energy gap has been calculated and is found to be around 1.45 eV, which matches with the earlier reports \(^{16,71}\).

In this temperature region, the semiconductor exhibits the intrinsic behaviour whereas for lower temperatures, the extrinsic behaviour is observed. The variation of electrical resistivity of CdTe crystals with temperature in lower temperature range was investigated with more interest to understand the type of conduction mechanisms involved. The low temperature electrical resistivity is always influenced by some important phenomena like the nearest neighbour hopping process of the carriers, the presence of excitons and their influence on the conduction mechanism, the back relaxation etc. Efforts have been made to investigate the influence of all these mechanisms on the electrical conductivity of the grown CdTe samples by selecting the lower temperature region of figure 3.15. According to Pollak and Knotek \(^{18}\) the electrical resistivity may find a dominance of the nearest neighbour hopping of carriers at moderate temperatures which result into the reduction of activation energy of the materials. Hence, a graph of \( \ln\left(\frac{\rho}{\rho_0}\right) \) vs. \( \frac{1}{T} \) was plotted for temperatures between 493K and 544K and is shown in figure 3.17. It is quite
Figure 3.15 Variation of $\ln(\rho / \rho_0)$ with $1/T$ for CdTe

Figure 3.16 Variation of $\ln(\rho / \rho_0)$ with $1/T$ for CdTe
Figure 3.17 Variation of \( \ln \left( \frac{\rho}{\rho_0} \right) \) with \( 1/T \) for CdTe

Figure 3.18 Variation of \( \ln \left( \frac{\rho}{\rho_0} \right) \) with \( 1/T \) for CdTe
Figure 3.19 Variation of $\ln (\rho / \rho_0)$ with $1/T$ for CdTe

Figure 3.20 Variation of $\ln (\rho / \rho_0)$ with $1/T$ for CdTe
Region 1: $E_g = 1.45 \text{ eV}$
Region 2: $E_a = 0.198 \text{ eV}$
Region 3: $E_a = 0.139 \text{ eV}$
Region 4: $E_a = 0.045 \text{ eV}$
Region 5: $E_a = 0.029 \text{ eV}$

Figure 3.21: Variation of $\ln (p/p_0)$ with $1/T$ for CdTe
Figure 3.22 Variation of $\ln \left( \frac{p}{p_0} \right)$ with $\ln T$ for CdTe

Figure 3.23 Variation of $\ln \left( \frac{p}{p_0} \right)$ with $\ln T$ for CdTe
Figure 3.24 Variation of $\ln (\sigma)$ with $\ln (T - T_c)$ for CdTe

Figure 3.25 Variation of $\ln (\ln (\sigma))$ with $\ln (T - T_c)$ for CdTe
apparent from this figure that $\ln\left(\frac{\rho}{\rho_0}\right)$ varies linearly with inverse of temperature. The slope of this linear variation has been used to find out the value of the activation energy. Corresponding to this temperature region, the activation energy was found to be around 0.198 eV which is a low value indicating the presence of hopping of carriers among the nearest neighbouring level.

Knotek and Pollak also explained the influence of excitonic mechanism on the activation energy of the material. According to them, the activation energy is found to decrease as the temperature decreases due to the excitonic mechanisms. In present investigations, the efforts have been made to study the influence of such excitonic mechanisms on the relationship of electrical resistivity with temperature. In this direction, different graphs of $\ln\left(\frac{\rho}{\rho_0}\right)$ vs. $\frac{1}{T}$ corresponding to temperature ranges 432K -
490K, 362K – 409K and 340K – 361K are plotted and shown in figures 3.18, 3.19 and 3.20 respectively. All these graphs show the linear variation of resistivity with temperature. Using the slope of these linear variations, the activation energies corresponding to the temperature ranges 432K – 490K, 362K – 409K and 340K – 361K have been calculated and found to have values 0.139 eV, 0.045 eV and 0.029 eV respectively. Thus, it is observed that the activation energy goes on decreasing at lower temperatures up to 340K. This is a clear indication of the influence of excitonic mechanism on the electrical conduction behaviour of CdTe material in temperature range 490K-340K /9/. This is a characteristic feature of quasi – one and two dimensional system/10/. Thus it can be inferred that, for the above mentioned temperature range the conduction mechanism in CdTe material is observed to follow the quasi – one and two dimensional system behaviour. So, this mechanism can be either because of the exciton mechanism or the onset of correlated hopping process effective in the system in this temperature range /8/. The systematic reduction in the activation energy investigated above has been shown in figure 3.21 for the full range of temperature, 340K – 544K.

In semiconductors, it is a general trend that initially the resistivity decreases as the temperature increases which is an indication of the fact that the extrinsic mechanism effectively governs the conduction process. After certain temperature, the resistivity starts increasing with temperature which is analogous to the conduction mechanism in metals. But it cannot be said that this increasing trend of resistivity exhibits the metallic behaviour of the semiconducting material. This is actually a result of the transition of the conduction mechanism from extrinsic to intrinsic behaviour, which is a normal feature of any doped semiconductor. The electrical resistivity of the semiconductor in this transition region can be expected to be dominated by the back relaxation mechanism. This phenomenon can be investigated if the variation of resistivity with temperature for this transition region can be analysed stepwise.

In present investigations, if we carefully observe the plot of \( \ln \left( \frac{\rho}{\rho_0} \right) \) vs. \( \frac{1}{T} \) shown in figure 3.15, it can be seen that the resistivity increases with temperature in the range
603K to 706K. In light of the above discussion, this variation is systematically analysed here. The Einstein’s power law for the metallic behaviour of materials is given by $\rho = A T^n$, where $A$ is a constant and $n$ is an integer. Hence if we plot a graph of $\ln\left(\frac{\rho}{\rho_0}\right)$ vs $\ln T$, it is expected to get a straight line. A graph of $\ln\left(\frac{\rho}{\rho_0}\right)$ vs $\ln T$ for the temperature range 603K to 706 K for the CdTe sample is shown in figure 3.22, which is just an enlarged version of the transition region observed in figure 3.15. From this figure, it is quite evident that, the electrical resistivity does not show a linear dependence on temperature, but this variation is found to be step wise in nature. This may be assigned to the Coulomb repulsion process among the charge carriers and among the broad excited levels which leads to a back relaxation of carriers to the lower levels. If a best linear fit is used in this region, a straight line can be drawn as shown in figure 3.23, of which the slope comes out to be 0.9. Ideally this slope should be unity according to the Einstein’s model. This variation can also be considered as the signature of optical phonon energy in such behaviour. So it is possible that some electron–phonon coupling may be present and the overall dispersion curve of the lattice vibrations can be deconvoluted into their Fourier components. These components can also lead to the discrete steps as found in figure 3.22.

Normally, in almost all semiconductor materials, the variation of electrical resistivity with temperature exhibits the intrinsic behaviour which is quite obvious also. According to Kirkpatrick, the intrinsic mechanism of conduction behavior of semiconductors at high temperatures may have an influence of beta distribution which is expected to follow the relation $\sigma = A + B T^* \left(1 - T^*\right)^{3/2}$, where, $T^* = (T - a) / b$ and $a$, $b$, $A$ and $B$ are constants. To observe this influence, it is essential to have large number of data for the above mentioned electrical behaviour in the intrinsic range. To verify the above concept whether present in CdTe case or not, a graph of $\ln \sigma$ vs. $\ln (T - T_C)$ is plotted in a temperature range 706K to 720K for verifying the relation $\sigma \sim (T - T_C)^{1/12}$ and is shown in figure 3.24. Here $T_C$ is actually the temperature related to the point of transition from where the electrical conduction behaviour changes from extrinsic one to the intrinsic one. In the present investigations, the value of $T_C$ is found to be 706 K as evident from figure.
3. 15. As per Kirkpatrick model\textsuperscript{1121}, the exponent '$t'$ which can of course be evaluated from the variation of $\sigma \sim (T - T_c)^t$ should have a value around 0.2. If this is true, then the system can be thought of as following the separated atomic system model and this can also be termed as the localised charge carrier system or the quantum dot system, where each energy level is completely isolated from the other levels. In present investigations, from the slope of $\ln \sigma$ vs. $\ln (T - T_c)$ (figure 3. 24), the value of '$t'$ is found to be around 0.11, which very largely deviates form the expected value (0.2) as per the Kirkpatrick model. This is an indication of the fact that the zero dimensional model is a complete misfit in our case at high temperatures. Therefore it is expected that at high temperatures, the electrical conduction mechanism may be following the one-dimensional or two-dimensional model.

From figure 3. 15, it is quite apparent that the high temperature tail as well as the low temperature tail of the variation of $\ln \left( \frac{\rho}{\rho_0} \right)$ vs. $\frac{1}{T}$ is found to be almost nonvariable. For further analysis, this flat region on both sides of the variation has been neglected. Thus a graph of $\ln (\ln \sigma)$ vs. $\ln T$ is plotted of the CdTe sample in the temperature range 331K - 771K as shown in figure 3.25. According to Mott\textsuperscript{13,14}, the variation of electrical conductivity with temperature follows the equation, $\sigma = \sigma_0 \exp \left[ -\left( \frac{T_0}{T} \right)^{1/4} \right]$, where, $\sigma_0$ and $T_0$ are constants. The slope of $\ln (\ln \sigma)$ vs. $\ln T$ should be $\frac{1}{4}$ ($= 0.25$) in ideal conditions. In present case, this slope is observed to be 0.249 which is very close to the standard value. This reveals that Mott's variable range hopping model governs the conduction behaviour of CdTe samples investigated here over a large range of temperature, which is also evident from a very good straight line shown in figure 3. 25 (in temperature range 331K - 771K). According to the same model and of the work of H. Bottger and B. V. Bryksin (1985)\textsuperscript{15}, for a linear temperature range discussed above, the density of states near the Fermi level should be constant. From the above discussion it is confirmed that the Mott model is applicable in this case. Therefore, a graph of $(\ln \sigma)$ vs. $T^{-1/4}$ is plotted for CdTe samples and to confirm the independence of the density of
Figure 3.27 Variation of $\sigma$ with temperature for CdTe

Figure 3.28 Variation of $\ln \sigma$ with $(T - T_0)^2$ for CdTe
Figure 3.29 Variation of $\ln \sigma T$ with $1/T$ for CdTe

Figure 3.30 Variation of $\ln \sigma T^2$ with $1/T$ for CdTe
Figure 3.31 Variation of $\ln \sigma T^{3/2}$ with $1/T$ for CdTe

Figure 3.32 Variation of $\ln \sigma T^{1/2}$ with $1/T$ for CdTe
Figure 3.33 Variation of $\ln \sigma T$ with $1/T$ for CdTe

Figure 3.34 Variation of $\ln \sigma T^{1/2}$ with $1/T$ for CdTe
Figure 3.35 Variation of $\ln \sigma T^{3/2}$ with $1/T$ for CdTe

Figure 3.36 Variation of $\ln \sigma T^{3/4}$ with $1/T$ for CdTe
energy states near the Fermi level. Such a graph is shown in figure 3.26. At a first glance this graph does not seem to be an absolute linear variation, but the linear best fit can be thought of as a good straight line approximation over the temperature range 331K – 771K. Since this temperature range is very large such small deviations are expected. The almost linear variation of \((\ln \sigma) vs. \frac{1}{T}\) indicates that the density of states is independent of energy near the Fermi level.

Since CdTe is a known semiconductor exhibiting the electronic conduction behaviour, efforts have been made to confirm the same and to show the absence of the effect of ionic conduction behaviour on the overall conduction mechanism. In this direction, the generalisation of a typical semiconductor relation can be written as \(^{11,15/}\),

\[ \ln \sigma = \ln \sigma_0 - \frac{E_g}{2k_B} \left( \frac{1}{T} - \frac{1}{T_0} \right) + \frac{1}{2k_B} \frac{dE_g}{d \frac{1}{T}} \left( \frac{1}{T} - \frac{1}{T_0} \right)^2, \]  

which is a resultant of the original equation of \(\ln \sigma = \ln \sigma_0 - \frac{E_g}{2k_B T}\). Here the second order expansion in the Taylor series has been taken into account. According to this expanded equation, a large Gaussian should be observed in the variation of \(\ln \sigma vs. \frac{1}{T}\). There are different possibilities involved in this variation. Single Gaussian reveals the electronic conduction mechanism indicating the conduction through the single lattice, whereas, two Gaussians show the presence of sub-lattices which is actually observed in case of ionically conductive materials like barium hydrogen phosphate \(^{16/}\). In present investigations, such plots are shown in figures 3.15 and 3.27 for the temperature range 331K – 771K. Now if we assume \(S = U / T\) and \(S_0 = U / T_0\), where \(U\) is the internal energy and \(S\) is the entropy, the equation of conductivity can be rewritten as \(^{16/}\)

\[ \sigma = \sigma_0 \exp \left[ - \frac{(S - S_0)^2}{2M_s} \right], \]  

where

\[ \frac{1}{2M_s} = \frac{1}{2k_B} \left( \frac{dE_g}{d \frac{1}{T}} \right) \]  

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Equation 3.11 shows that the conductivity is a gaussian in entropy. Defining a thermo
dynamical conjugate of S as a Fourier conjugate through \( \sigma(T) = \int e^{iST/v_0} \sigma(S) dS \), we
get the Fourier transform of a Gaussian which is also to be a Gaussian and thus –

\[
\sigma = \sigma_0 \exp \left[ -\frac{(T - T_0)^2}{2M_*} \right]. \tag{3.12}
\]

If equation 3.12 is valid, the graph of \( \ln \sigma \) vs. \( (T - T_0)^2 \) should be a straight line, which
means that, there is only one gaussian present in the system, asserting the electronic conduction mechanism in a material. Such a plot for CdTe sample over a wide range of
temperature from 331K – 771K has been shown in the figure 3.28. This figure clearly
shows a straight line which confirms the electronic conduction behaviour dominating in
CdTe material.

So far, the effect of temperature on the electrical conduction in CdTe samples has been
discussed in detail. But the mobility of charge carriers has not taken into account. Here,
the efforts have been made to study the dependence of mobility on temperature on the
basis of which the transport mechanism of carriers has been predicted like whether it is 1-
D or 2-D or 3-D.

For a general 3-D conductor\(^{11}\), the conductivity can be given as –

\[
\sigma_i = n e (\mu_e + \mu_h)
\]

\[
= Z e \left( \frac{k_B T}{2 \pi \hbar^2} \right)^{3/2} (m_e m_h)^{1/4} \exp \left[ -\left( \frac{E_g}{2k_B T} \right) \right] (\mu_e + \mu_h) \tag{3.13}
\]

where, \( n = Z \left( \frac{k_B T}{2 \pi \hbar^2} \right)^{3/2} (m_e m_h)^{1/4} \exp \left[ -\left( \frac{E_g}{2k_B T} \right) \right] \).

\[ \tag{3.14} \]

According to Bardeen and Shockley\(^{17}\), if there is a scattering of carriers by the acoustic
phonons present in the lattice, the mobility is expected to follow the relation \( \mu \propto T^{-3/2} \)
and the conductivity can be given as \( \sigma = A \exp \left( -\frac{E_g}{2k_B T} \right) \), where A is a constant. But if
other scattering mechanisms like, scattering by optical phonons, inter valley scattering, inter band scattering etc. are also effective, the mobility exhibits the temperature dependence as $\mu \propto T^{-5/2}$ and the equation for conductivity may be re-written as

$$\sigma = AT^{-1} \exp \left( \frac{-E_g}{2k_BT} \right).$$

To confirm the influence of various scattering mechanisms, a graph of $\ln(\sigma T)$ vs $1/T$ has been plotted for CdTe sample and shown in the figure 3.29.

For a one dimensional semiconductor, $\sigma$ can be written as –

$$\sigma = n \mu e$$

$$= e \mu N_0 \left( \frac{2m^*}{\hbar} \right)^{1/2} (k_BT)^{3/2} \exp \left( -\frac{E_g}{2k_BT} \right)$$

where $n = N_0 \left( \frac{2m^*}{\hbar} \right)^{1/2} (k_BT)^{3/2} \exp \left( -\frac{E_g}{2k_BT} \right)$ and $N_0$ is the number of chains per unit area. If the effect of acoustic phonon scattering on the electrical conduction is present, then the mobility dependence on temperature exhibits the relationship $\mu \propto T^{-3/2}$ and the equation 3.15 for the conductivity can be written as –

$$\sigma \propto T^{-3/2} \exp \left( -\frac{E_g}{2k_BT} \right)$$

$$\propto T^{-3} \exp \left( -\frac{E_g}{2k_BT} \right)$$

where, the dependence of mobility on temperature has been taken into account. Accordingly a graph of $\ln (\sigma T)$ vs. $1/T$ has been plotted for CdTe samples and shown in the figure 3.29.

The presence of optical scattering mechanism leads to the dependence of mobility on temperature as $\mu \propto T^{-5/2}$ and accordingly the conductivity is written as,
\[ \sigma \propto T^{-3/2} T^{1/2} \exp \left( -\frac{E_g}{2k_B T} \right) \tag{3.17} \]

\[ \propto T^{-2} \exp \left( -\frac{E_g}{2k_B T} \right) \]

A graph \( \ln(\sigma T^2) \) vs. \( 1/T \) has been plotted and shown in figure 3.30.

From the careful observation of figures 3.29 and 3.30, it can be concluded that the nature of the deviation is almost non-linear which indicates the fact that the conduction mechanism in CdTe sample investigated here has a negligible influence of optical phonon scattering, inter valley scattering or inter band scattering because if these scattering are dominant, then the above graphs should be straight lines.

If the mobility is independent of temperature, there are three cases that can arise:

1. For a 3D semiconductor, a graph of \( \ln(\sigma T^{-3/2}) \) vs. \( 1/T \) should be a straight line.
2. For a 1D semiconductor, a graph of \( \ln(\sigma T^{-1/2}) \) vs. \( 1/T \) should be a straight line.
3. For a 2D semiconductor like layered materials, a graph of \( \ln(\sigma T^{-1}) \) vs. \( 1/T \) should be a straight line.

From the present investigations, the above mentioned three graphs for CdTe sample have been plotted and shown in figures 3.31, 3.32 and 3.33 respectively.

If the acoustic phonons lead to the scattering of conducting carriers, the graph of \( \ln(\sigma T^{1/2}) \) vs. \( 1/T \) should be a straight line. Besides, the presence of other scattering mechanisms leads to a straight line of the graph of \( \ln(\sigma T^{3/2}) \) vs. \( 1/T \). All these graphs are plotted for the sample under investigation and shown in figures 3.34 and 3.35 respectively.

As a summary, to reach a final conclusion about the influence of any scattering mechanism on overall conduction behaviour in CdTe investigated here, all the above discussed variations have been plotted in the same figure as shown in figure 3.36. From the careful observation of figure 3.36, it can be said that the graph of \( \ln(\sigma T^{-1/2}) \) vs. \( 1/T \) corresponding to the 1-D behaviour looks to be a better approximation towards a
Figure 3.37(a) I - V plot of W (497Å) contacts on CdTe sample 1

Figure 3.37(b) I - V plot of W (497Å) contacts on CdTe sample 2
linear nature, which is an indication of the fact that at high temperatures, the one
dimensional behaviour is dominant leading to the independent behaviour of mobility with
temperature.

3.3 Ohmicity with Tungsten
The metal contact to the semiconducting samples has to be ohmic in nature. It is a fact
that all metals do not result in ohmic contact with semiconductors but may result in
metal-semiconductor Schottky barriers /18-22/. In present investigations, the ohmicity of
the metal contact of tungsten on the CdTe sample has been studied. The tungsten films
have been deposited using electron beam gun through a circular metal mask on CdTe
crystals on regions where contacts can be taken. The deposition of tungsten on CdTe was
carried out using HINDHIVAC Vacuum Coating Unit (Model BC-300) at a pressure of
10^-6 Torr. The thickness of the deposited tungsten film spots was 497Å. The back
contacts were taken with stainless steel leads using silver paste on the deposited tungsten
film spots. Constant currents of several decade range have been passed and voltage drop
across two such contacts were measured.

3.3-1 Result
The figure 3.37(a) and (b) show the variation of the current with respect to the voltage
drop across contacts. The good linearity for current over a wide current range clearly
indicates that the contact between tungsten and CdTe is ohmic.

3.4 References
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