APPENDIX I

THE ANALOG TO DIGITAL INTERFACE BOARD FOR THE TANDY MARK IV COMPUTER

This interface comprises of

a) A multi-channel analog to digital conversion circuit,

b) A Digital to Analog Output

c) The control and latch circuitry for the interface.

A twelve bit Intersil 7109 converter has been used in this board. Of the available devices this chip provides the greatest precision at low cost but is also the slowest in operation. The maximum sampling rate of this device is about 1/30\textsuperscript{th} of a second per channel. However this suffices for many purposes and the slow speed means that computer programs for acquiring the data can be written in a high level language. The diagram of the board's circuits shown in the figure.

The 7109 chip is a forty pin type and has a twelve bit digital output. But these are not directly interfaced to the eight bit data bus of the mark four computer. Hence two chip select pins (pins 18 & 19) are provided. The low order eight bits are selected by one pin (pin 18) and the remaining four bits along with a polarity and over range flags are selected by the other pin as a high byte. The seventh and eighth bits of this byte have no significance.

This is an integrating type of converter and its clock is configured by an R-C circuit connected to pin numbers 22, 23 & 25. Auto zero is provided by the R-C network connected to pins 30, 31 & 32. A reference voltage is available from the chip at pin no 29, and this is connected through a potentiometer to the + 5 volt supply, so that a variable reference voltage can be applied to the chip at the reference input pin (pin 36). This enables the full scale range to be adjusted. The nominal range of the full scale sensitivity is ±200 millivolts. This chip can take care of negative as well as positive swings in the voltage being sampled.
The input voltage signal is given at pin 35. The supply voltages for the chip are +5 and -5 volts. The RD strobe goes to pin 20 to read data. The BUSY flag can be checked while reading at pin no.2.

To take a reading a data request must be sent to pin 26. The busy signal at pin 2 is scanned till it goes low, then the high and low order bytes are read from the data pins of the 7109. In this board the various output pins (totally fourteen in number) are connected in such a way that 8 bits can be read at a time. The pins 9 to 16 provide the low order byte and the pins 3 to 8 provide the six bits of the high order byte. Both sets of pins are interlinked since there are tri-state buffers inside the chip to disable one set of bits while the other is being read.

An eight channel CMOS analog multiplexer is used to select one analog signal at a time from the eight provided in the interface. The multiplexer used is the CD4051. It requires the plus and minus voltages and can handle signals that alter between 5 volts and -5 volts. The channel selection is done by software inputs to pins A, B & C. The selected channel is available at pin 3. The analog inputs are given to the pins 2, 4, 5, 12, 13, 14, 15 & 16.

In order to select the analog input channel a separate four bit output port is provided on the board. This is a four bit latch which uses a 74LS75 latch chip. Three bits of the latch are used to select the channel. The fourth bit is used to generate the data request signal that starts the converter working.

Eight amplifiers each using an IC 741 chip are also provided on the board to provide a constant impedance to the CD4051 chip on all the channels and also to provide the range adjustment (offset and gain) for the individual channels. The offset adjustment comprises of 10 Kilo Ohm multiturn presets, one for each amplifier. The Gain adjustments are also 10K presets. The gain is set to give four pairs of channels, with maximum of 1, 2, 5 & 10 volts.

The 74LS138 latch has eight chip select outputs. Of these five are used as follows:

1. Chip Select 1: This reads the high order byte from the 7109
2. Chip select 2: This reads the low order byte from the 7109
3. Chip Select 3: This goes to the 74LS74 to select the analog channel and start data conversion.
4. Chip Select 4: This latches the digital to analog converter

5. Chip Select 5: This selects the input port that reads the BUSY bit (pin 2) on the 7109 chip using a 74LS126 chip.

The other lines are not used. The input to the 74LS138 consists of the three low order address lines from the computer's Bus. (the Tandy mark IV is a S100 bus system and the Bus lines are available at an edge connector at the bottom of the machine.) These give eight consecutive addresses in the range E000 to E008 which are used to select the decoder.

The PCB layout of this board was laid out using the Smartwork CAD program on an PC. Since this board involved both analog and digital signals the board was made on a larger scale than usual. Hence it was possible to make it a single sided board with a few jumpers on the component side.