Chapter 5

CAPACITANCE MODEL OF OPTICALLY CONTROLLED MESFET

A number of theoretical models for device intrinsic parameters like capacitance, Y–parameters and S–parameters were reported and discussed in section 2.7. Under direct optical control, photovoltaic effect is found to influence the device characteristics like device current, device voltage and internal device parameters. In the previous chapter the current model for the submicron GaAs MESFET device was developed.

This chapter presents the capacitance model of MESFET under illumination in detail by taking into account the Gunn domain effect which dominates the device operation at microwave frequencies. Section 5.1 presents the existing capacitance model of MESFET and their short comings. The improved capacitance model of the device is also developed in section 5.1. Section 5.2 discusses the results and section 5.3 provides the conclusion.

5.1 Theory

Capacitances of any junction device can be divided into two groups i.e. intrinsic and extrinsic capacitances. In case of GaAs MESFET extrinsic capacitances are related to metallurgical source and drain region, while intrinsic capacitances are related to device junction capacitances [31, 52]. Intrinsic device capacitances play an important role in process monitoring and sensitivity analysis.

The capacitance model of the MESFET shown in fig. 2.2 is an improved model suggested by Michael Shur [31, 52] because it considers the Gunn domain effect which was not considered by earlier researchers. The $C_{gs}$ and $C_{gd}$ are the intrinsic capacitances between the gate–source and gate–drain respectively. The external parasitic capacitances $C_{gsp}$, $C_{gd}$ and $C_{dsp}$ are between the gate–source, the gate–drain, and the drain–source terminals respectively. The other components seen in the fig. 2.2 are $R_{sh}$ which is the drain–source shunt resistance, $R_g$ and $R_d$ are the series gate and drain resistances respectively, $I_{ch}$ is the drain–source channel current, $I_{gs}$ is the gate–source current and $I_{gd}$ is the gate–drain current.

In this chapter an attempt is made to investigate the effect of illumination on the C–V characteristics of GaAs MESFET and a model is developed that is suitable for computer
aided design of GaAs MESFET. The model explains the variation of $C_{gd}$ and $C_{gs}$ with $V_{gs}$, $V_{gd}$ and illumination. It is developed for non-uniformly doped MESFET having channel with Gaussian profile (i.e. an ion–implanted channel). The calculation of intrinsic device capacitance is based on charge distribution in channel region under DC condition [31, 52].

It has been previously reported [5] that the optical illumination can influence the intrinsic capacitance of the GaAs MESFET. Thus the model developed can be used for simulation of optically controlled MESFET applications such as voltage controlled oscillator, optically controlled amplifiers, optical transducers, optical mixer etc. The next section gives details of the proposed capacitance model.

5.1.1 Capacitance Modeling

The structure under consideration is a conventional GaAs MESFET with an opaque gate. The schematic structure of the MESFET under consideration is as shown in fig. 1.1(a). The structure has a channel length of 0.25µm and active region thickness of 0.15µm with an opaque gate. The opaque metallic gate is made of gold. The metal gate and the n–type channel region form a Schottky barrier. The Schottky barrier depletion region under the gate extends into the active region. It controls the cross section of the channel under the gate and hence modulates the channel conductivity and the drain to source current.

Some of the models reported in the recent decades [5, 36] were found to have semi–transparent gate. Such gates increase the light absorbing area and give better optical sensitivity. The depletion layer exists only below the gate region with almost negligible spreading on either side of the gate. However, the semi–transparent gate is very difficult to fabricate as the thickness of the metallic layer is less than 100Å [26, 46–47, 68–70]. This problem can be overcome by replacing semi–transparent gate with opaque gate and allowing the spreading of depletion region on either side of the gate. This configuration will have improved absorption in the extended depletion region on either side of the gate which will cause changes in the intrinsic parameters (device capacitances).

From fig. 1.1(a) it can be seen that the depletion region extends beyond the gate region on the source side and on the drain side. For the ease of analysis depletion region is divided into three parts. Part–I constitutes the major portion which is the depletion region lying below the gate region, part–II is the quarter circle of the depletion region extending beyond gate on the source side and part–III is the quarter circle of the depletion region extending beyond gate on the drain side. Under the gate the depletion region is changing linearly with a maximum width of $Y_{dD} (r_2)$ at the drain end and minimum width of $Y_{dS} (r_1)$ at the source end.
To study the optical effects the optical radiation is assumed to be incident in the vertical $y$–direction while the drain–source current flows in horizontal $x$–direction as shown in fig. 1.1(a).

Figure 5.1(a): Charge distribution for MESFET in linear region [Ref.31 & Ref.52]

Figure 5.1(b): Charge distribution for MESFET in saturation region

[Ref.31 & Ref.52]
The gate being opaque, the excess carriers due to incident optical radiation will be generated in the extended gate depletion region in the inter–electrode spaces (side walls) and the neutral region of the channel. The photo–voltage developed at the gate greatly modulates the channel thickness resulting in the variation of the capacitances related to the inter–electrode spaces [5, 38]. However, the carriers generated in the channel region produce insignificant effect and therefore, can be neglected.

The capacitance model of MESFET shown in fig. 2.2 shows the important intrinsic capacitances namely: gate–to–drain and gate–to–source capacitances ($C_{gd}$ and $C_{gs}$).

The capacitance model of MESFET is developed in the subsequent sections. The equations describing C–V characteristics in linear, saturation, and pinch–off regions of the I–V characteristic are developed. The region of operation is decided according to following conditions:

1. If ($V_{gs} > V_T$) and ($V_{gs} - V_{ds} > V_T$), then the device is in linear region.
2. If ($V_{gs} > V_T$) and ($V_{gs} - V_{ds} \leq V_T$), then the device is in saturation region.
3. If ($V_{gs} < V_T$), then the device is in pinch–off region.

Here $V_T$ is the threshold voltage and is calculated as ($V_{bi} - V_{po}$) the difference of built–in potential ($V_{bi}$) at the Schottky barrier and pinch–off ($V_{po}$) voltage. Calculation of the intrinsic device capacitances is based on the simplified charge distribution shown in fig. 5.1(a) and fig. 5.1(b).

5.1.2 C–V Characteristics in Linear Region

In the ‘on’ condition when ($V_{gs} - V_{ds} > V_T$) the device is said to be in linear region. In the linear region, the gradual channel approximation can be applied to the entire channel to determine the position of the depletion–layer edge under the metallurgical gate. In order to obtain analytical expressions for the intrinsic gate–source capacitance $C_{gs}$ and the intrinsic gate–drain capacitance $C_{gd}$, the depletion–layer edge under the gate (region–1) is assumed to vary linearly (fig. 5.1(a)) along the length of the channel [31, 52]. The total charge under the depletion region is the sum of the charge in the linear region under the gate and the charge in the quarter arcs at the source and drain end [38].

Since the depletion–edge boundary varies linearly with distance the space charge within depletion region ($Q_i$) is given as [31, 52]:

$$Q_i = \int_{b}^{a} N_s(y)dy + \int_{Y_{ad}}^{Y_{ds}} N_d(y)(Y_{ad} - y)dy$$

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The total charge considering the quarter arc at the source and drain end is given by the following expression:

\[ Q_t = Q_0 + \int_0^{y_d} N_d(y)\sqrt{(Y_{ds}^2 - y^2)}\,dy + \int_0^{y_d} N_d(y)\sqrt{(Y_{dd}^2 - y^2)}\,dy \quad (5.2) \]

where, \( N_d(y) \) is the doping density (Gaussian profile) of the channel given by eq. (3.3b), \( Y_{ds} \) is the depletion-layer width at the source end with respect to the gate surface, \( Y_{dd} \) is the depletion-layer width at the drain end with respect to the gate surface.

\( Y_{ds} \) and \( Y_{dd} \) can be calculated by solving Poisson’s equation for the gate–channel–substrate (buffer) structure as in [31, 52].

\[ Y_{dp,s} = R_p + \sigma \sqrt{2}\left[-\ln \left(\frac{Z}{\pi R_p^2}\right)\right]^{1/2} \quad (5.3) \]

where,

\[ Z = \frac{A_1}{A_2} \left(\sqrt{1 + \frac{l - A_2^2}{A_1^2}} - 1\right) \quad (5.4) \]

where, \( A_1, A_2, A_3 \) can be calculated as:

\[ A_1 = \frac{2A_2 + l}{2A_3} \quad (5.5a) \]

\[ A_2 = \psi_{sd} - A_3 \exp \left[-\left(\frac{R_p}{\sigma \sqrt{2}}\right)^2\right] - \text{erf} \left(\frac{R_p}{\sigma \sqrt{2}}\right) \quad (5.5b) \]

\[ A_3 = \frac{2}{\sqrt{\pi}} \frac{\sigma}{R_p} \quad (5.5c) \]

The absolute value of the potential at the depletion layer edge of the Schottky contact at the source and drain end, \( V_{ms,d} \), can be evaluated as in [31, 52].

\[ \frac{V_{ms,d}}{V_{poc}} = \frac{r_{j1} + B_j - B_2}{r_{j1}^2} + \frac{B_j V_{bs} - V_{gs,d}}{V_{poc}} \quad (5.6) \]

where,

\[ B_j = V_{bs} - V_{gs,d} / V_{poc} \quad (5.7a) \]

\[ B_2 = \left[r_{j1}^2 - r_{21}^2 r_{21}^2 - 2\right]^{1/2} \quad (5.7b) \]
\[ V_{\text{poc}} = (V_{bi} - V_{tc} - V_{\text{bias}}) \]  \hspace{1cm} (5.7c)

\[ r_{1t} = \frac{V_{\text{poc}}}{V_{\text{bias}}} = \frac{V_{bi} - V_{tc} - V_{\text{bias}}}{V_{\text{bias}}} \]  \hspace{1cm} (5.7d)

\[ r_{2t} = \frac{V_{bi} - V_{gs,d}}{V_{\text{bias}}} \]  \hspace{1cm} (5.7e)

\[ V_{\text{bias}} \] is the built-in voltage of the channel-substrate (buffer layer) junction given by [31, 52]:

\[ V_{\text{bias}} = V_{eqT} \left( \ln \frac{N_{ch}}{n_i} + \ln \frac{N_{\text{sub}}}{n_i} \right) \]  \hspace{1cm} (5.8a)

\[ V_{eqT} = \frac{KT}{q} \]  \hspace{1cm} (5.8b)

\[ V_{tc} = V_{bi} - V_{\text{bias}} - \frac{qN_D A^2}{2}\varepsilon \]  \hspace{1cm} (5.8c)

\[ A = \frac{2eV_{po}}{Q_a} \]  \hspace{1cm} (5.8d)

where, \( N_{ch} \) is the channel doping density (\( N_{ch} = N_{\text{sub}} \) for non-uniform channel doping),

\( A \) is the effective active layer thickness,

\( N_{\text{sub}} \) is the effective doping density of the substrate.

Now, the capacitance at the source (\( C_{gs} \)) and drain (\( C_{gd} \)) end can be calculated as the rate of change of space charge in depletion region with change in \( V_{gs} \) and \( V_{ds} \) respectively [31, 52].

\[ C_{gs} = -\frac{\partial Q_x}{\partial V_{gs}} = \frac{\partial Q_x}{\partial V_{gs}} + \frac{\pi}{2} \varepsilon Z \]  \hspace{1cm} (5.9)

\[ C_{gd} = -\frac{\partial Q_x}{\partial V_{ds}} = \frac{\partial Q_x}{\partial V_{ds}} + \frac{\pi}{2} \varepsilon Z \]  \hspace{1cm} (5.10)

### 5.1.3 C–V Characteristics in Saturation Region

In the ‘on’ condition the device is in saturation region when \( (V_{gs} - V_{ds}) \leq V_T \). In the saturation region the gradual channel approximation can only be applied to part of the channel (region 1 in fig. 5.1(b)). The space charge within region 1 \( Q_1 \) can be calculated
from eq. (5.1) by substituting $L_1$ for $L_g$, where $L_1$ is the length of region–1 in fig. 5.1(b) [31, 52].

$$Q_i = qZL_1 \int_{y_a}^{y_g} N_d(y)dy + \frac{qZL_1}{Y_{ds} - Y_{db}} \int_{y_a}^{y_g} N_d(y)(Y_{db} - y)dy$$

(5.11)

The total charge considering the quarter arc at the source and drain end in the saturation region is given by eq. (5.2).

For the second region of length $L_2$ ($L_2 = L_g - L_1$) the value of the capacitance depends on the presence or absence of Gunn domain (high field region). Gunn domain formation takes place in III–V compounds when the electric field in the material reaches a threshold level ($F_{th}$). After the formation of Gunn domain the mobility of electrons decreases as the electric field increases. Therefore, the drift velocity also decreases which results in charge accumulation effects at the drain side. The Gunn domain formation takes place in devices with high pinch–off voltage. The conditions for Gunn domain formation are given by [31, 52]:

$$A > A_{dm} \quad \text{No Gunn domain}$$

$$A_{dm} < A < 2A_{dm} \quad \text{Stationary Gunn domain}$$

$$2A_{dm} < A \quad \text{Propagating Gunn domain}$$

$$A_{dm} = \left[ \frac{2\varepsilon(V_{G} - V_{GS} + F_{th}L_1)}{qN_{ed}} \right]^{1/2}$$

(5.12a)

$$N_{ed} = \frac{Q}{A}$$

(5.12b)

$$Q_d = \frac{Q}{2} \left( \left[ a_2 - \text{erf}(z_p) \right] + \frac{V_p}{V_2} \right)^{1/2} - \left[ a_2 - \text{erf}(z_p) \right]$$

(5.12c)

$$V_2 = \frac{qQ\sigma}{\varepsilon \sqrt{2\pi}}$$

(5.12d)

$$\alpha_2 = \frac{R_p}{2\sigma \sqrt{2}}$$

(5.12e)

$$z_p = \frac{R_p}{\sigma \sqrt{2}}$$

(5.12f)
where, $F_{th}$ is the threshold field for bulk negative differential mobility, $N_{ed}$ is the effective uniform doping density.

High field domain does not form in low pinch–off voltage devices with $V_{po} \leq 2V$. Typically pinch–off voltages of GaAs FETs are not high enough for the formation of propagating high field domains and therefore, devices in propagating domain are not considered. Consider the device under no Gunn domain and stationary Gunn domain.

**A. No Gunn Domain:** In this case the length of the carrier velocity saturation region $L_2$ is only a small fraction of the length of the entire channel. Therefore, the shape of the depletion region edge is insensitive to the source voltage when the drain and gate voltages are held fixed and no domain capacitance exists.

**B. Stationary Gunn Domain:** If a stationary Gunn domain forms in the channel at the drain side of the gate the equations of $C_{gs}$ and $C_{gd}$ for no Gunn domain can be used because the length of the Gunn domain is equally sensitive to the drain voltage and the source voltage. The additional domain capacitance ($C_{dom}$) is given by [31, 52]:

$$C_{dom} = \frac{Q_+}{2V_{2s}} \tag{5.13a}$$

$$V_{2s} = V_{ds} - V_s \tag{5.13b}$$

$$Q_+ = 0.728 \left[ qe \sqrt{n_{cr} N_{ch} V_{2s}} \right]^{1/2} \tag{5.13c}$$

where, $n_{cr}$ is the characteristic doping density (typical value for GaAs is $3 \times 10^{15} \text{cm}^{-3}$).

The voltage across region–1 ($V_{1s}$) for the non–uniform channel profile can be approximated by the following relation [31, 52]:

$$V_{1s} \approx \frac{(V_{gs} - V_T) F_{th} L_y}{F_{th} L_y + V_{gs} - V_T} \tag{5.13d}$$

If the small variation of the conducting channel opening in the carrier–velocity saturation region (region–2 in fig. 5.1(b)) could be neglected, then the space charge within region–2 can be approximated by [31, 52]:

$$Q_2 = qZL_2 \int_{\theta}^{\gamma_{sa}} N_d(y) dy \tag{5.14}$$

where, $L_2$ is the length of region–2.
From the definition the gate–source capacitance and gate–drain capacitance can be represented as \([31, 52]\):

\[
C_{gs} = -\frac{\partial Q_j}{\partial V_{gs}} - \frac{\partial Q_j}{\partial V_{gs}} + \frac{\pi \varepsilon Z}{2} \tag{5.15}
\]

\[
C_{gd} = \frac{\partial Q_j}{\partial V_{ds}} + \frac{\partial Q_j}{\partial V_{ds}} + C_{sw} \tag{5.16}
\]

where,

\[
C_{sw} = \varepsilon Z \sin^{-1}\left(\frac{V_{bi} - V_{gs} + V_{ds}}{V_{bi} - V_{gs}}\right)^{1/2} \tag{5.17}
\]

The third term on the right–hand side of eq. (5.16) is an approximate value for the sidewall capacitance. The charge derivatives \(\frac{\partial Q_j}{\partial V}\) depend on the presence or absence of a stationary high field domain which may form at the drain side of the gate.

### 5.1.4 C–V Characteristics in Pinch–off Region

When \((V_{gs} < V_T)\) the device is in pinch–off region. If a gate–source bias less than the threshold voltage \(V_T\) is applied then the conducting channel is totally depleted. Therefore, the contribution to the device capacitances is due to the variation of the space charges in the sidewalls and is given by \([31, 52]\):

\[
C_{gs} = \varepsilon Z \sin^{-1}\left(\frac{V_{bi} - V_{gs} + V_{ds}}{V_{bi} - V_{gs}}\right)^{1/2} \tag{5.18}
\]

\[
C_{gd} = \varepsilon Z \sin^{-1}\left(\frac{V_{bi} - V_{gs} + V_{gs}}{V_{bi} - V_{gs}}\right)^{1/2} \tag{5.19}
\]

### 5.1.5 Effect of Illumination on Intrinsic Capacitances

The effect of illumination on intrinsic parameters can be modeled by replacing \(V_{gs}\) by \(V_{gs}^{eff}\) in all the above model equations.

where,

\[
V_{gs}^{eff} = V_{gs} + V_{op} \tag{5.20}
\]

\(V_{op}\) is calculated as in eq. (3.16a). Here \(\phi\) is given by \([5]\):
\[ \phi = \frac{(1-R_s)(1-R_t)P_o}{hvL/Z} \]  (5.21)

where, \( P_o \) is the input optical power (in Watts) under illuminated condition.

5.2 Results and Discussions

Simulations to calculate gate capacitances \( (C_{gd} \) and \( C_{gs} \)) under dark and under illuminated condition (incident optical power \( (P_o) \)) are carried out in MATLAB using the model equations developed above and the parameter values given in table 3.1.

Fig. 5.2(a) shows the variation of \( C_{gd} \) with \( V_{ds} \) for varying \( V_{gs} \) at fixed illumination \( (P_o=0.25W) \). It is observed from the result that \( C_{gd} \) decreases with increase in \( V_{ds} \). As \( V_{ds} \) increases the drain side depletion region increases and therefore, capacitance decreases with increase in \( V_{ds} \).

Fig. 5.2(b) shows the variation of \( C_{gd} \) with \( V_{gs} \) for varying \( V_{ds} \) at fixed illumination. The result shows that as \( V_{gs} \) increases the drain gate capacitance \( (C_{gd}) \) increases. As \( V_{gs} \) increases, the drain side depletion region decreases and hence capacitance \( (C_{gd}) \) increases with increase in \( V_{gs} \).

![Figure 5.2(a): Capacitance vs. voltage \( (C_{gd-V_{ds}}) \) for different \( V_{gs} \) and fixed illumination \( P_o=0.25W \)]
Figure 5.2(b): Capacitance vs. voltage ($C_{gd}$–$V_{gs}$) for different $V_{ds}$ and fixed illumination $P_{oi}=0.25W$

Figure 5.3(a): Capacitance vs. voltage ($C_{gs}$–$V_{gs}$) for different $V_{ds}$ and fixed illumination $P_{oi}=0.25W$
Figure 5.3(b): Capacitance vs. voltage ($C_{gs}$-$V_{ds}$) for different $V_{gs}$ and fixed illumination $P_{oi}=0.25W$

Figure 5.4: Capacitance vs. voltage ($C_{gd}$-$V_{ds}$) for varying illuminations
Figure 5.5: Capacitance vs. voltage ($C_{gs}$–$V_{gs}$) for varying illuminations

Figure 5.6: Capacitance vs. voltage ($C_{gs}$–$V_{gs}$) curve for various frequencies and illuminations ($LIf_r$–($Poi$=0W and $10^{12}$Hz), $LIf_r$–($Poi$=0W and $10^{10}$Hz), $LIf_r$–($Poi$=0W and $10^{7}$Hz) $HIf_r$–($Poi$=25mW and $10^{12}$Hz), $HIf_r$–($Poi$=25mW and $10^{10}$Hz), $HIf_r$–($Poi$=25mW and $10^{7}$Hz))
Fig. 5.3(a) shows the variation of $C_{gs}$ with $V_{gs}$ for varying $V_{ds}$ at fixed illumination. The results show that $C_{gs}$ increases as $V_{gs}$ becomes more and more positive. As $V_{gs}$ becomes more positive the source side depletion region decreases and hence capacitance $C_{gs}$ increases with increase in $V_{gs}$.

Fig. 5.3(b) shows the variation of $C_{gs}$ with $V_{gs}$ for varying $V_{ds}$ at fixed illumination. It is observed from the result that $C_{gs}$ increases with increase in $V_{ds}$. As $V_{ds}$ increases the drain depletion region increases and starts to spread towards the source side. This will result in increase of the depletion region at the source end and will reduce equivalent source voltage. Hence, the net charge in depletion region under the source increases and the net voltage at the source reduces resulting in increase in $C_{gs}$ capacitance with increase in $V_{gs}$.

Fig. 5.4 shows the variation of $C_{gd}$ with $V_{ds}$ for varying illumination. It shows that the capacitance $C_{gd}$ increases as optical power of incident illumination on the gate increases. The illumination develops a photo–voltage at the gate which increases with the increase in optical power. As the gate potential increases the gate depletion region reduces and hence capacitance $C_{gd}$ increases with increase in illumination.

Fig. 5.5 shows the variation of $C_{gs}$ with $V_{gs}$ for varying illumination. It shows that as illumination at the gate increases the capacitance $C_{gs}$ increases. The illumination develops a photo–voltage at the gate which increases with the increase in illumination. As the gate potential increases the gate depletion region reduces and hence capacitance $C_{gs}$ increases with increase in illumination.

Fig. 5.6 shows the variation of $C_{gs}$ with $V_{gs}$ at different frequencies and illuminations. It shows that as illumination at the gate increases the capacitance $C_{gs}$ increases at a fixed frequency. It also shows that as frequency of the input signal increases the capacitance $C_{gs}$ decreases at a particular illumination and the capacitance plot shifts down for higher frequencies. As the frequency increases the optical potential developed at the gate decreases. Due to the decrease in gate potential, the gate depletion region increases and hence capacitance $C_{gs}$ decreases with increase in illumination.

5.3 Conclusion

A capacitance model of an optically controlled GaAs MESFET presented here can estimate the effect of illumination on the two non–linear gate capacitances of MESFET device. The modeling technique is based on charge distribution model in channel region. The model has been tested for a range of input optical power and frequencies. The obtained results for the model proposed give a more accurate description of the gate
capacitance under dark and illumination. The model considers the charges in the extended depletion region in the inter–electrode spaces of gate–source and gate–drain, which was not considered by earlier works for intrinsic capacitance calculation and is the highlight of this work. The study reveals that the device capacitances can be controlled by the incident optical power and frequency of operation. Both the capacitances increase with the increase in illumination and decrease with the increase in frequency. The device can be used for a variety of optoelectronic applications.