Chapter 3

Congestion Control in Communication Networks using Discrete Time Sliding Mode Control

3.1 Introduction

This chapter includes detailed description of congestion control mechanism using discrete time sliding mode control. Initial phase of this chapter focuses on requirement of congestion control mechanisms then subsequent chapter shows a mathematical background of multirate output feedback based sliding mode control, mathematical model of the proposed algorithm; mathematical description of the algorithm, simulation results, FPGA based simulation results and conclusion.

3.2 Congestion

All wireless communications systems are full of uncertainty that is why in all networks there are situations where the number of users or external load is higher
than the capacity of the channel. Therefore, network may not serve all users simultaneously and "congestion" occurs. To understand this concept in detail refers Fig. 3.1.

Figure 3.1: Network Structure to Explain Concept of Congestion in the Network

It shows the network, which contains ten nodes numbered N₁ - N₁₀. Where N₁, N₂, N₃, and N₄ are sending packets to N₇, N₈, N₉, N₁₀ respectively through N₅ and N₆. Maximum data rate supported by each link in the network is \( B \). Now if N₁, N₂, N₃, and N₄ are sending packets at maximum data rate \( B \), then the incoming data rate at node N₅ is \( 4 \times B \). Here node N₅ can handle only one node's data at a time, So all packets received at node N₅ cannot be forwarded immediately, Some packets need to be stored in buffer (memory) at node N₅ where they wait to be forwarded towards nodes N₇, N₈, N₉ and N₁₀. If the buffer size of the N₅ is not enough then buffer cannot store all packets coming from various nodes and congestion occurs. Due to congestion, some packet will be lost or corrupted during transmission. In short, if the input data rate is greater than the available link capacity then congestion occurs.

Assume that maximum buffer capacity is to handle at a time k-bits. If because of reduced input data rate buffer is getting less than k-bits then system is in
underutilization and if because of higher input data rate more than k-bits are coming to the buffer than the system is under congestion. In both case system throughput is getting lower and system cannot work efficiently. To overcome this, the optimum value of the input data rate has to be found out so that buffer can be used efficiently and more throughputs can achieve with good QoS.

3.3 Multirate Output Feedback and Discrete Sliding Mode Control

Discrete sliding mode control has been investigated since last three decades and has reached to point wherein a well-established theory as well as implementation has been reported in the literature. Advances in computer communication network with wired and wireless configurations have imposed a challenging problem for control community. Such system should be fast and for which fast acting controller needs to be designed. At the same time, such system uses inherent switching of data packets and routes. Hence, it has been found interesting to use inherent switching like control, a sliding mode control for such networks. The chapter explores the utilization of discrete sliding mode control approach for the congestion control in the communication network. For the past several years, many feedback control methods have been used for the control of various parameters of communication networks like traffic control, congestion control and power control. The work presented here proposes a new application of sliding mode control for congestion control in the communication network. As computer communication networks are inherently discrete in nature, the discrete sliding mode control has been applied to discrete time system.

3.3.1 Multirate Output Feedback

In general all control systems contain feedback but multirate output feedback is somewhat different from them. As the name suggests Multirate output feedback is a feedback control scheme, which sample the control input of the system at
multiple sampling rates. Multirate output feedback based control systems are more stable compared to static feedback control systems. The Multirate output feedback, the control input or sensor output is sampled at a faster rate than other [45-47]. Consider the discrete system

\[
\begin{align*}
x(k+1) &= \phi x(k) + \Gamma u(k) \\
y(k) &= C x(k)
\end{align*}
\]  

(3.1)

Where \( \tau \) is the sampling period, \( x \) is N-dimensional state vector which is to be controlled, \( u \) is a scalar input, \( y \) is the output vector. \( \phi, \Gamma, C \) is the input state matrix, controller input matrix and the output gain matrix respectively. For the further discussion, we assume that system is controllable and observable. Now assume the system represented in Eqn. 3.1 is sampled at the rate \( 1/\Delta \) where \( \Delta = \tau / N \). \( N \) is chosen to be greater than or equal to \( \nu \) where \( \nu \) be observability index (\( \phi, C \)). Output measurements are taken at time instants \( t = l\Delta \), where \( l = 0, 1, ..., N - 1 \). The control signal \( u(t) \) is applied during the interval \( k\tau \leq t \leq (k+1)\tau \). For the discrete time system having time \( t = k\tau \), the fast output samples [16]

\[
y_k = \begin{bmatrix}
y(k\tau - \tau) \\
y(k\tau - \tau + \Delta) \\
\vdots \\
y(k\tau - \Delta)
\end{bmatrix}
\]  

(3.2)

Now the multirate output sampled system can be represented as equation 3.3

\[
\begin{align*}
x(k+1) &= \phi x(k) + \Gamma u(k) \\
y_{k+1} &= C x(k) + D u(k)
\end{align*}
\]  

(3.3)

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3.3.2 Discrete Time Sliding Mode Control

Now a days every analog electronic system is converging into the digital systems. In general, control systems must be a continuous control system but because of the invention of high speed digital processors and availability of other electronic components continuous time control systems may also convert into the discrete time control systems. In discrete sliding mode control observation, analysis and control operations are performed at regular interval of time, which is nothing but a sampling time of the discrete time sliding mode control. Eqn. 2.1 shows the continuous time system in normal form where \( t \) is the time value while Eqn. 3.3 represents discrete time systems where \( k \) is the index of sampling time. Fundamentally, in discrete time sliding mode control systems, control signal is computed at a particular sampling instant. Discrete variable structure control may follow quasi-sliding mode motion. During such motion, the state of the system can approach the switching surface but cannot generally stay on it [48]. Fig. 3.2 represents the generalized working of multirate output feedback based discrete time sliding mode control.

3.3.3 Design of Switching Surface

According to the DVSC theory, all control laws must satisfy switching plane equation

\[
s(k) = c^T x(k) = 0
\]
Figure 3.2: Generalized Block Diagram of Multirate Output Feedback Based Discrete Time Sliding Mode Controller

For the design of switching hyper plane, the system given in Eqn. 3.1 is transformed into suitable form by appropriate transformation [49] as

$$\dot{x}(k) = Mx(k)$$

(3.6)

The transformed system takes the form

$$\dot{x}(k + 1) = \overline{\Phi} \dot{x}(k) + \overline{\Gamma} u(k)$$

(3.7)

Where;

$$\overline{\Phi} = \begin{bmatrix} \Phi_{11} & \Phi_{12} \\ \Phi_{21} & \Phi_{22} \end{bmatrix}$$

$$\overline{\Gamma}^T = \begin{bmatrix} 0 & \Gamma_2 \end{bmatrix}$$

The switching planes are described as shown in Eqn. 3.8

$$s(k) = c^T \overline{M}^{-1} \dot{x}(k) = 0$$

$$s(k) = (c^T) \begin{bmatrix} \dot{x}_1(k) \\ \dot{x}_2(k) \end{bmatrix}^T = 0$$

(3.8)

From Eqn. 3.7 and 3.8 we have
\[
\dot{x}(k+1) = \Phi_{11}\dot{x}_1(k) + \Phi_{12}\dot{x}_2(k)
\]
\[
\dot{x}_2(k) = -\varepsilon^T \dot{x}_1(k)
\]

3.3.4 Reaching law based Discrete Time Quasi Sliding Mode Control Law

The reaching law is a differential equation, which specifies the switching functions. The reaching law for the continuous time VSC is

\[
\dot{s}(t) = -\varepsilon \text{sgn}(s(t)) - qs(t)
\]

(3.10)

Where \( \varepsilon \) and \( q \) are the positive gain.

Now discrete time quasi-sliding mode control is based on state feedback, which uses reaching law approach. A reaching law for the sliding control of a discrete time system has the following form [50].

\[
s(k+1) - s(k) = -\eta s(k) - \varepsilon \eta \text{sgn}(s(k))
\]

(3.11)

Where \( \eta > 0 \), is the sampling period \( \varepsilon > 0, q > 0, 1 - \eta > 0 \)

A reaching law for the sliding mode control of discrete time system has the following form

\[
s(k+1) - s(k) = -\eta s(k) - \varepsilon \eta \text{sgn}(s(k))
\]

(3.12)

A desirable reaching mode response can be obtained by appropriate choice of parameters \( q \) and \( \varepsilon \). The presence of signum term indicates switching across sliding surface. The trajectory will stay in the specified band known as a quasi-sliding mode band (QSMB). Switching function \( s(k) \) is defined as

\[
s(k) = c^T x(k) = 0
\]

(3.13)
Using the reaching law in Eqn. 3.12, the control law for the system represented in Eqn. 3.1 may represent [16] as

\[ u(k) = Fx(k) + \gamma \text{sgn}(s(k)) \quad (3.14) \]

Where

\[ F = -(c^T \Gamma_r)^{-1}[c^T \Phi_r - c^T I + q \tau c^T] \]
\[ \gamma = -(c^T \Gamma_r)^{-1} \epsilon \tau \]

### 3.3.5 Sliding Surface and Control Law Computation Using Multirate Output Feedback Based Discrete Sliding Mode Control.

This scheme is a combination of Multirate output feedback and discrete sliding mode control. Sometimes states of the system is not measurable, this method is helpful. The algorithm uses past control input and output samples for computation of sliding surface and sliding mode control.

Generalize equation for switching surface and control may be represented [16] as

\[ s(k) = c^T \Phi_r C_0^{-1} y_k + c^T [\Gamma_r - \Phi_r C_0^{-1} D_0] u(k-1) \quad (3.15) \]
\[ u(k) = F \Phi_r C_0^{-1} y_k + F[\Gamma_r - \Phi_r C_0^{-1} D_0] u(k-1) + \gamma \text{sgn}(s(k)) \]

### 3.4 Congestion Control in Communication Networks

All commercially available communication networks are under the category of ATM (Asynchronous Transmission Mode) networks. Because of non-synchronization between transmitters and receivers. Designing and applying any control algorithm is very difficult for ATM Networks. Now a days ATM is a...
major technique used in the non-homogeneous network to provide broadband services. ATM services are broadly classified in two categories 1. Guaranteed service 2. Best effort service. The best effort service is further divided in two categories, unspecified bit rate (UBR) and absolute bit rate (ABR). UBR does not guarantee bandwidth and delay or loss in the network. ABR provides guaranteed bandwidth, delay or loss.

**Figure 3.3: Classification of ATM Network Services**

Congestion is defined as a condition of a wireless network, where the network does not meet a predefined QoS. As mentioned in the introduction part of chapter 1, there are two ways to reduce congestion in the network as shown in Fig. 3.4.

1. Reduce source flow rate
2. Increase buffer size

**Figure 3.4: Classification of Congestion Control Schemes**

Reduce input data rate

Increase buffer size
For ATM networks, where $n$-number of nodes are connected in parallel, congestion occurs when

$$\sum \text{Input rate} > \text{Channel Capacity}$$

Most of the congestion control mechanism consists of adjusting the input rates to match the available link capacity, so that desired QoS can be obtained. For short-term congestion, an end-to-end feedback control scheme can be used. As shown in Fig. 3.5, Sources are generating data, which are to be transferred to other nodes in the network through a router switch.

**Figure 3.5: Structure of Proposed Congestion Controller**

Router switch is responsible to multiplex the data of all active sources and contain memory to buffer the data if channels are not available. The proposed congestion controller depends on two feedbacks 1. buffer size 2. source data rate. Traditional congestion control algorithms contain either data rate controller or buffer length controller to control congestion. The source flow controller controls the data rate of the sources, so at router switch traffic accumulation and congestion decreases. Buffer length controller changes the size of buffer to
accommodate data coming from various sources with higher data rate. Proposed method contains a combination of source flow controller and buffer length controller. When congestion occurs, the controller increases the size of the buffer and sends a beacon signal towards sources to reduce their data rate.

3.5 Network Model

As shown in the Fig. 3.6, m-number of nodes are connected in the network.

![Communication Network Model]

In Figure 3.7,

$S_1, ..., S_m : m$-number of transmitters in the network (Sources)

$T_f :$ forward time delay
Congestion occurs when number of users want to transmit their data through the same channel. For the past few years, many NN based algorithms become very popular in engineering and technology, because the NN based schemes include the standard structure of function approximation and learning capabilities that can be used readily in many applications. The NN based methods can be broadly categorized based on learning scheme employed.

3.6 State-Space Representation of the System.

Multisource discrete-time nonlinear systems to be controlled may represented in state space form as

\[
x(kT + 1) = \phi(x(kT)) + \Gamma(u(kT) + d(kT))
\]

\[
y(kT) = Cx(kT)
\]

Where

\[
f(x(kT)) = \text{sat}[x(k) - q(T_f - T_b) + I_{mi}^{(k)} - S_r^{(k)}]
\]

Eqn. 3.17 is defined as an actual traffic flow and it is a function of current buffer occupancy \(x(k)\), the traffic arrival rate at destination buffer \(I_{mi}^{(k)}\), bottleneck queue level \(q(T_f - T_b)\) and Service capacity \(S_r^{(k)}\).

- \(T\) is sampling time of the control signal
- system order: \( n = (RTT / T) + 1 \)
- \( x(k) \in \mathbb{R}^n \) is the buffer length at a time instant \( k \), \( \phi_r \) is \( n \times n \) state matrix, \( \Gamma_r \) and \( C_r \) are \( n \times 1 \) vectors.

\[
\phi_r = \begin{bmatrix}
\phi_{11} & \phi_{12} & \cdots & \phi_{1n} \\
\phi_{21} & \phi_{22} & \cdots & \phi_{2n} \\
\vdots & \vdots & \ddots & \vdots \\
\phi_{n1} & \phi_{n2} & \cdots & \phi_{nn}
\end{bmatrix}
\]

\[
\Gamma_r = \begin{bmatrix}
\Gamma_1 \\
\Gamma_2 \\
\vdots \\
\Gamma_n
\end{bmatrix}, \quad C_r = \begin{bmatrix}
C_1 \\
C_2 \\
\vdots \\
C_n
\end{bmatrix}
\]

3.7 Simulation Results:

**Example: 1** Estimation of traffic accumulation in the network and restrict it to 250 (maximum capacity)

According to Eqn. 3.17, for this simulation we have assumed that system is controllable and observable. For the simulation purpose system is considered second order and other parameters \( q \) and \( \varepsilon \) are 5 and 0.05 respectively, sampling time \( \tau = 0.2(\mu s) \), and \( n = 2 \), \( x(1) = I \), \( I_{su}^{(k)} = 10 \), Bottleneck queue level \( q(T_f - T_b) = 8 \) and service capacity \( S_r^{(k)} = 100 \).
**Figure 3.7:** Variation in Buffer length With Time When Maximum Buffer Length Set at 250

**Figure 3.8:** Variation in Buffer Length Independent of Disturbances and Remain Less than 250 for Long Time
Example: 2 Computation of sliding surface and control law

From Eqn. 3.15, sliding surface and control law can be calculated; the simulation has been carried out with following parameters.

\[
A = \begin{bmatrix} 0 & 10 \\ -2 & -3 \end{bmatrix}, \quad B = \begin{bmatrix} 0 \\ 50 \end{bmatrix}, \quad C = [1 \quad 0], \quad \tau = 0.2, \quad N = 2, \quad q = 2, \quad e = 0.1, \quad x = \begin{bmatrix} 1600 \\ 250 \end{bmatrix}
\]

![Figure 3.9: State Responses of the System](image)

![Figure 3.10: Sliding Surface with Respect to Time](image)
3.8 FPGA Based Simulation Results

The FPGA stands for Field Programmable Gate Array; it is an array of configured logical block, which can be programmed using VHDL (high-speed integrated circuit Hardware Description Language). The FPGA can deal with only digital signals and communication networks considered in thesis is a digital communication network. This section shows the simulation results based on an FPGA platform. Simulation divided in two parts

1. buffer length control

2. flow Control
1. Buffer Length Control

**Simulation 1:** When network contains only two nodes and buffer of size 8-bits. Each node has 4-bits data to be transmitted and buffer has a size of 8-bits, so there is no congestion and no data loss. As shown in the Fig. 3.12, \textit{ln1} and \textit{ln2} are two nodes, which carry data "1101" and "0010" respectively. Buffer carries multiplexed data on \textit{node1} and \textit{node2} as "10011010." Here enough buffer size is available, so no congestion and no loss of data.

![Figure 3.12: Simulation Results of VHDL Program When Network Contain Two Nodes and Buffer Size 8-bits (No Congestion)]
Simulation2: When network contains three nodes and buffer of size 8-bits. Each node has 4-bits data to be transmitted and buffer has a size of 8-bits, which is not enough to accommodate all node data, so here congestion occurs and data has been lost from some nodes. As shown in the Fig. 3.13, In1, In2, and In3 are three nodes, which carry data “1101,” “0010” and “0011” respectively. Buffer carries multiplexed data of node1, node2, and node3 as “10101110.” Yellow rounded data could not find space in the buffer and lost.

Figure 3.13: Simulation Results of VHDL Program When Network Contain Three Nodes and Buffer Size 8-bits (Congestion occurs)
Simulation 3: When network contains three nodes and buffer of size 12-bits. Each node has 4-bits data to be transmitted and buffer has a size of 12-bits, so there is no congestion and no data loss. As shown in the Fig. 3.14, In1, In2, and In3 are three nodes, which carry data “1101,” “0010” and “0011” respectively. Buffer carries multiplexed data of node1, node2, and node3 as “101011100100.” Here also enough buffer size is available, so no congestion and no loss of data.

Figure 3.14: Simulation Results of VHDL Program When Network Contain Three Nodes and Buffer Size 12-bits (No Congestion)
2. Flow Control

Simulation: When network contains three nodes and buffer of size 12-bits. Each node has 4-bits data to be transmitted and buffer has a size of 12-bits, so no congestion and no loss of data so far buffer length is concerned.

Figure 3.15: Simulation Results of VHDL Program When Network Contain One Node and Node 1 is Following Clock Rate of divclk1 (No Congestion)

Figure 3.16: Simulation Results of VHDL Program When Network Contain Two Nodes and Nodes are Following Clock Rate of divclk2 (No Congestion)
The important part of this simulation is source data rate is decided by the number of nodes participating in the network. As shown in Fig. 3.15, 16, and 17 value of a (yellow rounded) is showing the number of nodes in the network. If a is “011” that means only one node in the network to transmit its data, so node can follow the fast clock rate which is given by \( \text{divclkl} \) (divided clock). When a is “011” that means two nodes in the network, so nodes can follow comparatively slower data rate \( \text{divclk2} \) and if a is “111” that means total three nodes in the network and little slower data rate \( \text{divclk3} \) can be followed by the nodes. If a node fails in following the particular data rate then congestion occurs and data will be lost.

![End Time: 1000 ns](image)

**Figure 3.17:** Simulation Results of VHDL Program When Network Contain Three Nodes and Nodes are Following Clock rate of \( \text{divclk3} \) (No Congestion)

<table>
<thead>
<tr>
<th>No. of Nodes in the Network</th>
<th>Source data rate (bits/sec)</th>
<th>Buffer length requirement</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>25Mbits/sec</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>12.5Mbits/sec</td>
<td>4-bits</td>
</tr>
<tr>
<td>2</td>
<td>6.255Mbits/sec</td>
<td>8-bits</td>
</tr>
<tr>
<td>3</td>
<td>3.1225 Mbits/sec</td>
<td>12-bits</td>
</tr>
</tbody>
</table>

Table 3.1 Experimental Results
* Data given in Table 3.1 is as per the FPGA board XC3E10 CP-132, as the board's clock frequency change data rate may change.

3.9 Conclusion

To reduce congestion in communication network source flow rate and buffer length is considered as a controlling parameter in this algorithm. According to increment/decrement of number of users in the network, size of the buffer increase/decrease. Equation 3.16 bound the buffer length limit to 250 maximum depends on the size of memory used in the device. Fig. 3.7 and 3.8 shows the size of the buffer required over a time.

Fig. 3.9 to 3.11 shows the simulation result of multi rate output feedback based discrete sliding mode control system. For the sake of simplicity, the system is considered as a second order system. The actual order of the system can be decided by the round trip time (RTT). Control law is somewhat adaptive in nature because it depends on the traffic condition when the number of users increase/decrease or occupancy of the buffer full/empty, control law is changed. The controller proposed here is robust as it less affected by external disturbances.