## CHAPTER-7
FABRICATION, CHARACTERIZATION AND APPLICATION OF CdSe THIN FILM TRANSISTORS

<table>
<thead>
<tr>
<th>Contents</th>
<th>Pages</th>
</tr>
</thead>
<tbody>
<tr>
<td>7.1 Introduction</td>
<td>096</td>
</tr>
<tr>
<td>7.2 Experimental</td>
<td>098</td>
</tr>
<tr>
<td>7.2.1 CdSe-TFT Structure and Fabrication</td>
<td>098</td>
</tr>
<tr>
<td>7.2.2 Measurements</td>
<td>098</td>
</tr>
<tr>
<td>7.3 Results and Discussions</td>
<td>098</td>
</tr>
<tr>
<td>7.3.1 Electrical characterization of TFT</td>
<td>098</td>
</tr>
<tr>
<td>7.3.2 Effect of Annealing on the I-V characteristics of TFTs</td>
<td>103</td>
</tr>
<tr>
<td>7.3.3 Electrical parameters of TFT</td>
<td>108</td>
</tr>
<tr>
<td>7.3.4 Optimization of Surce-Drain gap</td>
<td>108</td>
</tr>
<tr>
<td>7.3.5 Optimization of gate insulator thickness</td>
<td>109</td>
</tr>
<tr>
<td>7.3.6 Use of TFT as a Liquid Crystal Pixel Driver</td>
<td>110</td>
</tr>
<tr>
<td>7.4 Conclusions</td>
<td>113</td>
</tr>
<tr>
<td>References</td>
<td>114</td>
</tr>
</tbody>
</table>
7.1 INTRODUCTION

Integrated circuit development has followed two main approaches: silicon monolithic circuits and thin film circuits. Both techniques have lead to considerable advances in microminiaturization, reliability, and cost reduction.

The silicon integrated circuit is a logical extension of single transistor fabrication. Its rapid development was due to the exploitation of a favorable combination of properties of silicon, on which the epitaxial planner process is based.

One serious problem with silicon circuits is that silicon is far from a perfect insulator. Since all of the active devices and some passive devices are embedded in silicon, parasitic losses and spurious coupling between elements on the same substrate can seriously limit the circuit performance. A number of isolation techniques can be used, but they limit the packing density and increases the fabrication cost.

The deposition techniques for thin film elements such as resistors, capacitors and the interconnection between them are well established. The advantages as compared to silicon technology, can be considerable. For example, all elements are deposited on an insulating substrate, such as glass or ceramic, so excellent electrical isolation between them is achieved without any special techniques. Such isolation has the advantage of avoiding the parasitic capacitance that occurs with the isolation diffusions used in monolithic techniques.

The most successful thin film active element is the thin film field effect transistor (TFT). Apart from having desirable electrical properties, it satisfies the important economic criterion that it may be deposited by the same means as the thin film passive components of an integrated circuit.

The deposition of thin film transistors upon the same substrate with passive components permits the fabrication of complex integrated circuits entirely by
evaporation. An entire circuit can be deposited upon an insulating substrate in one pump down of the vacuum system using movable masks for pattern determination.

The TFT is an insulated gate field effect transistor in which the current is modulated on the same basic principle as the Metal-Oxide-Semiconductor (MOS) transistor. The differences lie mainly in the properties of the materials, the reduced thickness of the semiconductor, the modes of conduction, the convenience in integrated circuit fabrication. The advantages in circuit fabrication lie in the isolation between elements due to the insulating substrate and in the single process (vacuum deposition) used to fabricate both active and passive elements.

Among II-VI compound semiconductors, cadmium sulfide and cadmium selenide have been studied for the fabrication of thin film transistors [1-5]. Intense interest has been generated in the application of thin film transistors [6] to various large area of electronic systems. In particular, a strong driving force is to develop TFTs as a switching elements for Liquid Crystal Displays (LCDs) and Electroluminescent Displays (ELDs). For the last few years these applications have received considerable attention. This is due to the development of the flat panel displays based on Electroluminescence and Liquid crystal. The flat panel displays have now considerable market particularly, in portable work station, Lap-top computer, flat TV in the commercial air passenger craft, and small size to large size display panels, etc.. The main advantage of TFTs that they can be deposited on to large-area glass panels, which makes them unique for addressing of displays [7].

Efforts have been made in the similar direction for the fabrication of CdSe thin film transistors in our laboratory and first time yttrium oxide (Y2O3) has been used as a gate insulator for TFTs. The drain and transfer characteristics of the CdSe
thin film transistors have been studied. Attempts have also been made to use the CdSe TFT for driving of a LCD Pixel.

7.2 EXPERIMENTAL

7.2.1 CdSe-TFT STRUCTURE AND FABRICATION

The TFT structure comprises of two laterally spaced electrodes called a "source" and "drain" joined by a thin semiconductor film whose conductivity can be modulated by a third electrode called "gate". The source and drain make an ohmic contact to the semiconductor, but the gate is separated from the semiconductor by a thin layer of insulator. In the fabrication of TFT, all materials were deposited by evaporation upon an ultrasonically cleaned glass substrate using mica mask for defining the patterns for semiconductor channel, gate insulator and gate electrode while using metal wire mask for source-drain gap. Figure 7.1 shows photograph of (a) a magnified CdSe-TFT and (b) a group of four CdSe-TFT deposited on glass substrate.

Figure 7.2 shows (a) the cross sectional view and (b) an overview of CdSe thin film transistor used in the present study. The CdSe thin film transistors were fabricated by utilizing a mask rotating system without breaking vacuum. The flow chart for the fabrication of CdSe thin film transistors is shown in Fig.7.3.

7.2.2 MEASUREMENTS

The thickness and the deposition rate of all layers were measured by the quartz crystal digital thickness monitor during evaporation. The source-drain gap was measured by travelling microscope. The drain currents, drain voltages and gate voltages were measured using the digital multimeters. The gate capacitance was measured by digital capacitance meter(Aplab).

7.3 RESULTS AND DISCUSSION

7.3.1 ELECTRICAL CHARACTERISTICS OF TFTs
Figure 7.1 Photograph of (a) a magnified CdSe-TFT and (b) a group of four CdSe-TFTs deposited on glass substrate.
Figure 7.2 (a) The cross sectional view (b) an overall view of the CdSe-TFT.
Figure 7.3 Flow chart for the fabrication of CdSe-TFTs.

1. GLASS SUBSTRATE
2. SOURCE-DRAIN ELECTRODE (Cr-100nm)
3. CHANNEL (CdSe-70nm)
4. GATE INSULATOR (Y2O3-100nm)
5. GATE ELECTRODE (Al-100nm)

Cleaning of the glass substrate

Loading the substrate into the vacuum unit

Pump down and maintain vacuum of the order of $2.66 \times 10^{-4}$ Pa

Deposition of chromium for making source-drain electrode by thermal evaporation technique (100nm thick) at $T_s = 303K$

Deposition of CdSe for making channel by thermal evaporation technique (70nm thick) at $T_s = 373K$

Deposition of Y2O3 for making gate insulator by electron beam technique (100nm thick) at $T_s = 303K$

Deposition of aluminum for making gate electrode by thermal evaporation technique (100nm thick) at $T_s = 303K$

Removing from vacuum unit

Measurement of I-V characteristics

Slowly annealing at 373K in high vacuum

1-GLASS SUBSTRATE
2-SOURCE-DRAIN ELECTRODE(Cr-100nm)
3-CHANNEL(CdSe-70nm)
4-GATE INSULATOR(Y2O3-100nm)
5-GATE ELECTRODE(Al-100nm)
Modulation of the semiconductor conductivity in the TFT by variation of gate potential results from the electrostatic attraction or repulsion of free carriers into source-drain region. On increasing the voltage steps applied to the gate a family of drain current curves is obtained, the drain current saturates at higher values of drain voltage. For drain voltages up to the knee of the curve, the drain current is given by the expression

\[ I_d = \frac{\mu_s C_g}{L^2} [(V_{ds} - V_o)V_{ds} - \frac{V_{ds}^2}{2}] \]

where \( \mu_s \) = mobility of CdSe thin film

\( C_g \) = gate capacitance

\( L \) = Drain-source separation gap

\( V_{ds} \) = Drain source voltage

\( V_o \) = Threshold voltage

Beyond the knee, the drain current saturates. The parameters of TFTs can be calculated using the following expressions:

The output drain resistance

\[ R_d = \frac{\delta V_{ds}}{\delta I_{ds}} \text{ at } V_g \text{ constant} \] (7.2)

The transconductance below the knee is

\[ g_m = \frac{\delta I_d}{\delta V_{ds}} \text{ at } V_{ds} \text{ constant} \] (7.3)

The amplification factor

\[ \mu_A = g_m \times R_d \] (7.4)
and The gain band width (GBW) product is \[
\frac{g_m}{2\pi C_g}
\] (7.5)

7.3.2 EFFECT OF ANNEALING ON THE I-V CHARACTERISTICS OF TFTs

Figure 7.4 shows the I-V characteristics of the CdSe-TFTs without having any post fabrication treatment. It has been observed that as the \(V_{ds}\) increases the drain current increases at the different gate voltages. It is found that the drain current does not saturate but increases with increase of \(V_{ds}\). It shows that almost linear non saturated characteristics. Their usefulness is limited because it is difficult to fit load line to the characteristics in such a manner that any significant modulation of drain potential is obtained.

WEIMER[8] suggested that the possible factors which can lead to non saturation characteristics are: (a) An unmodulated parallel conductance path between source and drain. Such a path would occur if the semiconductor is of relatively low resistivity and of a thickness greater than the maximum attainable space charge layer thickness. (b) Insufficient electrostatic shielding of the gap region from the drain field by the gate. This would occur with a high resistivity semiconductor if the source-drain gap is too small or the gate insulator is too thick. Under such conditions no channel is found, and the device could operate as a space charge limited triode. (c) Internal breakdown in the semiconductor channel in the high field region which exists near the drain for drain voltages above knee. (d) Insulator breakdown from the gate to the drain or to the channel near the drain.

In the present case there may be a possibility of the existence of a large number of electrons in the CdSe semiconductor channel. All these electrons may create an unmodulated parallel conductance path between source and gate which prevents a fully depletion of the semiconductor channel. Therefore drain current is unable to saturate at high \(V_{ds}\).
Figure 7.4 The drain characteristics of CdSe-TFT without annealing.
In order to resolve the problem the CdSe-TFTs were subjected to post fabrication heat treatment. CdSe-TFT were annealed at 373K for two hour in high vacuum. For annealing process, the rising of the temperature upto 367K and bringing back to 303K were done very slowly in order to avoid the formation of any internal creak in the deposited layers of CdSe-TFT.

After annealing of the CdSe-TFT, the drain characteristics were measured and are shown in the Fig.7.5. It is observed that the drain characteristics show saturation of drain current at high $V_{ds}$ at different $V_g$. This may be due to the improvement of the grain size, reduction of the intercrystalline barriers and improvement of carrier mobility in the CdSe thin film channel and also better ohmic contact between Cr and CdSe film. NORIAN[9] and ANDERSON[10] have reported similar type of observation on the effect of annealing on TFTs. Attention may also be drawn to fact that the annealing improves the adhesion of layers on the glass substrate.

The saturation of drain current occurs when the conduction channel is pinch-off in the vicinity of drain electrode. The I-V characteristics shown in Fig.7.5 is like an enhancement type TFT in which a positive gate voltage requires to onset the conduction. The enhancement in the conductance of n-type semiconductor takes place by a positive gate bias. The reason is that the gate electrode forms one plate of a capacitor with the CdSe semiconductor channel forming the second plate, so that a positive charge on the gate induces an equal amount of negative charge on the surface of the semiconductor near the semiconductor-insulator interface. Since the semiconductor is of n-type, the induced negative charge enhances its conductance in a thin surface region called the conduction channel.

Figure 7.6 shows the transfer characteristics ($I_d$ versus $V_g$ at constant $V_d$) of the CdSe thin film transistor. It is confirmed from the Fig.7.6 that the transistor is operated in an enhancement mode. It is found that the threshold voltage is 0.4Volt for CdSe-TFT. For the switching application the important parameter is the ON-OFF
Figure 7.5 The drain characteristics of CdSe-TFT with annealing.
Figure 7.6 Transfer characteristics of CdSe-TFT at constant drain voltage $V_{ds} = 5$ V.
current ratio. The ON-OFF current ratio of CdSe TFT is calculated and found to be about 22.

7.3.3 THE ELECTRICAL PARAMETERS OF TFT

The electrical parameters of CdSe TFT calculated using equations (7.2) to (7.5) and Fig.7.5, are listed in Table 7.1.

Table 7.1
Calculated Electrical parameters of CdSe Thin Film Transistor

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value (at specified condition)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drain resistance (R_d)</td>
<td>$3.1 \times 10^4 \text{ohm}$</td>
</tr>
<tr>
<td>Transconductance ($g_m$)</td>
<td>$1.7 \times 10^{-4} \text{mho}$</td>
</tr>
<tr>
<td>Amplification factor ($\mu_A$)</td>
<td>5</td>
</tr>
<tr>
<td>Gate capacitance ($C_g$)</td>
<td>395 pf</td>
</tr>
<tr>
<td>Gain Band Width product (GBW)</td>
<td>68 KHz</td>
</tr>
</tbody>
</table>

7.3.4 OPTIMIZATION OF SOURCE-DRAIN GAP

The most critical dimension in a TFT is the source-drain gap which is strongly dependent on the applied electric field which the TFT can sustain. It is observed that wider the source-drain gap (>100μm) more applied field is required to operate TFT. A fine metal wire was used as a mask for making the source-drain gap. A gap of 80μm was optimized for the TFT with reference to the thickness of gate insulator as well as semiconductor channel. Since the transconductance ($g_m$) of a TFT is inversely proportional to the dimension of the source-drain gap (L) it is desirable to make L as small as possible. But, practically it is difficult to make very small source-drain gap (<60μm) with a fine to the substrate. As a result, source and drain may be shorted by the diffused atoms of chromium in the channel.
One great difficulty in the development of thin film transistors has been an instability in the insulting layer and this causes a shift in the characteristics with time. This problem was equally serious in MOS transistors until the drift was reduced to acceptable values by minimizing contamination during processing. The principle sources of instability are attributed to mobile ions and charged oxygen vacancies which drift with the field in the insulator. When a field is applied in the transistor, the ions generated augment the effect of the applied field; the conductance of the channel continues to drift in the same direction as the initial charge caused by field effect. Thus, ion migration may be distinguished from the slow trapping of the carriers which causes the channel conductance to drift in the opposite direction of the initial response.

The Y$_2$O$_3$ is found to be stable gate insulator due to higher dielectric constant and consequently charge trapping less and higher charge migration in the gate insulator. The dielectric constant of Y$_2$O$_3$ is 12 which is higher than Al$_2$O$_3$ of 9[11]. It was also reported by KALLFAS[12] that larger dielectric constant of insulator increased the transconductance. In the present study, it was observed that the gate insulator having thickness less than 90nm was punctured under applied low electric field ($V_{ds}$ = 5Volt and $V_g$ > 2Volt). It was also observed that the gate insulator layer having thickness about 100nm can withstand electrical field of $V_{ds}$ = 5Volt and $V_g$ = 4Volt. An increase in thickness of gate insulator above 100nm results in a sacrifice of saturation of the drain current. Therefore 100nm was the optimized thickness of TFT to operate at suitable applied voltage range.

Good stability and reproducibility are important parameters for the commercial use of any electronic device. Looking into these requirements an attempt has been made to check the stability and reproducibility of the CdSe-TFT. The drain current of the CdSe-TFT was measured periodically at constant values of
V\textsubscript{ds}, V\textsubscript{g} and gate insulator thickness of 100nm. Fig 7.6 shows the drain current versus time. It is found that after few days of operation the current decreases within the range of 5\% which is indicated by the range bar. However, attention may be drawn to the fact that the deviation in drain current may be due to raising of contact problem, surface contamination, or any chemical changes over the surface of the film.

7.3.6 USE OF TFT AS A LIQUID CRYSTAL PIXEL DRIVER

Matrix addressing technique is most suitable technique for flat panel technologies of electroluminescence displays(ELDs) and liquid crystal displays(LCDs), in which each pixel is electronically connected between one row lead and one column lead. Active matrix is deposited by the thin film technology employing thin film transistor(TFT) as an active element\textsuperscript{6,7}.

In a CdSe-TFT display an array of TFTs was formed on one of the substrates. The sources were connected to their respective column lines, the gates to corresponding rows, row and column crossovers were insulated, and the back plane was covered by indium tin oxide(ITO).

The pixels shown in Fig. 7.8 are written with a driving voltage applied to the source electrodes. The row lines are addressed time sequentially so that only the gates in the row to be addressed are powered. In that row, only the source electrodes of the columns to be written are charged with the driving voltage. After a complete cycle the same row is addressed again.

Compare to the LCD pixel, EL pixel requires more current to drive it. Usually LCD consumes about 1000 times less power than that of EL. Our TFT output current is of the order of microampere which is sufficient to drive LCD pixel but unable to drive EL therefore we have utilized one LCD pixel for the case of study. Fig.7.8 shows that a CdSe-TFT used to drive one LCD pixel. LCD pixel is madeup of twisted numeric liquid crystal(TNLC) which is sandwiched between two indium
$V_{ds} = 5V$
$V_{g} = 4V$

GATE INSULATOR(Y$_2$O$_3$) THICKNESS = 100nm

Figure 7.7 Plot of drain current versus time.
Figure 7.8 An elemental driver circuit for Liquid Crystal Pixel using CdSe-TFT.
tion oxide (ITO) coated glass substrate. ITO film is highly conductive and optical transparent, which act as a transparent electrode. When CdSe-TFT turns ON it switch ON LCD pixel and change the contrast of the LCD, because applied field across pixel change phase of the liquid crystal in the pixel. Similarly when, CdSe-TFT is OFF LCD turns OFF and comes to the original phase. In our case CdSE-TFT as well as LCD both are discrete but for a fabrication of LCD display number of CdSe-TFTs in metrix with LCD are required to fabricated over the same substrate. This experiment verify that if we can decrease the size of CdSe-TFT as well as LCD pixel it may be useful in making a large size of a LCD display.

7.4 CONCLUSIONS

Thin film transistor have been fabricated using CdSe as the active semiconductor material and Y2O3 as the gate insulator. The various TFT electrical parameters were evaluated. The effect of annealing, thickness of insulator, source-drain gap on the performance of CdSe were also studied. The TFT was successfully used as a Liquid Crystal pixel driver.
REFERENCES

1 J. C. ERSKINE and A. CSERHATI,

2 V. DAMODARDAS and G. SRINIVASAN,

3 J. LEVINSON, F. R. SHEPHERD, P. SCANLON,
   W. D. WESTWOOD, G. ESTE and M. RIDER,

4 F. R. SHEPHERD, W. D. WESTWOOD, P. J. SCANLON
   J. LEVINSON, I. V. MITCHEL and H. PLATTNER,

5 A. VAN CLASTER,

6 F. OKUMURA, S. KANEKO,

7 A. G. FISCHER,
   Microelectronics, 7 (1976) 5.

8 P. K. WEIMER,
   Physics of thin films Vol. II (Ed. G. Hass and R. E. Thun,

9 K. H. NORIAN,

10 J. C. ANDERSON,

11 DIETER GERSTENBERG,
    "Handbook of Thin Film Technology", McGrow Hill Company, p.17.

12 T. KALLFASS and E. LUEDER,