List of Tables

Table 2.1: Comparison of Available Resources on Existing FPGA based Video Processing Platforms. .......................................................................................................................... 16
Table 2.2: FPGA Resource Utilization by Different Interfaces .......................................................... 32
Table 3.1: FPGA Resource Utilization by Clustering based Motion Detection System...................... 47
Table 3.2: Comparison of FPGA Resource Utilization by the Implementations of Proposed Memory Efficient Algorithm and the Original Algorithm. .............................................................. 78
Table 3.3: FPGA Resource Utilization by Motion Detection System and its Modules ....................... 79
Table 3.4: Performance Comparison with Existing Motion Detection Implementations ................. 80
Table 3.5: Frame Rates of Proposed Memory-Efficient Motion Detection Architecture for Different Video Resolutions ....................................................................................... 81
Table 4.1: Comparison of FPGA Resource Utilization for Sobel Compass Edge Detector: Standard Architecture versus Area Efficient Architecture Designed by us .................... 109
Table 4.2: Comparison of FPGA Resource Utilization for Sobel Compass Edge Detector: Standard Architecture versus Pipelined Area Efficient Architecture Designed by us ................ 109
Table 4.3: Comparison of FPGA Resource Utilization for Edge Width Computation Architectures: Standard Architecture versus Area Efficient Architecture Designed by us .............. 112
Table 4.4: FPGA Resource Utilization by Individual Modules of Focused Edge Region Extraction System and their Integration ........................................................................................................ 112
Table 4.5: FPGA Resource Utilization by Complete Implemented System for Extraction of Focused Edge Regions ................................................................................................................. 113
Table 4.6: Frame Rates of Proposed Pipelined Area Efficient Focused Region Extraction Architecture for Different Video Resolutions ........................................................................................ 114
Table 5.1: FPGA Resource Utilization by Object Tracking Architecture and Four Interfaces .......... 148
Table 5.2: FPGA Resource Utilization by Complete Implementation of Object Tracking System ... 149
Table 5.3: Performance Comparison with Existing Object Tracking Implementations .................... 150
Table 5.4: Frame Rates of Proposed Object Tracking Architecture for Different Video Resolutions. ................................................................................................................................. 151
Table 6.1: FPGA Resource Utilization by Complete Implemented Prototype Automated Video Surveillance System ........................................................................................................... 161