III-V compound semiconductors are the basic components of integrated circuits and are responsible for the startling rapid growth of the electronics industry in the past fifty years worldwide. The number and type of semiconductor devices have been growing steadily whether it is for high speed, lower power, higher efficiency or new functionality. The performance and reliability of all these semiconductor devices are dominated by their surface conditions. Hence, investigations on the surface and interface related properties of semiconductors are very much essential. The MIS structure is useful in surface studies because any change in processing that improves the electrical properties of the MIS structure makes the same improvement on the actual device.

Among the III-V compounds, indium phosphide (InP) is the potentially attractive material for the development of high-speed, high power devices and opto-electronic integration because of the high values of saturation current, breakdown voltage, electron mobility, thermal conductivity and radiation resistance. However, preparation of a mirror-like, well-defined InP surface is very difficult. Further, the high density of midgap states on the unpassivated surface of InP results in high surface recombination velocities and Fermi-level pinning that limit the device performance. These problems can be minimised by optimising the polishing conditions using suitable polishing solution in which the diffusion process is well behaved and by passivating the surface with a suitable passivating agent. In this investigation, cadmium sulfide (CdS) has been used as a passivating agent.
since it has been reported that CdS passivation improves the properties of the MIS structures. Explicit understanding of the defects in bulk semiconductor and in the oxide interface regions is necessary for the development of InP based device technology. DLTS is a highly sensitive technique and is able to differentiate the bulk and interface state traps. Hence, DLTS has been employed for the present investigations on InP based MIS structures to analyse the interface as well as bulk defect levels.

In this investigation, a systematic approach has been made to understand the polishing and passivation mechanisms in reducing the surface states on the LEC grown (111) n-type InP surface and to analyse the effect of process induced defects in InP MIS structures.

HBr:K$_2$Cr$_2$O$_7$:H$_2$O (BCA) based solution has been identified as a very good polishing solution for InP. The quality of the BCA polished InP surface has been analysed using low temperature Photoluminescence (PL) and High Resolution X-Ray Diffraction (HRXRD) measurements and has been compared with similar measurements carried out on InP samples polished with the conventional Bromine-Methanol (BM). An increase in the PL intensity has been observed for the BCA polished samples as compared to BM polished samples which establish the reduction in the surface states on BCA polished samples. XRD results for BM polished sample show an additional peak due to the porous nature of the surface which has not been observed in the BCA polished sample. Hence it is established that BCA is a better polishing solution for InP. Anodic oxides were used as insulators for the fabrication of MIS structures. Surface and compositional analysis of the oxides have been carried out using Atomic Force Microscopy (AFM) and X-ray Photoelectron
Spectroscopy (XPS) respectively. AFM results show a minimum surface roughness \( (R_{\text{ms}} = 18.4 \text{ nm}) \) for the oxide layer grown at the electrolyte pH value of 6. From the XPS analysis, it has been observed that the oxide layers grown at pH 5 and 7 are composed of \( \text{In}_2\text{O}_3 \) and \( \text{InPO}_3 \) while the pH 6 grown oxide layer is composed of \( \text{InPO}_4 \). From the C-V characteristics of MOS structures, it has been inferred that the BCA polished samples exhibit better electrical properties as compared to the BM polished samples and a minimum surface state density \( (N_{\text{SS}}) \) value as low as \( 6 \times 10^{10} \text{ cm}^{-2} \text{ eV}^{-1} \) has been obtained for the BCA polished sample.

CdS passivation on InP using Chemical Bath Deposition (CBD) technique at room temperature has been carried out. Passivation effect on InP surfaces has been analysed using low temperature PL measurements and the results show an increased PL intensity for CdS passivated InP samples and is maximum for 20 min passivated sample. CdS passivation of InP shows the removal of native oxides present on the InP surface as evidenced from the XPS analysis. The XPS results of anodic oxides on CdS passivated InP show the formation of a highly stable and a relatively very high resistive oxide layer of \( \text{P}_2\text{O}_5 \). XPS analysis at the interface indicates the fact that the sulfur atoms replace oxygen atoms in \( \text{In}_2\text{O}_3 \) and forms \( \text{In}_2\text{S}_3 \). The minimum \( N_{\text{SS}} \) value as low as \( 3 \times 10^{10} \text{ cm}^{-2} \text{ eV}^{-1} \) has been obtained for CdS passivated samples from C-V measurements. Positive bias stress measurements confirm the stability of the oxides.

An attempt has been made, for the first time, to fabricate BaTiO\textsubscript{3}/InP based MOS structures. BaTiO\textsubscript{3} films were deposited using sol-gel process. The composition of BaTiO\textsubscript{3} has been analysed using XPS and the formation of BaTiO\textsubscript{3} has been confirmed. The
minimum surface state density value calculated from the Terman analysis is $6 \times 10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$ and is comparable with other insulators.

DLTS measurements have been carried out on Au/SiO$_2$/InP, Au/Si$_3$N$_4$/InP and Au/BaTiO$_3$/InP type of MIS structures. The results show the presence of both majority and minority carrier interface traps as well as bulk traps. The bulk trap level with an activation energy of 0.62 eV was observed and was attributed to P$_{in}$ antisite defect. Bulk traps and interface state traps were distinguished by varying the applied reverse bias values. The effect of substrate temperature during the deposition of SiO$_2$ on InP has been studied. The minority carrier trap has been eliminated while depositing the SiO$_2$ at an elevated temperature. The interface trap with an activation energy value of 0.55 eV has been observed for both SiO$_2$/InP and Si$_3$N$_4$/InP samples while the insulator layers are deposited at the elevated temperature.

Defects created during proton implantation has been found to create a high resistive layer for device isolation. Investigations on the electrical properties of 80 keV proton irradiated n-InP MIS structures at different ion fluences have been carried out. C-V measurements carried out on the irradiated MIS structures show reduction in the accumulation capacitance value and very weak dependence on the applied bias with increase of the incident particle fluence. The effect of proton irradiation on Au/n-GaAs metal-semiconductor (MS) structures (SBDs) has also been studied. The GaAs samples used for the investigations are undoped n-type epilayers grown using Metal Organic Vapour Phase Epitaxy (MOVPE) technique. The electrical characteristics were analysed
using I-V, C-V and DLTS measurements. Enhancement in the barrier height has been observed for irradiated (fluence-1x10^{11} particles/cm^2) and 673 K annealed SBDs. C-V results show a decrease in the capacitance for all the annealed irradiated MIS structures and SBDs. DLTS studies on the SBDs show the presence of EL2 defect in the as-grown GaAs epilayer and the low energy proton irradiation enhances the concentration of EL2 defect.

The results of the investigations have been published in International journals and presented in several international/national conferences.