CHAPTER 7

SUMMARY AND SUGGESTIONS FOR FUTURE RESEARCH

7.1 SUMMARY

This thesis elucidates the problems associated with the surface of InP, which is the most promising material for opto-electronic applications, and the solutions to minimise the problems involved in the surface and interface in the aspects of polishing, passivation and insulating layer with the use of Metal-Insulator-Semiconductor (MIS) structures.

The materials properties and importance of InP, details about surface and interface states, the basic understanding of capacitance-voltage (C-V) characteristics of ideal MIS structures, the influence of surface states on the capacitance of MIS structure and the calculation of surface state density using Terman analysis have been reviewed. The effects of surface processing on the characteristics of MIS structures have been analysed in detail.

A new polishing solution, HBr:K₂Cr₂O₇:H₂O (BCA), has been realised as a better polishing solution for InP. The polishing conditions were optimised by varying the ratio of the constituents. The very good polishing action of BCA on InP has been affirmed using PL and XRD measurements. It has been shown that BCA is not only the best polishing agent for InP but also has been shown to be effective in realising better MOS structures. The effect of BCA in reducing the surface states was analysed using C-V measurements and a minimum surface state density ($N_{ss}$) value of $6 \times 10^{10}$ eV$^{-1}$ cm$^{-2}$ has been achieved on BCA polished InP surface while the $N_{ss}$ value obtained using conventional Bromine Methanol (BM) polishing is $8 \times 10^{10}$ eV$^{-1}$ cm$^{-2}$. For fabricating MOS structures, anodic oxides were used as insulators to avoid the thermal damages and it has been shown that the
oxides grown under the electrolyte pH value of 6 has high resistivity and high stability when compared to pH 5 and pH 7 grown oxides. Highly stable nature of oxides has been confirmed using C-V measurements.

To further reduce the surface states on InP, CdS passivation has been performed on BCA polished InP using chemical bath deposition technique at room temperature. The effect of CdS passivation on InP has been analysed using PL measurements. PL result exhibits enhanced intensity for CdS passivated surfaces and confirms the reduced surface recombination centres. XPS results prove that sulfur in CdS removes native oxide present on InP and forms chemically stable surface. XPS analysis on the anodic oxides grown on CdS passivated InP surface shows the formation of the high resistive and highly stable native oxide namely $P_2O_5$. CdS passivation yielded the minimum surface state density, $3 \times 10^{10}$ eV$^{-1}$ cm$^{-2}$, when compared to the unpassivated diodes. The C-V results confirm the best electrical properties with the lowest density of interface state and highest stability of CdS passivated InP MOS diodes.

An attempt has been made to find a suitable insulating material with high resistivity and high stability for the fabrication of InP MOS device. Barium Titanate (BaTiO$_3$), a dielectric material, is proposed as a new insulator, for the first time, to fabricate InP MOS structures. BaTiO$_3$ thin films have been deposited on InP substrates by sol-gel technique in which there is no thermal damage during deposition. Formation of BaTiO$_3$ thin film has been confirmed through XPS analysis. The minimum surface state density value as low as $6 \times 10^{10}$ cm$^{-2}$ eV$^{-1}$ has been obtained for Au/BaTiO$_3$/InP MOS structures and is comparatively less than that of the other deposited insulators.

Investigations on the process induced defects in the MIS structures have been carried out. The deep level transient spectroscopy (DLTS) system has been established in our laboratory to study the bulk as well as interface related defect levels in the fabricated MIS structures. DLTS measurements have been carried out on Au/SiO$_2$/InP, Au/Si$_3$N$_4$/InP and Au/BaTiO$_3$/InP type of MIS structures. Bulk traps and interface state traps were
distinguished by varying the applied reverse bias values during the measurements. The bulk trap level with activation energy of 0.62 eV was observed and it was identified as a \text{P}_\text{In} antisite defect. For the sample with SiO\textsubscript{2} deposited at the elevated temperature (423 K), new electron trap levels due to the interface states have been observed, while the trap levels that were observed in the room temperature SiO\textsubscript{2} deposited sample were absent since they might have been eliminated due to the elevated temperature of deposition.

To understand the influence of irradiation-induced defects on the electrical characteristics of Au/ Si\textsubscript{3}N\textsubscript{4}/InP MIS structures and Au/n-GaAs MS structures, low energy proton particles were irradiated using 150 kV accelerator. C-V and I-V measurements were used to analyse the effect of irradiation-induced defects on the properties of the diodes. The capacitance values decrease for all the irradiated diodes both for MIS and MS (SBDs) structures. Annealing the irradiated diodes further reduces the capacitance values. Surface state density value increases for the irradiated MIS structures. The decrease in the barrier height and increase in the ideality factor has been obtained for irradiated MS diodes. Annealing of the irradiated diodes reduces the reverse leakage current and increases the barrier height values which in turn improves the rectifying behaviour of the diode.

An enhancement in the barrier height as compared to the un-irradiated diode has been obtained for annealed (673 K), \textit{1}x\textit{10}^{13} \text{cm}^{-2} irradiated SBDs. DLTS measurements carried out on the SBDs show the presence of EL\textsubscript{2} defect in the as-grown epilayer and further, an increase in the concentration of the EL\textsubscript{2} defects by low energy proton irradiation has been observed.

7.2 SUGGESTIONS FOR FUTURE RESEARCH

In this investigation, BCA polishing has been shown to improve the surface quality of InP. Further work can be continued on polishing the InP surface using BCA by varying the polishing parameters such as the flow rate of the solution, rotation rate of the polishing pad, temperature of the solution, applied pressure, etc., to realise a better surface. Etching
studies on InP can also be done using BCA solution by varying the ratio of the components in BCA. As passivation enhances the device performance, it is very much essential to study the various passivation methods in detail. It has been reported that selenium is more stable than sulfur at high temperatures. Hence, selenium passivation studies may be attempted in understanding the passivation mechanism.

For the first time, BaTiO$_3$ (deposited using sol-gel process) has been used as an insulating material for InP MIS structures to overcome the problem of interface states produced during thermal deposition of insulators. The mechanism behind the properties of BaTiO$_3$ on the behaviour of MIS characteristics is yet to be understood. The stability of the BaTiO$_3$/InP interface can be further improved by passivating the InP surface and then depositing the insulator.

Many theoretical models such as Unified Defect (UD) model, Metal Induced Gap State (MIGS) model, Defect Induced Gap State model (DIGS), etc., have been proposed to understand the nature, origin and position of Fermi-level pinning due to interface states. The problem is not yet well understood. Hence, based on these models, more work on theoretical modelling can be developed to understand the interface related problems.

The DLTS system can be effectively utilised to understand the effect and origin of grown-in defects and process induced defects on the characteristics of the metal-semiconductor and metal-insulator-semiconductor structures. As all the devices should be functioned in radiation environment, irradiation studies on MIS structures using different ions with different fluences can be done. The fabrication of a complete device structure of Metal-Insulator-Semiconductor Field Effect Transistors (MISFETs) with different insulators can be tried.