ABSTRACT

ATM is a multiplexing and switching technology used to transport small fixed length packets called cells over high-speed network and is a basic building block for Broad Band Integrated Services Digital Network (B-ISDN). One of the primary factors that have hindered the deployment of fast Asynchronous Transfer Mode (ATM) networks is the speed requirement of the switches needed to interconnect ATM-capable workstations. The present work involves design and testing of a high-speed (8.5 Gbits/s) single chip two-port ATM switch using a novel architecture. There have been previous attempts to integrate much of the functionality of an ATM switch onto a single IC in order to reduce the size, cost and cell processing time of the switches. However, their switching capacities are limited by the conventional architectures. It is noted that the switching speeds of ATM can be tremendously increased by use of chip-to-chip optical interconnections with the existing architectures, which is not a cost effective solution. Moreover, use of Copper-optic converters, in spite of their high cost, introduces cross talk problems, which gives, rise to enormous increase in cell loss probability. This document describes preliminary high-level design and testing of a single-chip, two port ATM switch, to be implemented using VLSI.

Shared Medium and Shared Memory approaches to design of ATM switches do not scale well due to the speed up factor involved in the design and their
switching speeds are limited by the shared buffering strategies. This new design exploits the advantages of both the architectures as well as the advantage of parallel switching paths offered by Space division Architecture. The switch adopts multiple logical Input queuing strategies for buffering of cells, which gives significant improvements in the throughput of the switch. The new architecture enables easy scalability to larger number of ports and will provide guaranteed bandwidth and QoS due to space division approach. The novelty of the single chip design is that the design houses inbuilt routing tables for each of the input ports, main switching module, header validation module, memory module, memory controller and VPI translation tables. Very high switching speeds are achieved due to the single chip architecture, which eliminates transfer delays for header validation, VPI translations and switching operations that are presently done by separate modules. The architecture also offers the flexibility of selection of a suitable Switching Fabric according to the number of ports and the specific application. The memory architecture for Routing and Translation tables offers the facility for storing some advanced connection related information. The single chip architecture eliminates high cost chip-to-chip optical interconnections to achieve similar switching speeds, thereby avoiding cross talk problems. The simulation studies of the single chip design shows that switching speeds up to 8.5 Gbps can be achieved with the novel architecture.

The most important feature is that the regularity of the architecture and interconnection pattern makes the VLSI implementation of the single chip ATM switch a good proposition. The logical description for the design is done using
Verilog HDL. The real time performance of the design is tested in Field Programmable Gate Array (FPGA) with advanced feature sets. Testing the design in FPGA is done by designing advanced test control benches, which includes SDRAM controllers, block RAM assignments for memory mapping in the target device with modules in the design, Read Write controllers, Pin locking etc. The single chip design is synthesized and the generated bit stream is fused into the FPGA. The complex design consumes a total of 1,92,877 system gates in the FPGA. The input stream of bits is given to the single chip switch and tested for its performance, using test benches and the desired results are obtained. The constraints involved in testing the design in an FPGA matrix are solved and this gives rise to the scope that the single chip high speed ATM switch can be manufactured as an ASIC.