ABSTRACT

The rapid pace of technological change in communication and computers has introduced many new switching system concepts to cater to the needs of the users. Different switch fabric designs have been proposed and developed at various research organizations over the past few years. All these designs employ a high degree of parallelism, distributed control and the routing function. The self-routing networks are extensively used in communication and parallel processing applications. One of the popular self-routing networks is the Banyan network. The Banyan network is attractive for its simple routing scheme, hardware simplicity, regular structure and the ability to deliver multiple packets simultaneously. Its throughput is however limited due to its internal blocking and output contention due to its inherent nature. Banyan network because of its topology, simplifies the fault diagnosis problem. Several types of ATM switching architecture such as input buffered switch, output buffered switch and shared buffer switch have been proposed in the literature. In buffered Banyan networks, the buffers are added at the input ports of each switching element. When a conflict occurs, one packet is forwarded while the other is kept in the buffer. The throughput can then be increased. To avoid buffer overflow, flow control mechanisms are implemented between stages of the switching element. Yet, the switch can become congested if the traffic is bursty.
The Self-routing network allows distributed control of the individual switches in the network and can, therefore, be more advantageous than the conventional switch design in high-speed systems. This has a bi-tonic sorting network and a Banyan routing network. Various types of switching architecture proposed in the literature are discussed for their merits and demerits. It is noted that the Sunshine network, the self routing network, the Multipath self routing ATM switch and the PIPN basically use the Banyan topology for the design of the switch fabric. A switch design, which uses a topology other than the Banyan topology, needs complex hardware to give maximum throughput. Some of the switching networks discussed use buffers with sharing mechanism to enhance the throughput, but fail to reduce the latency of the switch fabric. Hence, this thesis focuses on the switch fabric design suitable for BISDN / ATM and various means to enhance its performance. The Banyan network with various buffering schemes taken up for study in this work. They are (i) The input buffered scheme, (ii) The inter-stage buffered scheme and (iii) The Shared output buffered scheme. The cell loss and delay caused by these schemes are presented. Also studies have been made to reduce the cell loss ratio by applying some error control techniques to recover the lost cells. Initially, the Sort Banyan architecture is applied with simple FEC technique and the performance in terms of cell loss and delay versus the cell arrival rate is presented. The performance obtained by this technique shows a significant improvement. But, the performance varies with the arrival rate and thus deteriorates at higher arrival rates. So, the Sort Banyan network with FEC technique is simulated along with
the inter-stage buffering scheme and the cell loss ratio and delay performance is 
presented. The result obtained does not show any improvement. Hence, a 
special class of coding namely the Reed-Solomon code is applied as the cell 
loss recovery mechanism to the Banyan network. The performance of this 
scheme is presented for cell loss and delay versus the 'h' parameter. Apart from 
the above, the Sort Banyan network is simulated with 2-degree dilation and the 
cell loss and delay performance is presented. The simulations of the networks 
mentioned above are carried out by assuming that the cell arrival is Poisson 
distributed. But from the recent literature, it is found that the ATM traffic 
behaves in a self-similar pattern. Hence, in order to validate the switch design, 
the Banyan switch architecture with the three different buffering schemes is 
studied using the Self-similar traffic model. Also, the FEC technique applied to 
the Sort Banyan network and the RS coded Banyan network are investigated for 
their performance using Self-similar traces and is presented. The performance 
of the cell loss recovery mechanism using the error correcting technique is 
found to be better compared to the buffering schemes. Some of the buffering 
schemes studied and the error correcting techniques applied to the Banyan 
switch architecture are implemented using VHDL. The delay performances of 
the implemented networks are compared for various utilization properties.