CHAPTER 5

POWER FACTOR IMPROVEMENT

5.1 INTRODUCTION

For major industries power is supplied by the utility network at high or extra high voltage. The summary of power tariff schedule for all state electricity boards in India (1977) tells that the power tariff structure is obviously two part: one part for maximum demand charge and the other for energy charges. The maximum demand charges are based on maximum KVA demand and, therefore, penalty for low power factor is in-built in the tariff. In addition, penalty for low power factor is directly imposed in many cases. This is the main reason for the large industries to attempt at the improvement of their load power factor, allowing more efficient utilisation of the transmission / distribution system of the utility network as per the report IEC-555, Part III (1982). Nature of reactive power compensation to be adopted for a particular plant is dictated by the load characteristics as per papers (J. Arrilaga 1978, G.L. Kusic 1984, IEEE guide 1990). In 1914, fixed shunt capacitor banks were first used for the improvement of power factor. These fixed capacitor banks can cause problem at light load conditions as per papers (Timothy R. Feldman 1984, S.A. Nasar 1987). To have control over VAR compensation, switched capacitors together with controlled reactors can be employed as per reports (R.P. Stratford 1976, T.J.E. Miller 1982, V.P. Ramamoorthy 1986).

5.2 DIFFERENT TECHNIQUES TO CONTROL POWER FACTOR

5.2.1 Power factor improvement using solid state devices

The efficiency and the power factor of a normal induction motor are dependent on the load and are maximum when the load on the motor is nearer...
to its rated capacity. At light loads, these two factors fall drastically down to a poor value as per literature (R.F. Horrell 1954; L. Gyugyi 1979; T.N. Rowan 1982).

The magnetizing current, which is lagging in nature, remains unaltered for different loads when the motor is operated at a constant voltage, thereby affecting the power factor.

The power factor decreases at reduced loads. One way to improve the above situation is to reduce the magnetising current at light loads. This helps in improving the power factor as per literature (B.R. Pelly 1971; Frank J. Nola 1984).

For light loads the reduction of magnetizing current can be easily achieved by the reduction of the input voltage to the motor. Figure 5.1 shows the vector diagram of induction motor under normal operation. Figure 5.2 shows the effect of the reduction of magnetizing current on the no load/light load power factor.

An excellent voltage control can be easily achieved by using phase controlled antiparallel SGRs. Figure 5.3 shows the connection of the ac power controller to the induction motor. The thyristors 1,3 and 5 are triggered in positive half cycle and 2,4 and 6 in negative half cycle of the respective input ac voltage (Syril W. Lander 1981; P.C. Sen 1981; T.W. Jain 1983; Vedam Subramaniyam 1988).

When the desired power factor is more than the operating power factor, the firing angle is increased to reduce the voltage applied and thereby reducing the magnetizing current. Conversely, if the desired power factor is less than the operating power factor, the firing angle is decreased to increase the voltage applied and thereby increasing the magnetizing current as shown in literature (IEEE tutorial text 1978; L.J. Bohmann 1986).
FIGURE 5-1 VECTOR DIAGRAM OF INDUCTION MOTOR UNDER NORMAL OPERATION
FIGURE 5-2 IMPROVEMENT OF POWER FACTOR ON REDUCTION OF MAGNETIZING CURRENT
FIGURE 5.3 AC POWER CONTROLLER USING ANTIPARALLEL THYRISTORS
5.2.2 Power factor improvement using dual stator windings

The power factor of an induction motor can be improved by means of solid state excitation, wherein an auxiliary three phase stator winding is used to feed excitation power to the machine through a pulse width modulated (PWM) inverter as per paper (Eduard Muljadi 1989).

When the PWM inverter of Figure 5.4 is provided with a suitable feedback control, the main winding of the induction machine can be controlled to carry only the active power and the auxiliary winding to carry only the reactive power. PWM inverter serves to act as a buffer to circulate reactive power between the machine windings and the dc capacitor. The dc voltage required for the PWM inverter can be supported by the capacitor and need not be connected to a power source. The PWM inverter can be controlled (voltage amplitude and phase) in such a manner so as to always provide the desired power factor at the terminals of the main winding. With sufficient ampere-turn capacity of the auxiliary winding, unity power factor operation of the main winding is possible over a wide range of load conditions including rated load. The principle of solid state excitation of an induction motor can be well understood from the equivalent circuit of Figure 5.5 as per paper (T.A. Lipo 1980). The dual stator windings can be effectively modelled by two branches each having separate resistance and leakage reactance together with a common mutual inductance $X_m$. This inductance accounts for the mutual coupling between the two sets of stator windings, occupying the same slots, due to their leakage flux (ie., non-air gap component of stator flux) as per reports (I.Takahashi 1980; Y.Harunoto 1981). When the PWM inverter is controlled to pass only reactive power its effect can be represented in the equivalent circuit by a variable capacitor, which is functionally dependent on the voltage across the capacitor as per paper (P.C. Krause 1969; A.T. Kefalas 1978).
FIGURE 5-4: INDUCTION MOTOR WITH AUXILIARY PWM INVERTER EXCITATION
FIGURE 5.5 EQUIVALENT CIRCUIT OF DUAL THREE PHASE INDUCTION MOTOR
5.2.3 Power factor improvement using SVC

To improve load power factor as per papers (K.Reichert 1974; L. Gyugyi 1978; J.D. Ainsworth 1979) Static Var Compensators (SVC) can be designed to meet the varying reactive power requirement of loads. An induction motor with a fixed capacitor and thyristor controlled reactor (FC-TCR) is shown in Figure 5.6. The SVC is composed of delta connected fixed capacitors in parallel with delta connected TCRs.

In Figure 5.6, \( Q_S \), \( Q_L \) and \( Q_{SVC} \) relate to net reactive power supplied by the source, consumed by the load and generated by SVC, respectively. For unity power factor operation at load terminals, the following conditions should be satisfied as per literature (R.P. Gupta 1990).

\[
Q_{SVC} = Q_L \tag{5.1}
\]

The reactive power generated by SVC is given by

\[
Q_{SVC} = 3V_L^2 wC - 3V_L I_{TCR} \tag{5.2}
\]

The reactive power absorbed by the load is

\[
Q_L = \sqrt{3} V_L I_L \sin (90^\circ - \phi) \tag{5.3}
\]

Substituting (5.2) and (5.3) in (5.1), the required susceptance of TCR is obtained as

\[
B_{TCR} = \frac{[V_L wC - (1/\sqrt{3}) I_L \cos (90^\circ - \phi)]/V_L}{\pi wL_{TCR}} \tag{5.4}
\]

The TCR susceptance is related to the firing angle of thyristor as given by,

\[
B_{TCR} = \frac{\pi - 2\alpha - \sin (2\alpha)\pi wL_{TCR}}{\pi wL_{TCR}} \tag{5.5}
\]
FIGURE 5.6 INDUCTION MOTOR CONNECTED IN SHUNT WITH DELTA CONNECTED SVC
Knowing the value of \( w_C \) and the on-line load voltage \( V_L \) and reactive load current component \( I_L \cos (90^\circ - \phi) \), the required magnitude of \( B_{TCR} \) can be calculated using (5.5). \( \alpha \) is then found from a look-up table, representing the equation (5.5). This value of \( \alpha \) is utilized to gate the thyristors of the TCR to get unity power factor.

5.3 POWER FACTOR MEASUREMENT USING MICROPROCESSOR

5.3.1 Using signal amplitudes and power

This method involves a direct approach using the basic relation as given in the paper (K.Balasubramaniam 1984).

\[
\text{Power} = V_{\text{rms}} I_{\text{rms}} \cos \phi \quad (5.6)
\]

and computing the PF directly as follows

\[
PF = \cos \phi = \frac{2 \times \text{Power}}{V_{\text{max}} I_{\text{max}}} \quad (5.7)
\]

The procedure for computing \( \cos \phi \) is illustrated in Figure 5.7. The amplitudes of voltage and current are determined by comparing the successive samples of the same signal (either the voltage or current), until the absolute value of a particular sample of a signal falls below that of its previous sample. To improve the accuracy, this operation is repeated over \( G \) number of cycles, and the average value is taken. In fact, the maximum of these \( G \) determined amplitudes seems to be appropriate but it demands that there exist no surge. In the first phase of computation, power is determined over a period of 0.5s as reported earlier in paper (J.J. Hill 1981), and is also retained in the memory. During the next 0.5s period, \( V_{\text{max}} \) and \( I_{\text{max}} \) are determined and the PF is computed. The display subroutine is then initiated to display the PF or power as desired.
FIGURE 5.7 FLOW CHART- POWER FACTOR MEASUREMENT SCHEME INVOLVING SIGNAL AMPLITUDES AND POWER
5.3.2 Using RMS values of signals and power

Power Factor (PF) is defined as

\[ PF = \frac{\text{average load power}}{V_{\text{RMS}} \times I_{\text{RMS}}} \]  

(5.8)

In mathematical form, it is equal to

\[
PF = \frac{1}{T} \left[ \frac{1}{T} \int_{0}^{T} v(t) \cdot i(t) \, dt \right]^{1/2} \cdot \left[ \frac{1}{T} \int_{0}^{T} v^2(t) \, dt \right]^{1/2}
\]

(5.9)

where \( T \) is the period of both the signals. The evaluation of Equation (5.9) can be performed by using sampled data as per literature (S.S. Omran 1987). Both the current and voltage signals are sampled simultaneously at regular time intervals. Thus the cycle is divided into ‘n’ sections. Each section has its corresponding voltage \( v_j \) and current \( i_j \) samples. Power factor is computed numerically through the equation.

\[
PF = \left[ \frac{1}{n} \sum_{j=1}^{n} v_j i_j \right] \cdot \left[ \frac{1}{n} \sum_{j=1}^{n} v_j^2 \right]^{1/2} \cdot \left[ \frac{1}{n} \sum_{j=1}^{n} i_j^2 \right]^{1/2}
\]

(5.10)

where \( n \) is the number of samples taken per cycle, \( v_j \) is the amplitude of \( j^{\text{th}} \) voltage sample and \( i_j \) is the amplitude of the \( j^{\text{th}} \) current sample.
The software section of power factor measurement can be classified into four parts.

a. Sample/hold and analog to digital conversion and storing the digital data.
b. Calculation of power factor from these stored digital values.
c. Lag-lead indication.
d. Displaying of calculated power factor value.

These four parts are explained briefly below.

a. The ports of programmable peripheral interface (PPI) are used to read voltage and current samples. The maximum number of samples per cycles is limited to 76 due to the large conversion time of the ADC's used. By writing necessary control words, PPI initiates sampling and analog to digital conversion. The digitised voltage signals and current signals are stored in memory.

b. The second section of the software deals with the calculation of power factor from the stored digital values. Power factor calculation involves the calculation of three quantities. They are

1. Average power
2. \(V_{\text{rms}}\)
3. \(I_{\text{rms}}\)

To calculate average power the samples of v & i corresponding to the same instant are multiplied and then stored in the memory. From the table of vi products, positive vi and negative vi products are separated. These are summed up separately and finally average power is calculated. To calculate \(V_{\text{rms}}\), voltage samples are squared and then summed up. The final value is divided by the number of samples and square root is taken to find \(V_{\text{rms}}\). The above said procedure is used to find \(I_{\text{rms}}\) also.

From \(V_{\text{rms}}, I_{\text{rms}}\) and average power, power factor is calculated as given by

\[
PF(\%) = \frac{\text{Average power} \times 100}{V_{\text{rms}} \times I_{\text{rms}}} \quad (5.11)
\]
This value of power factor is stored in memory which is referred later for display.

5.3.3 Using angle difference between the signals

Power factor can be measured using microprocessor with minimum hardware as developed by the authors V.P. Ramamoorthy and R.Subramanian (1986).

The microprocessor measures the time between positive going zero crossings of the voltage and current signals. The software starts incrementing a counter from the positive zero crossing of the voltage wave and stops it at the following positive zero crossing of the current wave. The value of the count is proportional to the phase angle between the voltage and current signals.

5.4 MICROPROCESSOR BASED POWER FACTOR CONTROLLER

5.4.1 Overview of the control scheme

The block diagram of the microprocessor based system for control of power factor is shown in Figure 5.8. The desired factor is entered into the microprocessor by the operator through thumbwheel switches which have been interfaced to the microprocessor. The voltage and current crossing circuits make the microprocessor to compute the actual system power factor. Depending on the difference between the desired and actual power factors, the power factor control algorithm adjusts the switching schemes of capacitor banks and firing schemes of thyristorised phase controlled inductor in the power circuit.

LEDs are provided to indicate the lead and lag power factor and also situations when the power factor cannot not be improved.
FIGURE 5.8 OVERVIEW OF CONTROL SCHEME
5.4.2 System hardware

The system power circuit is shown in Figure 5.9. It consists of three phase delta connected switched capacitors along with thyristorised full wave phase controlled inductance. The switching of capacitor banks on and off the line is done through three phase contactors.

5.4.3 Interface circuitry

Interface circuitry is used to interface the microprocessor to the thyristor firing circuits, contactor driver circuits and LED driver circuits. All these circuits are shown in Figure 5.10. In phase control circuits the thyristor which has more forward bias should get the triggering pulse at its gate. For this purpose a synchronising circuit is used. The synchronising circuit is a conventional circuit comprising of synchronising transformers, zero crossing detectors and one-shots. The three phase line-status from synchronising circuit are fed to the input port of 8255II to select the firing sequence software. 8255II output port supplies the firing signals to the buffer stages. Buffer stage comprising transistors T_{r1} and T_{r2} with pulse transformer, is used for isolation between triggering circuit and power circuit as per literature (National TTL Logic Data Book, 1983). Contactor coil driver is obtained using transistor T_{r3} and T_{r4}. T_{r5} to drive LED display. Similar circuits are constructed for the other phases.

5.5 SOFTWARE

The various steps of the software developed for automatic power factor correction are:

a) measurement of system power factor
b) comparison with the reference power factor to find the error
c) switching of capacitors and
d) changing the firing angle of TCR to minimise the error in power factor.
FIGURE 5.9 SYSTEM POWER CIRCUIT
FIGURE 5.10 MICROPROCESSOR SYSTEM FOR POWER FACTOR IMPROVEMENT
The complete flow chart is given in Figure 5.11. The reference power factor is set on the thumbwheel switches. If the reference power factor is less than the minimum value, the microprocessor will indicate that the set power factor is low.

If the reference power factor is above the set minimum value, the microprocessor checks whether the port pin connected to the voltage zero-crossing circuit has gone high (The pin goes high at the zero crossing). When the pin goes high the C register is initialized and then incremented by one. The microprocessor then checks whether zero crossing of current has occurred while each time incrementing the C register. Once the zero crossing of current occurs, the value stored in C register, when multiplied with the number of T states of the loop, gives the actual count Na.

The microprocessor takes the reference count Nr from the lookup table corresponding to the set power factor and compares it with the actual count. Since the count is of two bytes, the higher order byte (H.O.B.) is first compared. If the values are the same, then the lower order byte (L.O.B.) is compared. If Nr equals Na then the actual count Na is compared with the count corresponding to 90° (N90). If N90 equals Na or is greater than Na, the microprocessor displays the lagging power factor.

If Nr (L.O.B.) is greater than Na (L.O.B.) by more than the tolerance band, then microprocessor decrements the phase angle and the above steps are repeated until Nr equals Na.

If Na (L.O.B.) is greater than Nr (L.O.B.) by more than the tolerance band, the microprocessor increments the phase angle and again checks the voltage and current crossings to make the actual power factor equal to set value.

Now, if higher byte of (Nr-Na) is positive, then the microprocessor checks whether all the capacitors have been switched off. If not, capacitor value is
CHANGE THE SWITCHING SEQUENCE
no ywK VWJEN.NO
CHANGETHE SWITCHING SEQUENCE
TO DECREASE CAPACITORS

DISPLAY DISPLAY
LAG PF
DECREMENT a

INCORENT a
ze - Zero crossing
Nh - Reference count
Na - Actual count
H.O.B. - Higher order byte
L.O.B. - Lower order byte
No = Count at 90°
a - Firing angle of thyristor

FIGURE 5.11 FLOW CHART TO SWITCH ON/OFF CAPACITORS
AND PHASE CONTROL THYRISTORS
decreased and the microprocessor reads the voltage and current ports. If all the capacitors have been switched off and still \( N_r \) is greater than \( N_a \), the power factor cannot be changed further. If it happens that \( N_r \) (H.O.B) is less than \( N_a \) (H.O.B), then capacitor value is increased. If all the capacitors, have been switched on and still if \( N_r \) (H.O.B.) is less than \( N_a \) (H.O.B.) then the power factor cannot be improved further. Table 5.1 gives the relationship between the effective capacitance values and the state of the port C. While switching the capacitors, if it happens that the actual count exceeds the reference count, then the thyristors are fired to include inductance.

The firing pulses are modulated and given to respective thyristors (\( T_1 \) to \( T_6 \)) via buffer stages. Modulation of firing pulses are essential to have reliable firing of thyristors driving inductive loads. The sequence of firing of thyristor is shown in Tables 5.2a, 5.2b and 5.2c as given in literature (W.N. Cheng 1969; Hoany Le-Huy 1982; S.B. Dewan 1983). Table 5.3 shows the data for the power factor control scheme.

5.6 CONCLUSION

A simple technique for automatic control of power factor is presented. Thyristorised fullwave phase controlled inductor gives an accurate power factor control. The system hardware is reduced to a minimum and hence, less maintenance and greater reliability can be expected. The control is implemented by software and hence any modification of the control logic can be done easily.
TABLE 5.1 VALUES OF CAPACITORS AND STATES OF PORT C PINS

<table>
<thead>
<tr>
<th>PC₂</th>
<th>PC₁</th>
<th>PC₀</th>
<th>Number of capacitors switched on</th>
<th>Capacitance included (p.u)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>No capacitors switched on</td>
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</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>C₁ switched on</td>
<td>1</td>
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<td>0</td>
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<td>0</td>
<td>C₂ switched on</td>
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<td>1</td>
<td>C₁ and C₂ switched on</td>
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<td>0</td>
<td>C₃ switched on</td>
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<td>1</td>
<td>1</td>
<td>0</td>
<td>C₂ and C₃ switched on</td>
<td>6</td>
</tr>
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<td>1</td>
<td>1</td>
<td>C₁, C₂ and C₃ switched on</td>
<td>7</td>
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### TABLE 5.2a FIRING SEQUENCE [0 < \( \alpha < 60^\circ \)]

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<th>Line Status</th>
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<tr>
<td></td>
<td>( P_{B7} X )</td>
</tr>
<tr>
<td>R</td>
<td>Y</td>
</tr>
<tr>
<td>---</td>
<td>---</td>
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<td>0</td>
<td>0</td>
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<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

\( X \): Don't Care  
\( Th \): Thyristor
### Table 5.2b Firing Sequence [$60^\circ < \alpha < 120^\circ$]

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<tr>
<th>Line Status</th>
<th>X : Don't Care</th>
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<tbody>
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<td>X</td>
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<td>0</td>
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<tr>
<td>1</td>
<td>1</td>
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</tbody>
</table>

Th : Thyristor
### TABLE 5.2c FIRING SEQUENCE \([\alpha > 120^\circ]\)

<table>
<thead>
<tr>
<th>Line Status</th>
<th>R</th>
<th>Y</th>
<th>B</th>
<th>(P_{B7})</th>
<th>(P_{B6})</th>
<th>(P_{B5})</th>
<th>(P_{B4})</th>
<th>(P_{B3})</th>
<th>(P_{B2})</th>
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<th>(P_{B0})</th>
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<td>1</td>
<td>0</td>
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</tr>
</tbody>
</table>

\(X\) : Don’t Care  \hspace{1cm} \(\text{Th} : \text{Thyristor}\)
### TABLE 5.3 DATA FOR POWER FACTOR IMPROVEMENT SCHEME

<table>
<thead>
<tr>
<th>Detail</th>
<th>Values</th>
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<tbody>
<tr>
<td>Horse power</td>
<td>7.5 hp</td>
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<tr>
<td>Full load current</td>
<td>20.7 A</td>
</tr>
<tr>
<td>Supply voltage</td>
<td>220 V</td>
</tr>
<tr>
<td>Speed</td>
<td>950 rpm</td>
</tr>
<tr>
<td>Condenser banks values</td>
<td>1 kvar, 2 kvar, 4 kvar</td>
</tr>
<tr>
<td>Inductance value</td>
<td>2 kvar</td>
</tr>
<tr>
<td>Power factor range</td>
<td>0.7 to 0.99 lagging</td>
</tr>
</tbody>
</table>