CHAPTER IV

STUDIES ON PROCESS INDUCED DEEP LEVELS IN SILICON

4.1 Introduction :

It is well known that the presence of impurities and defects play an important role in determining the behaviour of semiconductor materials and hence the devices. In silicon device fabrication technology, the semiconductor undergoes various process related thermal and chemical treatments. Despite the intended purpose, these treatments may result in introducing impurities and defects in the semiconductor crystal. For example, high temperature long time treatment of silicon results in development of point defects, thermal donors, quenched-in-defects, oxidation induced stacking faults etc. The amount of impurity incorporated depends on the process time, temperature and also on the diffusion induced stress. In the manufacture of silicon power devices like power diodes, triacs, thyristors, the high voltage requirements demand the use of lightly doped (10^{13}-10^{14} cm^{-3}) base regions. In such applications, minority carrier lifetime is an important parameter, which determines the device switching speed, reverse leakage current and conduction losses. In the normal production of a power semiconductor device there is a trade-off between the minority carrier lifetime and forward voltage drop. This is achieved by careful control of the processing conditions. Therefore, it is important to be able to control the carrier lifetime which can be affected directly or

indirectly by point defects, stacking faults, dislocations, carbon, oxygen and metallic impurities [1].

Depending on various processing parameters such as temperature, ambient, chemicals used and cooling rate different defect levels result in the bandgap of Silicon. Long time (2-20 hours) high temperature (1000-1200°C) heat treatment of silicon and then quenching to room temperature or even to lower temperatures result in introduction of quenched-in centers in silicon [2]. Highly strained surface layers (caused by the presence of very high concentration surface layers of phosphorus or boron) serve as source of vacancies. At high temperature treatments, these vacancies rapidly diffuse in to the bulk [3]. High temperature treatment of the wafers having rough surfaces (i.e., highly strained and disordered surfaces) also act as source of defects in silicon. Repeated heating and cooling will result in generation of more defect centers in silicon than long time high temperature treatment [3]. Thermal oxidation of silicon usually results in oxidation induced stacking faults (OSF) and anomalous diffusion substitutional dopants [4]. It is well known that prolonged heat treatment of silicon even at low temperatures (300 - 500°C) results in generation of thermal donors in silicon [5].

Presence of deep lying recombination centers in the conventionally diffused power silicon devices is well known. In particular deep diffusion of aluminium in power semiconductor fabrication under different experimental conditions

result in introduction of deep levels in silicon [6].

Marchand et.al.,[7] observed four deep levels in silicon after heat treatment in dry O_2 at temperatures greater than or equal to 1000°C for various lengths of time. It was concluded that these levels are 'aluminium - Oxygen' related complexes. It was observed [8] that the high-concentrated phosphorus diffused layer on Al doped p-type Silicon acts as sink for this 'aluminium - oxygen' deep levels.

Gresserov et.al.,[9] and Vyzhigin et.al.,[10] observed several deep levels in silicon, deep diffused with aluminium under different atmospheres.

Metal contamination in silicon from various sources is another factor to be considered. Fast diffusing metal impurities in silicon are detrimental because they result is killing lifetime of the minority carriers. Generally observed metallic impurities in silicon are the III group transition metal elements such as Ti, Cr, Mn, Fe, Cu, Mo, Ta, Pt, and Au [11]. The possible sources for the metallic contamination in silicon during devices processing are the chemicals used for cleaning and doping [12], quartz glassware used in diffusion furnace [13]. In order to inactivate partially or completely the defects or the metal impurities in silicon several techniques are formulated over the years.

High temperature quench-in centers introduced in silicon (formed by quenching the samples, heat treated at high temperatures for long time) are found to be annealed out by

very slow cooling (25°C/hr, till the sample temperature reaches 650°C and then quench to room temperature) after high temperature process [2].

It is well known that very high concentration of surface phosphorus or Boron layers or surface oxide glasses such as phosphosilicate or borosilicate glasses (PSG or BSG) getter most of the metallic and defect centers in silicon [3,14].

Presence of deep energy levels in the silicon power semiconductor devices has two major consequences. Firstly, the deep levels affect the minority carrier lifetime and in turn degrade the forward conduction characterstics of thyristors and p-i-n diodes. During conduction the base region is flooded with minority carriers and hence the resistance of this region becomes low to carry large currents. Since the current density is inversely proportional to the diffusion length, special efforts should be made to minimise the presence of deep levels. Secondly, condensation of deep impurities around dislocations results in metallic precipitates. This causes distortion of the potential line located in the depletion region of a p-n junction. This leads to localised regions of high electric field through which excess leakage current will flow. Consequently, " soft spots" and " soft breakdown" characteristics are observed with excess reverse (leakage) currents at voltages below the avalanche voltage. If these precipitates or soft spots are minimized or completely eliminated, the sharpness of the reverse Current-

Voltage characterstics will improve along with the minority carrier lifetime.

To enhance the performance and also to improve the yield in the manufacturing of thyristors particularly the study of process induced defects and impurities is very important.

In the present work, we made an attempt to analyze and study the deep level impurities and defects introduced in to the thyristor grade silicon under different processing conditions. Measurements such as DLTS, forward voltage drop and carrier lifetimes by open circuit voltage decay (OCVD) are carried out to find the effect of processing steps in the device making. Also, the efforts made to improve the carrier lifetime and device conduction characteristics using gettering and passivation are discussed.

Thyristors operate at high voltages (2000-3000 Volts) and currents (100-3000 amps). To operate at such high currents, generally the area of the device should be large (some times full wafers of 100 mm dia are used for making a single device). Therefore, uniform doping concentration is essential over the entire wafer. Otherwise the weak points are vulnerable for breakdown. Generally, neutron transmutation doped (NTD) wafers are used as the starting material in the fabrication of thyristors, as the doping in these type of wafers is extremely uniform [15]. It is well known that aluminium diffuses fast in silicon, it is used as p-type

dopant in the fabrication of deep junctions in the power semiconductor devices. In addition to aluminium, gallium is also used for p-type diffusion, because gallium diffuses even through the native silicon dioxide layers [15].

Diffusion of aluminium in silicon is influenced by the ambient under which the diffusions are carried out [9]. High temperature treatment of silicon results in introducing deep levels in the bandgap of silicon and this is also influenced by the ambient atmosphere [7-10]. Generally high temperature, long time heat treatment result in supersaturation of silicon with intrinsic point defects and these may be influenced by the ambient atmosphere during the heat treatment [4,16,17] and on the cooling rate [3].

4.2 Experimental work :

Starting material used for fabricating the devices is semi-processed 5 cm dia, 800 μm thick, 140-200 Ω-cm, Float Zone grown, neutron transmutation doped (NTD) n-type silicon wafers. Aluminium is used for deep p-type diffusion. For required impurity profile in the thyristors (high concentrations of the order of 10^{18} cm^{-3} near the surface) gallium is used in addition to aluminium. After p-type diffusion phosphorus is selectively diffused simultaneously from both sides to form n^+ regions on both sides. All the devices fabricated have 'n^+-p-n-p-n^+' structures as shown in Fig.4.1 and are fabricated at M/S Bharat Heavy Electricals Limited, Bangalore, India.

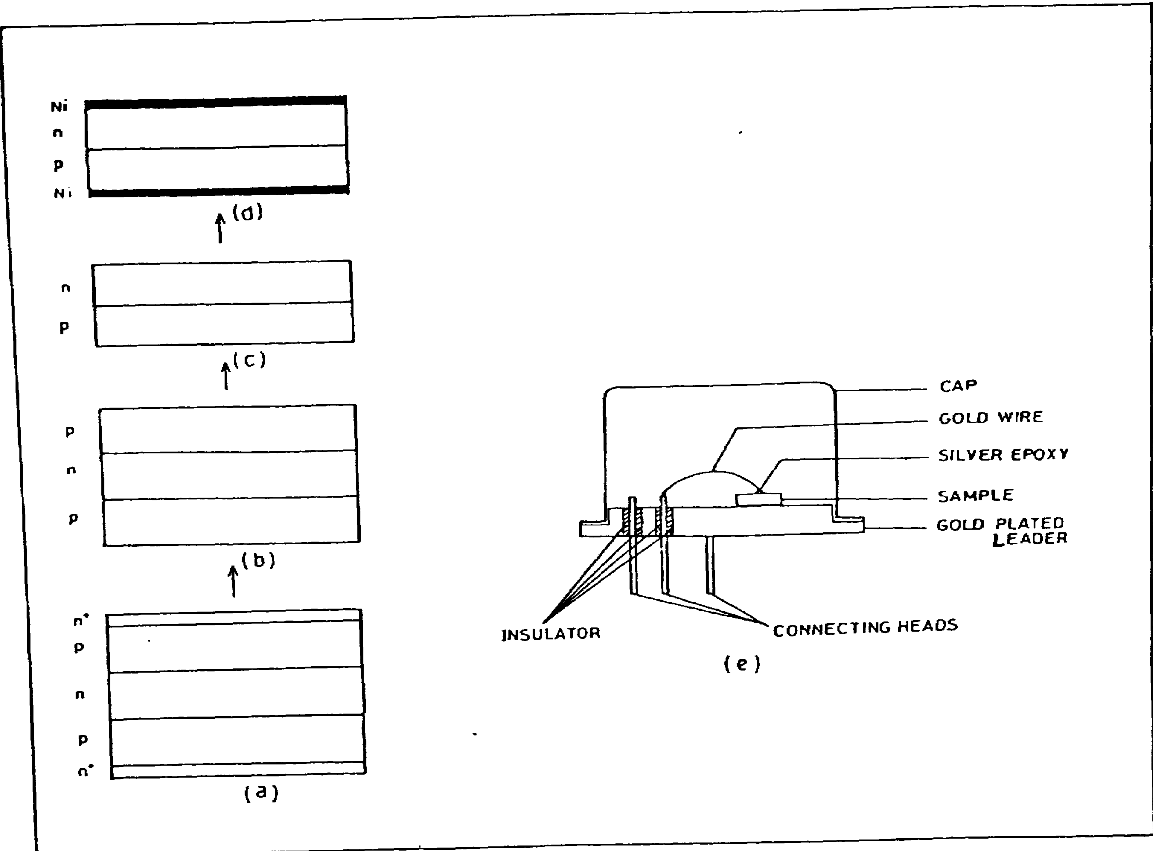


Fig.4.1 (a-d)Sample preparation for DLTS
(e) Sample mounting on TO-5 header

Aluminum or aluminium and gallium diffusions in the starting materials were carried out under different conditions for different samples as described below.

Sample 1 : First deposition of aluminium is done by heating the silicon wafers placed in an aluminium enriched quartz tube at 990°C for about 45 minutes in vacuum. Then drive-in is done by heating the aluminium deposited silicon wafers, kept in an open tube, at 1300°C for 10 hrs in oxygen atmosphere. The wafers are allowed to cool slowly (1-3°C/m) by switching-off the furnace heater power supply. After reaching the temperature of about 700°C, the samples are drawn out of the furnace and quenched in air.

Sample 2 : Aluminium diffusion is carried out similar to process followed in the case of sample 1 except that the drive-in diffusion is carried out at 1190°C for 10 hrs.

Sample 3 : Standard sealed tube diffusion procedure is employed for p-layer fabrication. In this process the silicon wafers stacked in a silicon tube are placed in a quartz ampoule along with pure aluminium (99.999%) elemental dopant. After evacuating (10^{-6} Torr) and sealing diffusion is carried out at 1230°C for 15-25 hours to obtain deep junctions at 50-90 μm depth and surface concentration of 10^{16} cm^{-3}. The wafers are then cooled at the rate of 1-3°C/m at the end of diffusion process.

Sample 4 : In this case aluminium deep diffused wafers (sample 3) are taken as the starting material. To this, gallium diffusion is carried out at 1230°C for 15-24 hrs similar to the process followed in the case of sample 3 for surface concentrations of 10^{18} cm^{-3} of gallium. Cooling is similar to the other samples.

Sample 5 : Here relatively new procedure compared to the above sample fabrication steps is followed. Aluminium and Boron are co-diffused in the NTD samples at 1230°C for 14 hrs. High pure aluminium foils are used as source for alumininum and for boron, heavily boron doped silicon wafers crushed into powder is used. Both of these are kept along with the silicon wafers in the evacuated quartz ampoule.

Sample 6 : These samples are prepared by diffusing aluminium and gallium under similar conditions followed in the case of Sample 3 and sample 4. But here the diffusions are carried out in the furnaces where the furnace quartz tubes are replaced by fresh quartz tubes.

Sample 7 : After diffusing aluminium and gallium under high vacuum (similar to sample 4), phosphorus is diffused at 1235°C for 10 hrs. Deposition of phosphorus is carried out in an open tube (Oxygen ambient) diffusion system. Nitrogen gas is bubbled through the phosphorus chloride ($POCl_3$) kept in a constant temperature (25°C) bath and makes bidirectional passes in the diffusion tube during the doping cycle.

Sample 8: These samples are prepared on the similar lines followed in the case of sample 7. Only difference between this and the previous one is the oxygen flow rate. In this case, the oxygen flow rate is increased to 100 lit/m from 10 lit/m during diffusion of phosphorus.

4.3 Sample preparation for DLTS :

For DLTS measurements, the sample should have a single junction. The original thyristor devices made (at M/S Bharat Heavy Electricals Limited, Bangalore, India) are having the structure of 'n^+-p-n-p-n^+' and are not suitable for conducting DLTS experiment as they are having more than one junction. Thus, the samples are lapped on both sides to remove thin n^+ layer first. The resulting p-n-p structured samples are further lapped on one side to remove p-layer, so that only one p-n junction remains. Mechanical lapping is done by using carborundum powder [Fig.4.1a].

As the background doping is very low (5.10^{13}-10^{14} cm^{-3}) in thyristors, comparatively large area diodes (p-n junctions) of the order of 3mm.3mm are cut from the big wafer and used for DLTS measurements. The diodes thus made are cleaned in an ultrasonic bath for 10 minutes and then in organic solvents such as trichloroethylene, acetone and methanol. Finally, the samples are cleaned with Transene-100 (a proprietary solution from Transene Co., USA). To remove native oxide layer on the surface the samples are dipped in hdrofluoric acid (48%) for about 10-15 seconds and then

thoroughly washed in deionised water. Finally the samples are treated in transene-100 and methanol. For ohmic contacts, the samples are coated with nickel by the process of electroless nickel plating as this gives very good ohmic contacts with silicon [18]. For this, the samples are heated at 80°C in ammonia free Nickelex solution (a proprietary of Nickelex coating solution from Transene Co., USA) for about 1 hour. The nickel coating on the edges of the sample are removed by dilute HNO_3 after covering the top and bottom by dental wax (which can dissolve in boiling trichloroethylene easily). To avoid excess leakage currents due to the rough edges, the edges are chemically polished with CP4 etchant. Since CP4 is a slow etchant, the samples are etched for about 1 hour for bright and good polishing. Finally, the samples are cleaned with organic solvents. The samples are then sintered in nitrogen ambient (from liquid source) at 450°C for about 15 minutes for good ohmic contact.

The samples thus prepared are mounted on a TO-5 header as shown in Fig.4.1b. The n-side of the sample is attached to the base of the header using silver epoxy. From the top of the sample (p-side) a gold wire is bonded using same epoxy. The second end of the wire is bonded to one of the posts on TO-5 header. Then the samples are cured at 120°C for 30 minutes. This is needed to harden the silver epoxy. The samples thus fixed on the TO-5 header are encapsulated by pressing the oval shaped cap of the header.

4.4 Results and discussion :

Capacitance-voltage, current-voltage, open circuit voltage decay (using Life Time Test Unit Type OCD-2B of Solid State Measurements, Inc.) and DLTS measurements are carried out for characterizing the defects and their effect on the minority carrier lifetime in thyristors.

Typical current-voltage (forward and reverse) characteristics are shown in Fig.4.2. The ideality factor for all the diodes is around 1.7, which is typical of almost all the p-n junction diodes fabricated in this way. Capacitance-voltage measurements are done to check the nature of the junction and also to measure the background concentration. Typical capacitance-voltage plot is shown in Fig.4.3. Reverse bias voltages upto 15 volts are applied. Linear dependence of $1/C^3$ on the reverse bias voltage region reveals the linear nature of the junction.

DLTS measurements are carried out for all the samples. Fig.4.4 show the DLTS spectra recorded for the samples 1 and 2 where, the process variable is the diffusion temperature only. DLTS plots of the samples 3,4 and 5, where the diffusions are done under vacuum is shown in Fig.4.5. Fig.4.6 shows the DLTS spectra recorded for the samples 6,7 and 8. The activation energy plots for the different levels observed are shown in Fig.4.7. Table 4.1 gives the activation energy and the density of the levels observed for different samples.

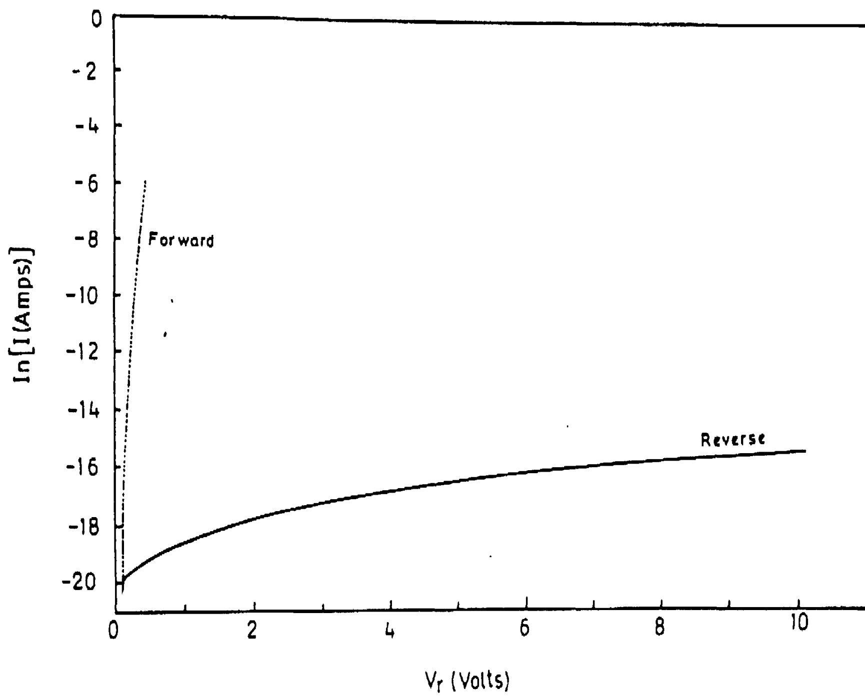


Fig.,4.2 Typical I-V plot of Al deep diffused thyrister grade silicon p-n junction.

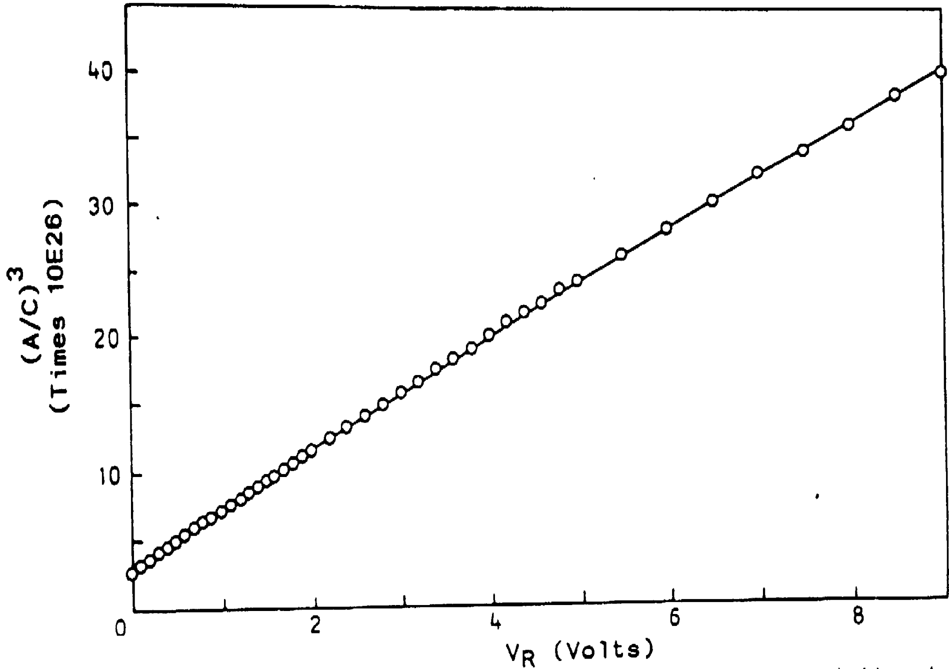


Fig.4.3 Typical C-V plot of Al deep diffused thyristor grade silicon p-n junction (linear junction).

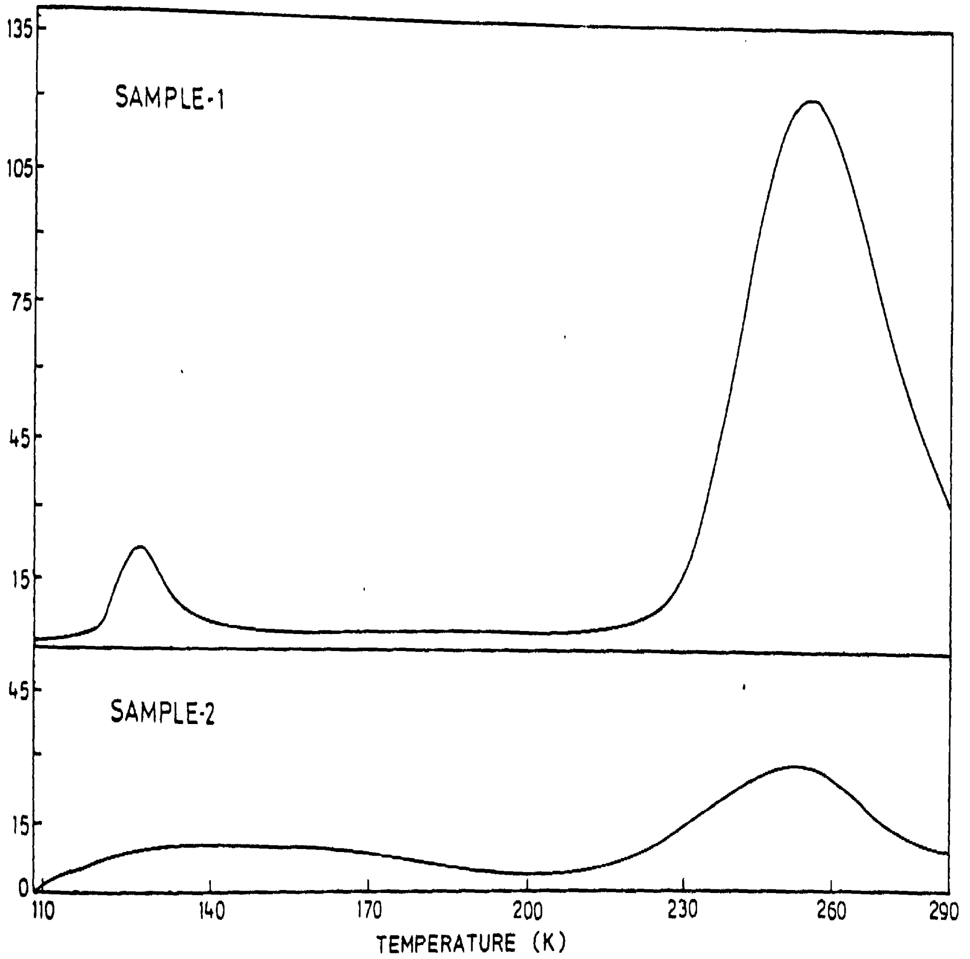


Fig.4.4 DLTS plots of Al deep diffused silicon (open tube diffusion) (a) at 1235°C (b) at 1190°C.

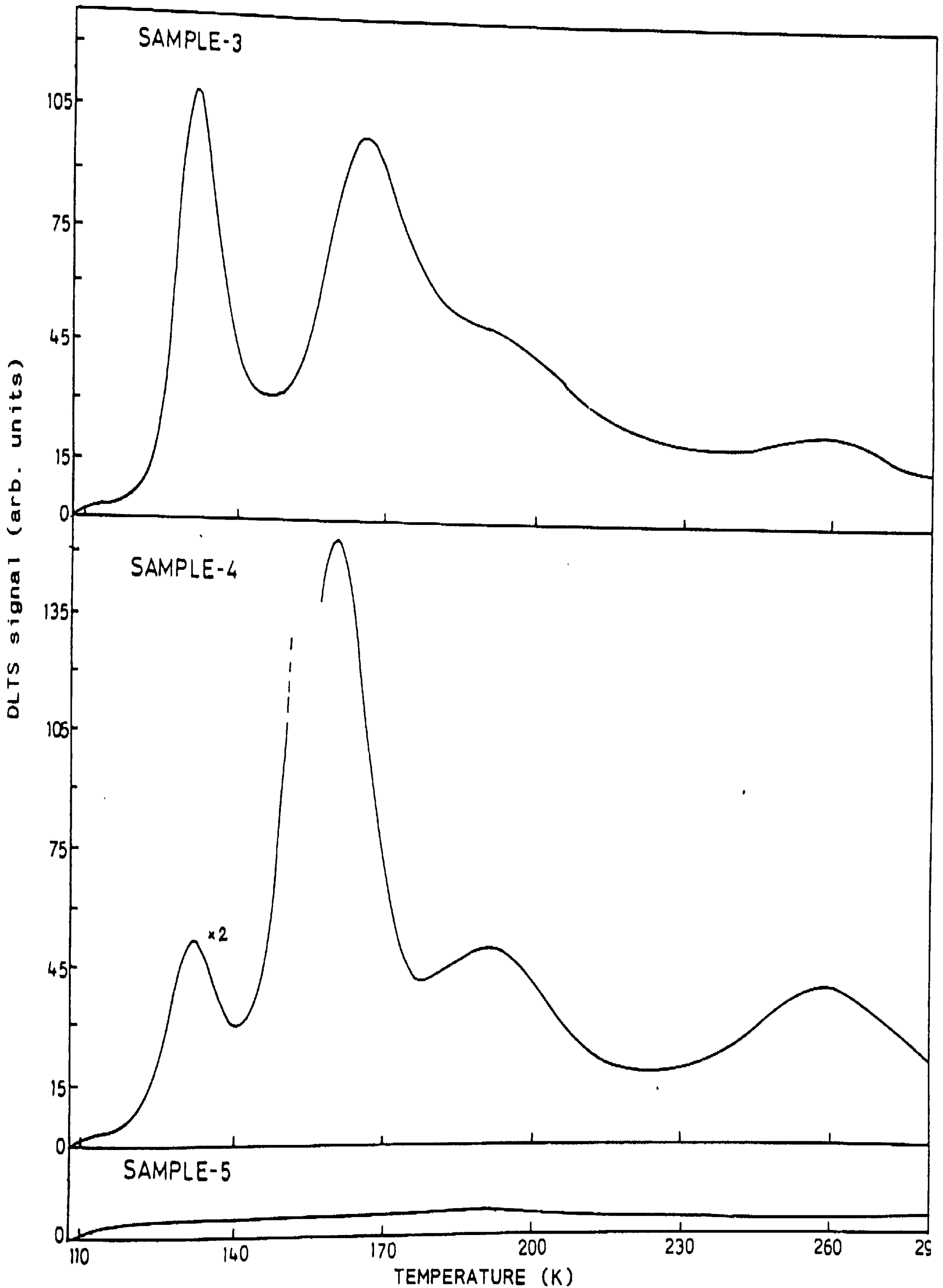
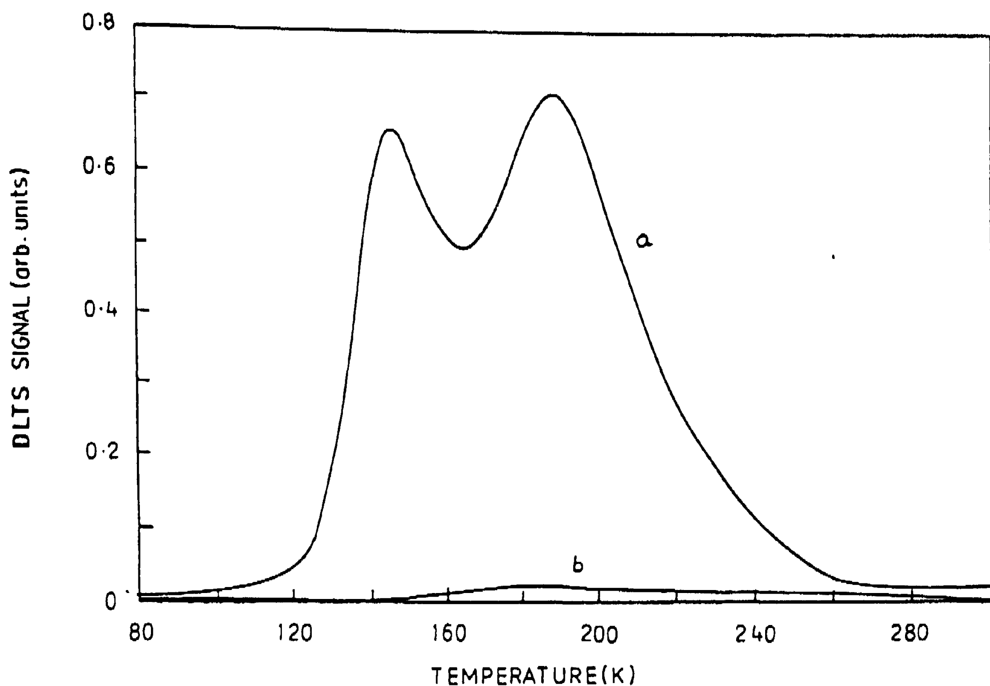


Fig.4.5 DLTS plots of Al deep diffused silicon (vacuum diffusion)
(a) Only Al diffused (b) Al and Ga diffused
(c) Al, Ga and Boron diffused



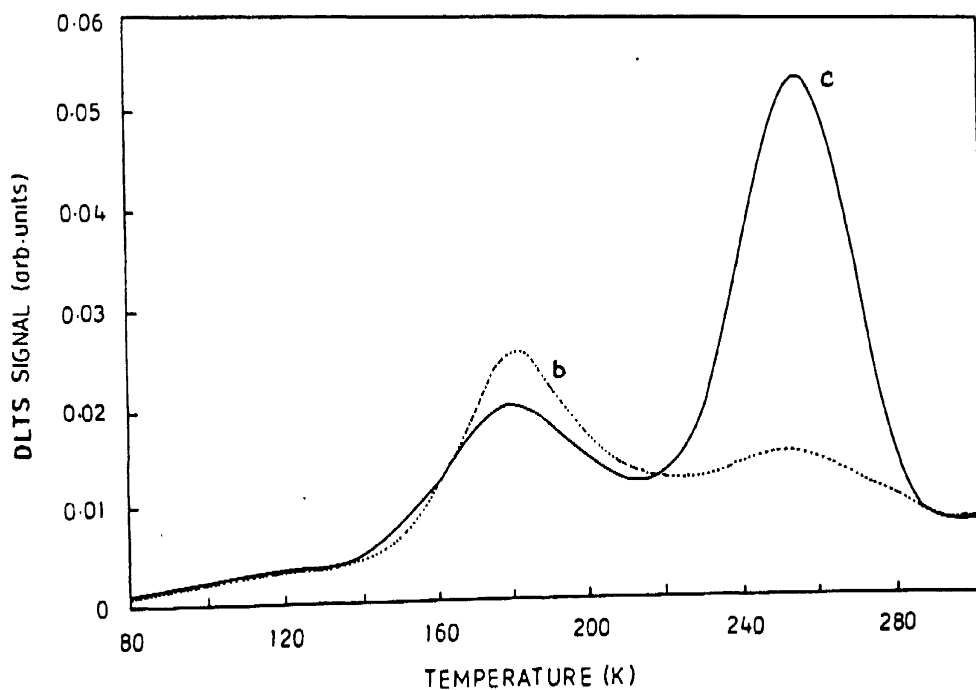
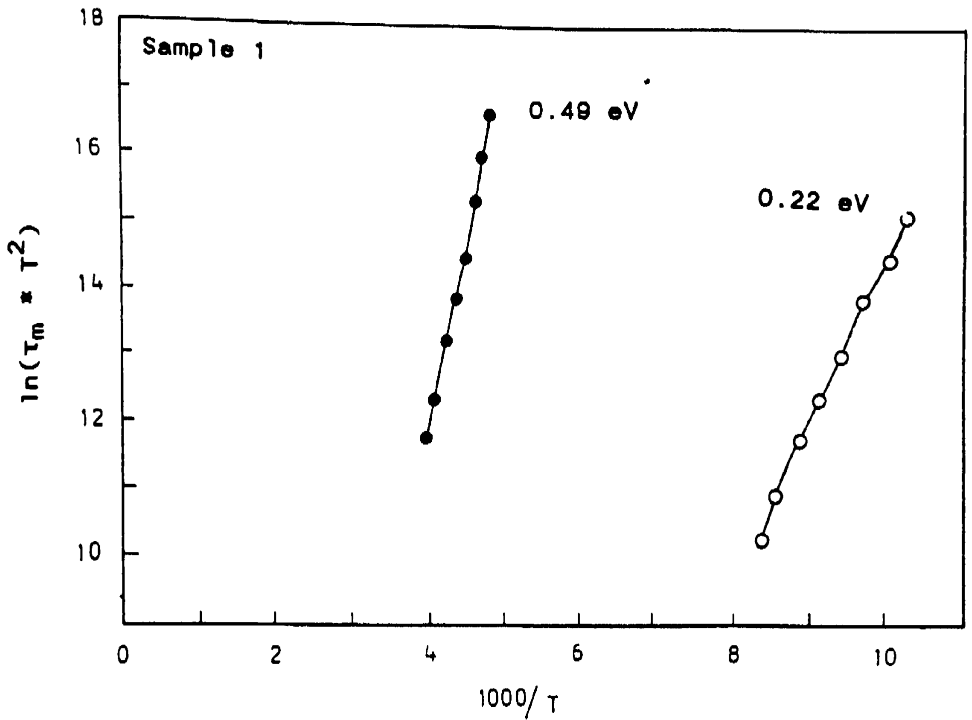


Fig.4.6 DLTS plots of (a) Al and Ga (vacuum) (b) Al,Ga and P (oxygen ambient) (b) Al,Ga and P (increased oxygen flow) diffused (fresh quartz ware used) Si diodes.



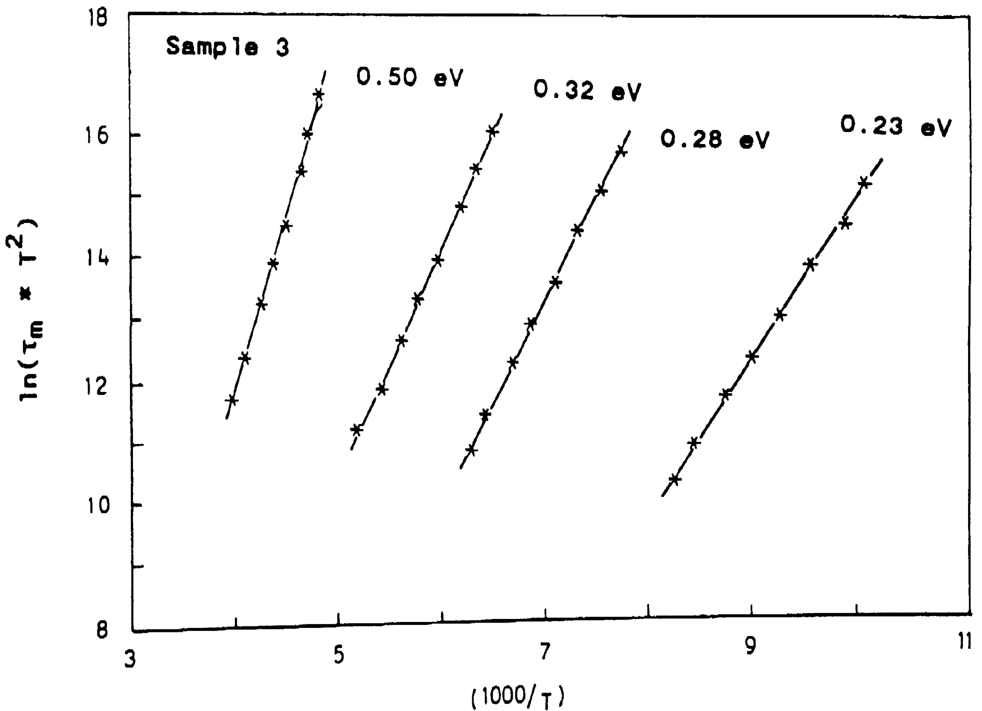


Fig.4.7 (a) Arrhenius plots of the deep level in sample 1
(b) Arrhenius plots of the deep level in sample 3

Table 4.1 : Activation energy, trap density and minority carrier lifetimes observed in differernt samples :

Activation Energy (eV) / Sample no.	0.22	0.23	0.28	0.32	0.49	0.50	Minority carrier lifetime μs
	Trap density (10^{11} cm^{-3})						
Sample 1	7.6	....	....	....	24	....	5.2
Sample 2	....	....	....	....	2.3	....	26.1
Sample 3	....	23	17	7.1	....	3.1	6.2
Sample 4	....	7.5	51	10	....	5.1	6.7
Sample 5	....	....	....	....	....	....	120.0
Sample 6	....	75	51	....	....	....	1.0
Sample 7	....	....	....	1.4 (peak1)		0.1	15.0
Sample 8	....	....	....	8.2 (peak1)		3.1	28.0

4.4.1 Effect of temperature on the deep level concentration :

It is clear from Fig.4.4 that the deep level concentration increases with temperature of diffusion. The concentration of deep levels observed in sample 1 are very large compared to sample 2. Sample 1 is diffused with Al at 1300°C and in sample 2 diffusion is carried out at 1190°C for 10 hrs under oxygen ambient. The only processing difference between sample 1 and sample 2 is the diffusion temperature. This is further confirmed by the increase in minority carrier lifetime.

It is well known that the minority carrier lifetime 'τ' depends on the concentration as well as capture cross section of the defect or impurity center significantly and can be written as

$$\tau = \frac{1}{\sigma V_{th} N_T}$$

Where σ is the capture cross-section of the deep level

V_{th} is the thermal velocity of the charge carriers and

N_T is the concentration of the deep level.

In the case where more than one deep level is present in the sample, depending on the capture cross-section and concentration, the level for which 'τ' is minimum will decide the device performance.

The minority carrier lifetime measured with OCVD in the case of sample 1 is 5 μs and it is 26.1 μs in the

case of sample 2. Concentration of the observed levels are given in Table 4.1. It can be seen good correlation existing between deep level concentration and minority carrier lifetime.

4.4.2 Effect of ambient on the deep level formation:

Diffusion of aluminium is carried out under vacuum and oxygen ambients separately. Fig.4.5 shows the DLTS plots of the samples 3,4 and 5. Comparing these plots with those in Fig.4.4 it is clear that the ambient under which the thermal treatments are carried out, affects very much on the deep level formation in silicon. In the case of sample 1, Al is diffused under oxygen ambient whereas in the case of sample 3 the diffusion is under vacuum. Sample 1 shows only two deep levels at 0.22 eV and 0.49 eV, whereas sample 3 is having four deep levels at 0.23 eV, 0.281 eV, 0.32 eV and 0.50 eV. It is clear from this result that the deep level (unintentional) introduction in silicon is influenced by the ambient under which diffusions are carried out. From these spectra, further it is observed that the concentration of dominant deep level in sample 1 is reduced significantly, under vacuum diffusion. However, vacuum diffusion causes formation of more deep levels. Minority carrier lifetimes observed in these cases are 5.2 µs and 6.2 µs. It seems, that the deep level 0.49 eV in sample 1 and the deep level 0.28 eV (corresponding to peak 2 in DLTS spectra of sample 3) are the dominant levels killing the minority carrier lifetime.

In the case of sample 4, where Ga was diffused at 1235°C for 12 hours (after Al diffusion under vacuum), the concentration of the observed deep levels are getting enhanced without any new levels as can be seen from Fig.4.5. The formation of deep levels due to impurity complexes seems to be more probable at high temperatures and long processing times.

4.4.3 Gettering effect of Boron on deep levels :

Our new method of co-diffusing of aluminium and boron resulted in excellent improvement in the minority carrier lifetime. In these samples, the lifetime of the minority carriers has been observed as 120 μs. The DLTS spectrum of the sample is quite flat indicating no deep levels, at least within the detection limit of the instrument (10^{10} cm^{-3}) (see Fig.4.5). All the DLTS spectra shown are for the same set of experimental parameters.

Sah et.al.,[3] discussed the gettering action of boron and phosphorus on the defects and impurity complexes. They have argued that the phosposilicate glass (PSG) or borosilicate glass (BSG) films on the surface reduce the defect density possibly by reducing the surface strain and disorder. Further, it was suggested that most of the metallic related defects are gettered by BSG and PSG [3]. Also, it is well known that most of the defects generated in silicon after high temperature long time treatment anneals out at temperatures around 450°C.

In the present case, all the measurements are done after annealing the samples at 450°C for 30 mnts. Based on this, and from gettering of all these deep levels by boron further indicates that these deep levels centers observed may be metallic related.

In all the high temperature long time processing steps, normally the source of contamination is the quartz ware and the furnace [13]. Since the impurity contamination is of the order of 1 PPM or less, it is suspected the quartz ware as the source of contamination which introduce these levels in silicon devices. In the following experiments quartz ware and furnace tubes are replaced with fresh ones. After replacing the quartz ware, the number of deep levels observed has been reduced to two only. Fig.4.6b shows the DLTS spectra recorded on the samples prepared under same experimental conditions, but with replaced quartz tubes. But there is no improvement in the minority carrier lifetime with these changes.

4.4.4 Gettering effect of phosphorus on the deep levels :

In the samples where Al and Ga diffusions are carried out in fresh quartz tube, only two deep levels are observed: 0.28 eV and 0.32 eV. On these samples, high concentration phosphorus layer was formed by phosphorus deposition [sample preparation discussed in the earlier section]. After drive-in diffusion of this phosphorus at 1235°C for 10 hrs, the deep level concentration has reduced substantially. DLTS spectra of the samples diffused with Al

and Ga, and Al,Ga and P are shown in Fig.4.6. In the later sample, a peak of small magnitude is observed at about 180 K. Its concentration is very low and we believe that this peak is a manifestation of peaks 1 and 1 in sample 6. These results reveal the gettering action of phosphorus on the deep levels. The improvement in the minority carrier lifetime from 1-2 μs (sample 6) to 15 μs after phosphorus diffusion is also in agreement with the DLTS results.

4.4.5 Effect of oxygen flow rate on the phosphorus gettering:

During the drive-in process of phosphorus, the samples are kept under flowing oxygen ambient. When the oxygen flow rate is increased during the drive-in cycle of phosphorus it is observed that the gettering effect is more pronounced and this resulted in increasing the minority carrier lifetime. When the oxygen flow rate is increased to 100 lit/min from 15 lit/min during the drive-in cycle, the minority carrier lifetime is increased to about 28 μs. The corresponding DLTS spectrum (Fig.4.6b) shows only a marginal decrease in the magnitude of the peak 1 while the peak 2 (0.50 eV) observed in the previous samples, reappeared with a small magnitude. The fabricated devices showed substantial increase in lifetime in the range 300 to 400 μs accompanied by an expected reduction in the forward voltage drop.

4.5 Identification of the deep levels :

We tried to identify the deep levels observed, based on the DLTS measurements. DLTS is an excellent tool for

identify very low concentrations of deep impurities effectively. It is essentially a relative measurement which compares with background doping. One can identify the deep levels with concentrations at least 1000 times smaller than the background doping. But unfortunately it can not identify the impurity i.e., DLTS is not defect specific technique. Because of this reason one has to intentionally dope the semiconductor with the expected impurity and cross check the results or choose other analytical technique to identify the elements. Suspecting platinum may be the contaminant (from DLTS results of 0.28 eV, 0.32 eV and 0.50 eV) we have intentionally diffused the platinum and identified its energy levels. These results are presented in chapter III. Based on these results, we may conclude that the peaks 2 and 3 (samples 3) with measured activation energy 0.28 eV, 0.32 eV in all the aluminium diffused (vacuum diffusion) samples may be due to platinum contamination.

Further, iron contamination is very common in silicon device processing [13,14,19,20] from different sources. The observed deep level with activation energy 0.50 eV may be due to iron contamination.

The exact identity of the impurity elements associated with the measured energy levels is difficult, because many elements exhibit overlapping energy levels in silicon [21]. In the present study, all the samples prepared are linearly graded junctions only. In such samples it is not

possible to identify whether the DLTS signal comes from the p-region of from the n-region of the junction. At the same time from the study of emission characteristics it is found that the impurity concentrations are of the order of 10^{11} to $10^{13}/cm^3$. With this very low concentration it is difficult to evaluate the impurities using SIMS or other analytical techniques or tools.

Rutherford Back Scattering (RBS) (done at The University of Western Ontario, department of Physics, London, Ontario, Canada, N6A, 3K7) is employed in the present case to identify the elements responsible for the deep levels observed. It is known that RBS is a defect specific technique i.e, it can identify the elements present in the material. Fig.4.8 shows the RBS profile taken on the sample 4 (where all the deep levels are observed in DLTS spectra). The RBS profile gives clear evidence of platinum and iron as major impurities in the sample. These results are in confirmation with that of the DLTS results.

The source of platinum is yet to be identified in the processing of sample preparation.

Based on the results obtained from DLTS and RBS, the DLTS peaks (2,3,4) observed (in sample 4) may be due to platinum and iron.

The low temperature peak (peak 1 in samples 1-4) observed may be due to the aluminium-oxygen complex. The possibility of this level being related to vacancies,

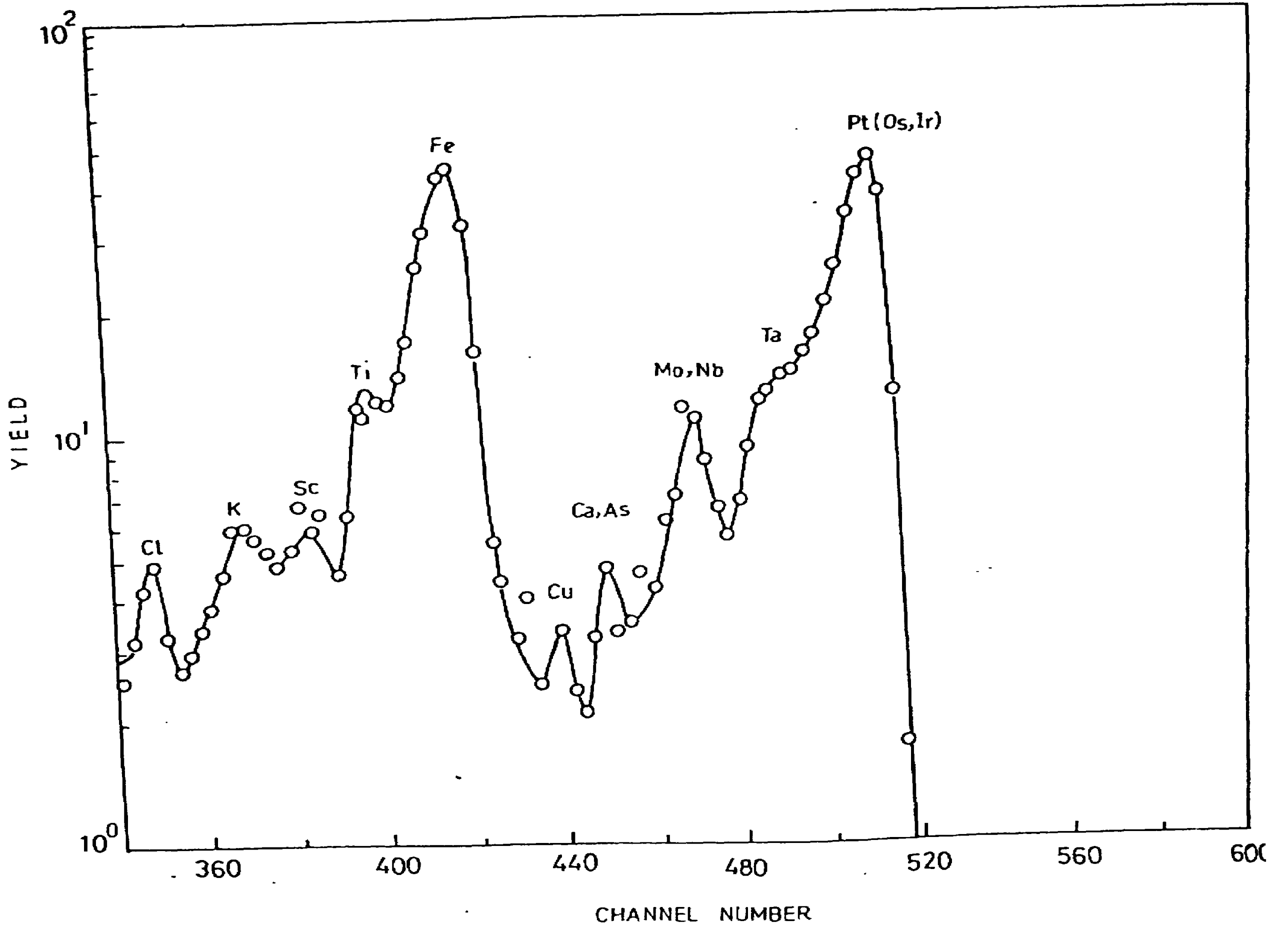


Fig.4.8 RBS profile of sample 3.

divacancies, Ali (interstitial aluminium) , V-Als (vacancy-substitutional aluminium), Als-Ali (substitutional and interstitial aluminium) is ruled out, because all these centers are not stable and annealed out at 400°C [7].

4.6 Conclusions :

When aluminium is deep diffused under oxygen ambient at 1300°C two deep levels are observed at 0.22 eV and 0.49 eV. Samples diffused with Al, Al and Ga in vacuum at 1238°C showed four deep levels at 0.23 eV, 0.28 eV, 0.32 eV and 0.50 eV. The minority carrier lifetimes in the above samples are 5.2 μs and 6.2 μs respectively.

Aluminium is co-diffused with boron under vacuum all the deep levels are disappeared. Due to this gettering action, the minority carrier lifetime is increased to 120 μs. Similar gettering action is observed when phosphorous is diffused in to the aluminium diffused samples. In this case the minority carrier lifetime increased to 28 μs.

Further, from the DLTS and RBS results it is found that the dominating defect levels observed may be due to platinum and iron contamination.

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