3.1. Initial development

Initially a microprocessor trainer kit - SDK 85 was taken to try out simple programs to light LEDs representing signals by scanning switches representing controls for the Signals. On board I/O chip '8155' was used for the purpose.

Later, the control of points and signals in a small passenger yard was simulated on a 'Cromemco' System III microcomputer which is based on Z80A microprocessor by using macro-assembler. The specifications of the system used are given in Appendix 7.

The points, signals and other gears are assigned bits in memory and the lighting of signals and setting of routes are simulated through software written in macro-assembly language the details of which are explained later. The signal lights simulated for some of the routes are also recorded through a printer. The route diagram and plan of the yard are shown in Fig.3.1. Software redundancy utilising redundant inputs is also simulated.
3.2 MODEL OF MICROPROCESSOR CONTROLLED SIGNALLING AND INTERLOCKING PHASEI

A part of a small scale model of a circular railway corresponding to a station has been operated by a dedicated microcomputer kit (MTA85-1) incorporating a microprocessor (8085). This kit had the following memory and I/O capability, hence expansion board was utilised:

1. 0000 to 07FF: monitor EPROM (2K bytes in 2716)
2. 2000 to 20FF: user RAM (256 bytes in 8155)
3. 2800 to 2FFF: user RAM (2K bytes in 2114 Nos)
4. I/O ports 21 to 23: user ports, in all 22 I/O lines in 8155.

The signals and points including the layout at the station called 'Sanketpuri' are shown in Fig.3.2 along with the controlling panel. For signals, LEDs (light emitting diodes) were used and for point operation solenoids were fitted which in turn were energised through relays driven from the peripheral chip. In the first phase described here approach locking and backlocking were not incorporated; only the point switch position was detected and not the position of the point at site. Also direct control of signals through switches is incorporated instead of the entrance/exit type with route setting. The block diagram of the hardware required for the interlocking project phase I is given in Fig.3.3. The software required running into about 1.3K bytes of object code is stored in EPROM (2716) on the
Down direction.

Switch 1 (turned right) and knob 'A' pressed — Route 1A.
Switch 1 (turned right) and Knob 'B' pressed — Route 1B.
Switch 2 (turned right) and Knob 'E' pressed — Route 2E.
Switch 3 (turned right) and Knob '£' pressed — Route 3E.
Switch 4 (turned right) and Knob 'T' pressed — Route 4F.

Switch 10 (turned left) and Knob 'C' pressed — Route 10C.
Switch 10 (turned left) and Knob 'D' pressed — Route 10D.
Switch 8 (turned left) and Knob 'H' pressed — Route 8H.
Switch 9 (turned left) and Knob 'H' pressed — Route 9H.
Switch 7 (turned left) and Knob 'G' pressed — Route 7G.

Up direction.

Switch 10 (turned left) and Knob 'C' pressed — Route 10C.
Switch 10 (turned left) and Knob 'D' pressed — Route 10D.
Switch 8 (turned left) and Knob 'H' pressed — Route 8H.
Switch 9 (turned left) and Knob 'H' pressed — Route 9H.
Switch 7 (turned left) and Knob 'G' pressed — Route 7G.

FIG. 3.1 - ROUTE DIAGRAM.
FIG. 3.2: LAYOUT & PANEL OF 'SANKETPURI' STATION (PHASE I)
FIG. 3.3: BLOCK DIAGRAM OF HARDWARE FOR SOLID STATE INTERLOCKING (PHASE-1)
expansion board. The switches on the control panel and the track circuit relay contacts are scanned through the three ports of '8155' chip of the main board. A port of the peripheral chip '8155' on the expansion board is also utilised for such inputs and the other ports of the two chips on expansion board are connected through transistor drive circuits to the signal LEDs and the LEDs on control panel. The point switches are connected directly to point solenoids through relays. The contacts of point switches are only connected to the I/O ports. The I/O port map and the details of drive circuits are given in Figures 3.4, 3.5 and 3.6.

The hardware configuration for the suggested error-detection method is given in Fig. 3.7. The output on bit 0 of port B of 8155(chip 2) of expansion board is connected through an opto-isolator to bit 4 of port A of 8155(Chip 1). The opto-isolator used is MCT2-822. The output on this line from port B of chip 2 was programmed by software to be a square wave of a large period of 1 sec. and was read by the port A of chip 1. Any erroneous reading of this output is programmed to feed a high level through PB of chip 2 (8155) to the interrupt controller(8259). As soon as the interrupt request is received the processor fetches the interrupt service program which switches on all the red LEDs of the signals. In this experiment, only one interrupt
FIG. 3.4: I/O PORT MAP (PHASE I)
FIG. 3.5: DRIVE CIRCUIT (LEDS)

FIG. 3.6: DRIVE CIRCUIT (RELAYS)
FIG. 3.7: HARDWARE FOR ERROR DETECTION.
request was connected to the controller as shown in the figure.

3.3. MODEL OF MICROPROCESSOR CONTROLLED SIGNALLING & INTERLOCKING - PHASE-II

The earlier station 'Sanketpuri' has been taken for control of signalling and interlocking with the entrance-exit type of control with approach locking and back-locking similar to a small passenger yard provided with route-relay interlocking. The layout of the yard with entrance-exit i.e. switch and push button controls and the altered control panel is shown in Fig.3.8. A separate expansion board has been fabricated and the block diagram of the main board and expansion board is in Fig. 3.9. As usual LEDs have been used for signals and point operation is by solenoids energised through polarised relays which are in turn driven through peripheral chips. The contacts of the polarised relays are detected in this phase. For setting a route a switch is turned either left or right at the entrance and a push button is pressed at the exit. If the route is set and locked, the track is free, the train signalled has arrived and the earlier signals have been put back to danger, the permissive aspect of signal i.e. yellow or green is switched on; the route setting is indicated by the lighting of white LEDs along the track. The route is not released till the train has traversed the assigned path and if a train has approached the signal but has not traversed the assigned
FIG. 3.8: LAYOUT & PANEL OF 'SANKETPUR' STATION (PHASE II)
FIG. 3.9. BLOCK DIAGRAM OF HARDWARE FOR SOLID STATE INTERLOCKING (PHASE II)
path, the route can be released and another route set, only after a lapse of a certain time interval either 120 sec. or 60 sec. depending on whether it is a home signal or a loop line starter signal etc.

The software required for this phase running into about 7.5 k.bytes is stored in 4 Nos. EPROMS (2716) on the expansion board. Five peripheral chips (8255) and one RAM+I/O chip (8155) on the expansion board have been utilised to scan the switches and push buttons on control panel, the track circuit relay contacts or switches in lieu used to simulate the point switch positions and the polarised relay contacts corresponding to the position of points as the point positions are not detected directly as done in real working conditions. The relay coils, signal LEDs and track LEDs are also driven through these peripheral chips. The counter/timer chip 8253 is used to set timings needed for approach locking namely 120 sec. and 60 sec. The interrupt controller (8259) chip is utilised for the same purpose as given in Phase I. The two chips 74LS138 are located on the expansion board to enable chip selection by memory and I/O mapping as appropriate. The chip 7404 is fixed to supply inverted address bit A15 required for decoding addresses for chip selection. The I/O port map for Phase II is given in Fig.3.10. The drive circuits are similar to those shown in Fig. 3.5 and 3.6.
FIG. 3.10: I/O PORT MAP (PHASE II)
FIG. 3.10: I/O PORT MAP (PHASE II) (Contd.)
NOs. IN BRACKETS DENOTE PIN NOs.

FIG. 3.11: TIMER CONNECTIONS

TO PA_0 OF PORT 88/8255 (CHIP 2) ON BOARD.

NOs. IN BRACKETS DENOTE PIN NOs.
The timer output of 8155 which is a square wave is fed to the clock of counter 1 of 8253 and the output is connected through the outlet to PA of port 88 of 8255(2). The gate of counter 1 is connected permanently to +5v. The connections are illustrated in Fig. 3.11.

Photographs of the model of signalling and interlocking are in Figures 3.12, 3.13 and 3.14.

3.4. Summary

A model for microprocessor control of signals and points has been described. The incorporation of approach locking and back-locking essential for route interlocking and the hardware for various timings has been detailed. The model has been working continuously for more than a year and is suitable for adoption in the field with suitable modifications.
FIG. 3.12. CONTROL PANEL

FIG. 3.13. CONTROL EQPT INCLUDING PCBs AND RELAYS
FIG 3.14. MODEL OF STATION 'SANKETPURI'