CHAPTER 5

CONCLUSIONS

5.1 SUMMARY OF THE INVESTIGATIONS

In this thesis, an attempt has been made to present a method which will reduce the complexity of testing of 2-D polynomials for stability. The algebraic method available now in the literature (Huang, 1981) is not efficient particularly when $N \geq 4$. This is because of the complexity involved in the computations and also the inaccuracies that creep in a big way because of the finite precision involved in the computers. So whenever the degree of the polynomial $N$ is large, numerical methods like row and column algorithm or row and column concatenation algorithm are more practical and so they are recommended. Even these methods do not assure (in some cases) that the polynomial has no zeros on the unit bi-circle $T^2$. So these methods to a large extent test only the necessary condition for the existence of zeros on $T^2$. They are not exact enough to test for sufficiency. This is so because in the case of row and column concatenation test one has to test infinite number of 1-D polynomials for root distribution to be sufficient.

In this thesis the row and column concatenation method is simplified and applied to reduce the number of 1-D polynomials to be tested for root distribution to one and also to check if the given first quadrant 2-D polynomial is devoid of zeros on the unit bi-circle $T^2$. The method presented tests stability for
both necessary and sufficient conditions and reduces complexity of testing when compared to all the available methods and is more accurate.

This thesis proposes a new SOC folded architecture for 2-D IIR filtering applications. Proposed folded architecture reduces drastically the number of processing elements in comparison to Global Speed Up Architecture discussed by Zhang et al (1990). In synthesizing system on chip architectures, it is important to minimize the design area by reducing the number of functional units. Signed sixteen bit fixed point and thirty-two bit floating point high speed folded architecture are designed for two dimensional recursive filter applications resulting in minimizing silicon area and maintaining the same throughput rate of one pixel per clock period.

The thesis also deals with VLSI design and simulation of fast eight bit and sixteen-bit microcontroller based system on chip for real time filtering applications and is simulated. In the SOC architecture the proposed folded architecture is combined with microcontroller to make it more useful for different applications. Because of pipelining and parallel processing features each instruction takes one clock period for execution. Control signals for folded architecture is generated in the Harvard architecture of RISC processor. The folded architecture has seven column processors that are capable of handling forty-nine pixels in forty-nine clock periods. The core has been designed using Verilog as HDL with Xilinx XC2S300E Spartan family as target FPGA device. Waveform of functional simulation of core confirms the micro-controller's capability of having throughput rate of one pixel per clock period. Due to parallelism multiple outputs are computed in parallel for a clock period. Therefore the level of parallelism increases effective sampling speed. Critical
path has been reduced due to pipelining which can be exploited to reduce power consumption.

5.2 PROBLEMS FOR FURTHER INVESTIGATIONS

Stabilization of an unstable 2-D recursive filter can be investigated along the lines of Chapter 2 though many methods are available in literature. ASIC implementation of the cores designed in chapter 3,4 can be worked on for further investigation.