Chapter 2

Literature Review

2.1 Motivation

As various wireless communication systems emerge, average consumers want smaller and lower price mobile sets. A lot of research efforts have been dedicated to make standard CMOS technology applicate to System-on-Chip configuration (SoC). SoC is highly wanted by wireless Industry since it reduces the area of transceiver and price of product. For Integrated circuit technology(IC) integrating all analog circuitry on a single chip is very difficult. High frequency filters are still realized with discrete components in wireless communication systems because the required selectivity is infeasible with current integrated circuit (IC) technology. These discrete filters are not only expensive but are increasing the loss in the receiver chain.

To increase the integration rate of the analog circuitry, the use of discrete filters must be minimized; so as to achieve such goal minimum number of high frequency filters should be used. Number of external components and problem of power consumption can create major impact in radio architecture design [30]. Among so many types of receiver architecture available, the number discrete filter can be reduced and integration of analog filter is easy but other problems may arise. For example in direct conversion architecture channel selection is done at base band level(RF to direct baseband) with all intermediate frequency(IF) filters are eliminated, but this direct conversion architecture is susceptible to DC offset and flicker noise.

In low frequency, the integration of analog filter is feasible because the required selectivity is low but many difficulties arise in such integration because of limited

dynamic range (DR) and unwanted variation. Most low frequency range filters are based on operational amplifier (Op-amp) or operational transconductance amplifier (OTA). Since the active components are only linear in certain frequencies and signal range, there is a problem of dynamic range and linearity of filter with the use of active components. Tuning circuits must be used to compensate the frequency shift because integrated filter are sensitive to process and temperature variations. The tuning circuits sometimes affect the dynamic range (DR).

As wireless communication systems are required to process high data rate signals, baseband analog filters must have wide bandwidths, while maintaining high linearity, low noise, and low power consumption. In wide bandwidth system, it is not easy to achieve high linearity and low noise with low power consumption since linearity and integrated noise are increased with power consumption and bandwidth respectively. As the bandwidth increases, design of baseband filter is more complicated. Wide bandwidth filters are only possible when the active component achieves wide gain bandwidth, high linearity, and low noise.

The motivation of this thesis is to investigate and propose simple and robust CMOS Continuous time filter for Dual-band receivers. The analog continuous filter is essential block in the wireless communication system.

2.2 Analog Baseband Filter in Wireless Communication

Analog baseband filters can be divided into two different kinds: sampled data filters and continuous time filters. Sampled data filters are accurate and not sensitive to process variation. Because of the high clock frequency and settling time requirement of the amplifier, sampled data filters are not used in wideband signal processing. In contrast, continuous time filters are widely used in wideband signal processing, but they are very sensitive to process and temperature variations. The design and performance of continuous time filter is the main bottleneck in improving the performance of receiver

[31]. Due to problem of frequency variation, mismatch, and phase error in the baseband filter, performance of receiver is often limited

Nowadays, wireless communication systems are required to process not only high data rates but also multi-standard information. The reason for this is that second generation and third generation cellular phones or WLAN and Bluetooth will coexist for some time [32]. This implies that the filter in the receiver must have wideband cut-off frequency and multi-standard capability. High gain bandwidth is usually achieved at the expense of high current consumption, which is the main reason for the increase of power consumption in the filter. Multi-standard capability is usually obtained with parallel connection of passive components with switches. Since the bandwidth of different standard is determined by digital signal processor (DSP), programmable switches must be implemented to change the bandwidth.

There are still many problems in achieving wideband continuous time filter. Linearity is the main problem because desired signals are blocked in wideband filter due to inter-modulation products of two in-band signals. Parasitic near the cut-off frequency degrades the linearity and also increases the time constant of the filter. Since the size of passive components used in the filter is getting smaller as the filter bandwidth increases, mismatch or process variation of the passive components is more critical to the variation of the filter's time constant. Therefore, integration of wideband filter requires additional time for post design tuning.

2.3 Channel Select Filtering and Tradeoffs

The filter circuit used in any application can be of three different types depending on the type of signals handled. The general types of filters used in most applications are digital filters, continuous-time filters (Analog) and sampled-data filters.

2.3.1 Digital Filters

A digital filter [33] uses a digital processor to perform numerical calculations on sampled values of the signal. The processor may be a general-purpose computer such as a PC, or a specialized DSP chip. The analog input signal must first be sampled and digitized using an ADC. The resulting binary numbers, representing successive sampled values of the input signal, are transferred to the processor, which carries out numerical calculations on them. These calculations typically involve multiplying the input values by constants and adding the products together. If necessary, the results of these calculations, which now represent sampled values of the filtered signal, are output through a DAC (digital to analog converter) to convert the signal back to analog form. In a digital filter, instead of voltage or current sequence of numbers represent signal. Such setup of basic digital filtering process as shown in Figure 2.1 that combines the anti-aliasing filter and ADC together and the reconstruction filter with DAC to focus more on the digital filtering block.

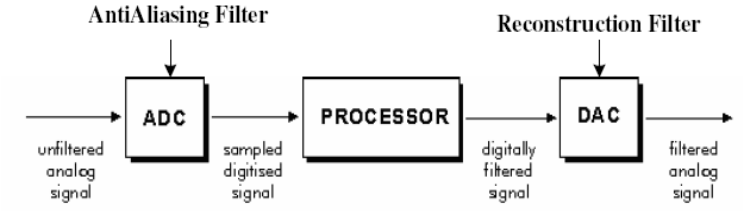


Figure 2.1 Digital Filtering Processes

2.3.2 Sampled-Data Filters

Sampled-data filters do not work with the digital representation of the signal samples, but operate on samples of the signal. Both the digital filters and sampled data filters are discontinuous in time but continuous in processed data value. Both the digital and sampled data filter are characterized in Z-domain. The best-known example of such an approach is that of switched-capacitor (SC) filters. An SC filter is a continuous-amplitude, sampled-data system. This means that the amplitude of the signals can assume any value within the possible range in a continuous manner. On the other hand, these values are assumed at certain time instants and then they are held for the entire sampling period. Thus, the resulting waveforms are not continuous in time but look like a staircase. Figure 2.2 describes how an input continuous time signal can be sampled. The sampling

operation extracts from the continuous-time waveform the values of the input signal at the instant *n·Ts (n = 1,2,3, …),* where *Ts* is the sampling period *(Ts = 1/Fs).*

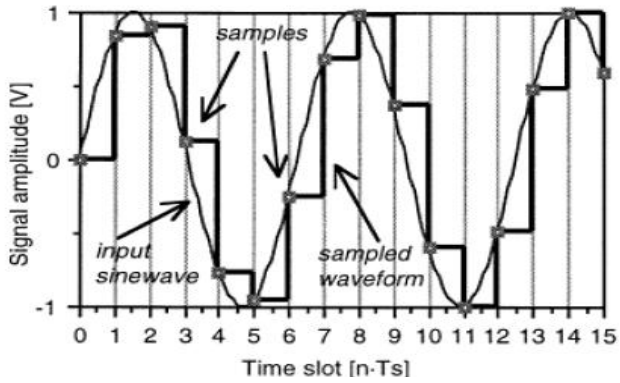


Figure 2.2 Sampling of Continuous Time Signal

The switched capacitor filter can be used in an application [34]-[35] similar to those shown in Figure 2.1 and Figure 2.2. Figure. 2.3 show the usage of SC filter in the standard application example. Due to the sampling operation involved, continuous-time (CT) anti-aliasing filter and reconstruction (smoothing) filter are requiring switched-capacitor systems.

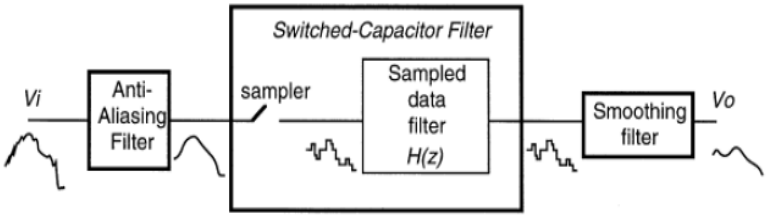


Figure 2.3: A Switch Capacitor Filter Application

2.3.3 Continuous Time Filters

An analog filter is any filter, which operates on continuous-time signals. In particular, Linear Time Invariant (LTI) analog filters can be characterized by their (continuous) differential equation. Instead of a difference equation as in digital and SC filters, analog filters are described by a differential equation. Instead of using the *z* transform to compute the transfer function, CT systems use the Laplace transform. In the real world, analog filters are usually electrical models, or ‘‘analogues", of mechanical systems

working in continuous time. If the physical system is linear and time-invariant (LTI) (e.g. consisting of elastic springs and masses which are constant over time), an LTI analog filter can be used to model it. Before the widespread use of digital computers, physical systems were simulated on so-called ``analog computers." An analog computer was much like an analog synthesizer providing modular building blocks (``integrators") that could be patched together to build models of dynamic systems.

Filters can be also be categorized according to the relative size (depending on the frequency of operation) of the elements used with respect to the wavelength of the signal into two categories: Distributed [36] and Non-distributed filters. In a non-distributed [37] (lumped) filter, the physical dimensions of the used elements (resistance, inductance, or capacitance) are negligible compared to the wavelength of the fields associated with the signal. Thus they are simple elements concentrated within the boundaries of the corresponding physical element. This is in contrast to the distributed filter, in which the physical elements have dimensions comparable to the wavelength of the fields associated with the signal and hence it is represented by a combination of physical elements.

2.3.3.1 Continuous Time Analog Filters

The main focus of this research is the design issues of continuous-time integrated filters. High frequency continuous-time filters have been widely used in various applications, in cases where high speed and low power dissipation are needed. Those applications include video signal processing [38], hard-disk drive read channels [39], loop filters for phase-locked loops [40], and radio frequency wireless communication systems [41]. The low frequency applications are in the bio-medical applications [42] like Hearing-aid and also for seismic systems [43].

Digital filter is not feasible for high frequency applications because they are very power hungry at high frequencies, i.e., $power = f_{clock} V_{DD}^2 / 2$. Although switched capacitor filters can have good linearity and dynamic range properties, they are not suitable because of their limited ability to process high frequency signals due to the sampling operation. The

sampling frequency should be chosen larger than the filter bandwidth to avoid inaccurate filter frequency response. That requires the use of operational amplifiers (Op-Amps) with very wide bandwidths,to provide proper settling, demanding large currents; it is required that the unity gain frequency of the used operational amplifier be at least five times larger than the clock frequency used. Another bottleneck is the inability of real switches to operate at high frequency and at low voltages. Thus continuous-time filters become the only option in these types of applications. Continuous-time filters are divided into two main categories: Passive filters and Active filters. All the components of passive filter are passive. Therefore, a passive filter may include among its elements resistors, capacitors, inductors and transformers. If the elements of the filter include amplifiers or negative resistances, this is called active.

2.4 Receiver Architecture

Earlier radio receiver cannot utilize frequency translation because they detected signals directly from radio frequency (RF), however such signal detection is not possible in modern radio receiver. Because the modulation schemes are used to deliver information effectively, a radio receiver must select a certain frequency band and translate the band to another frequency to detect the transmitted information [44]. Modern communication system is designed for efficient use of radio bandwidth. Received signal may contain adjacent channels, which have higher level of power than desired channel.

As an example, Figure 2.4 shows the GSM specification for the possible power levels of the nearby channels as a function of frequency offset. If the adjacent channel which is 600 kHz offset from the desired channel must be attenuated by 10 dB below the desired channel to detect the information, the adjacent channel must be attenuated by 65 dB according to the Figure 2.4. Since the desired channel is -98 dBm, the power of adjacent channel, -43 dBm, should be attenuated to -108 dBm. In the case of GSM, the desired channel has a bandwidth of 200 KHz with center frequency 900 MHz; the required filter must have a quality factor (Q):

$$Q = \frac{900MHz}{200KHz} = 4500$$

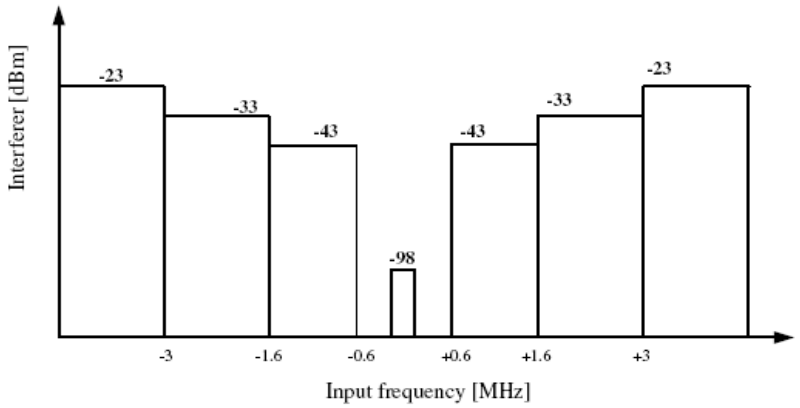


Figure 2.4 Power Level of different channel

This is not possible to realize with current technology [44]. The solution for this problem is to translate the frequency to lower or zero frequency for easier detection with feasible filters. In modern receivers, detection of information is usually done in low IF or zero IF. The analog filters in low IF or zero IF separate the desired channel from unwanted ones and surrounding interferers, which may be orders of larger than the desired signal. Accomplishing the same job without analog filters would require analog to digital converters (ADCs) with much larger number of bits to properly digitize and process large interferers [31]. Therefore, analog baseband filters are needed for the proper detection of the desired signal in radio receivers [45].

Analog channel selection filter's specifications are highly affected by receiver architecture. Therefore, it is important to understand the requirements of receiver architectures for the effective design of analog filters.

2.4.1 Superheterodyne receiver

A superheterodyne receiver removes the image component by filtering before each down conversion stage [46]. When the radio frequency(RF) signal is down converted to a non-zero intermediate frequency(IF), the image component which is at the same frequency offset from the local oscillator(LO) as the desired RF signal, but on the other side of the LO, is mixed to the same IF(Intermediate Frequency) as the desired signal. Before frequency translation, image frequency must attenuate by image rejection filter otherwise from desired signal, image frequency component cannot remove.

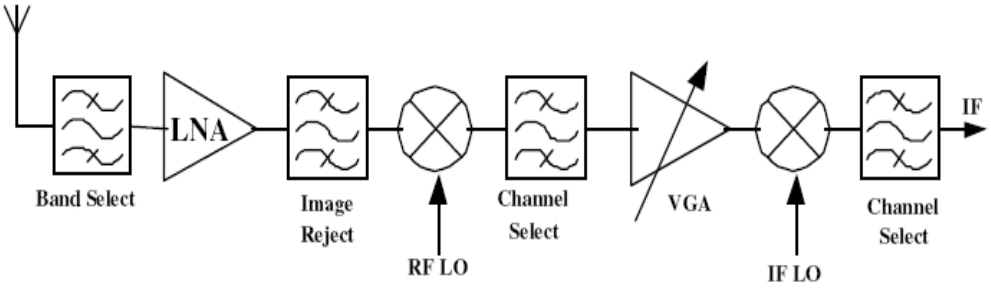


Figure 2.5 Superhetrodyne Receiver

First, a passive off-chip pre-select filter attenuates the signal outside the desired system band [47]. This filter suppresses out-of-band signals and thus reduces the dynamic range requirements of the next stages. It is desirable to suppress out-of-band signals as much as possible, but there is a tradeoff between stop band attenuation and pass band insertion loss [48]. The insertion loss of this filter is important because it directly adds to the receiver noise Figure. Usually, the band select filter is realized as a ceramic or a surface acoustic wave (SAW) filter. Above 1GHz, Ceramic filters are often preferred because of less insertion loss [48]. A low noise amplifier follows the preselect filter. The low noise amplifier (LNA) input must be matched to a specified impedance level, typically 50Ω, since the impedance matching is part of the preselect filter [47]. After the LNA, mixer converts the desired channel to a fixed IF.

The first IF frequency must be chosen carefully to allow the image at any possible LO frequency to lie outside the system band and to be attenuated enough by the pre-selection filter [44]. The first IF in a superheterodyne receiver must be given as:

$$f_{IF1} > \frac{B}{2}$$

----------(2.1)

where B indicate the bandwidth of the pre-selection filter. A high intermediate frequency relaxes the requirements on the preceding filter, but places higher demands on the circuitry of the subsequent IF stage. If the received radio frequency is very high when compared to the available filter technologies, it might be impossible to filter the signal. Such problem can be overcome by filtering and down converting several times. The number of down conversions depends on the frequency planning and on the selectivity of the filters. However, every down converting generates a new image frequency which must be rejected before the mixing, and the successive stages usually add a lot of noise which significantly impact on the dynamic range of the receiver.

After the down-conversion mixer, a passive off-chip channel-select filter attenuates the adjacent signals to a sufficiently low level. Therefore, the linearity requirements of the subsequent stages are drastically decreased. The first IF is typically between 30MHz and 100MHz [47]. The selection of the IF requires a trade-off. If a high IF is chosen, a less selective image-reject filter is sufficient at RF, but the required selectivity of the IF channel-select filter is increased. On the other hand, if a low IF is selected, the requirements for the channel-select filters are relaxed at the expense of tighter specifications for the RF filters. In most applications, the channel select filters cannot be implemented on chip with active components [47]. Therefore, power consumption is increased because input and output of the channel select filter should be matched to low impedance level. The channel-select filtering is usually divided between one or more IF filters and analog or digital base band filters. A variable-gain amplifier (VGA) decreases the dynamic range requirements of the following stages. After the first IF, the signal can be down converted to another IF or to DC using quadrature down conversion. The signal may also be sampled and digitized if the IF is sufficiently low. More than one IF can be used to divide the channel-select filtering and amplification between several stages.

The superheterodyne receiver architecture has dominated the field for decades since it offers an excellent performance [44]. The excellent sensitivity and selectivity come from the use of passive, highly linear off-chip filters. These filters provide a sufficient image rejection and selectivity at IF. The problems related to DC offsets and flicker noise can be avoided since the signal can be processed at an IF far from DC.

2.4.2 Direct Conversion Receiver

A direct conversion receiver converts the carrier of the desired channel to the zero frequency directly [46]. The direct conversion receiver is an alternative solution to the image rejection problem. The intermediate frequency is moved to DC making the desired channel an image of itself. Consequently, no image rejection filter is needed prior to mixing. Compared to superhetrodyne receiver, the direct conversion receiver implements external IF filters. The IF stages and the passive IF filters are eliminated so that the integrability of the direct conversion receiver is much higher than the super heterodyne. Furthermore, the direct conversion receiver is suitable for the multi-mode receivers since the bandwidth of the integrated low pass filters can be designed programmable. Figure 2.6 shows the schematic of the direct conversion receiver architecture.

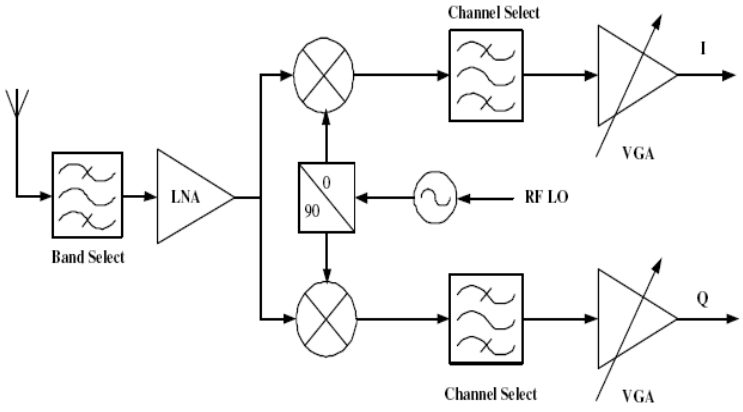


Figure 2.6 Direct Conversion Receiver

Two down conversion mixers must be used for demodulation at RF if a signal with quadrature modulation is received [46]. The pre-select filter is used to attenuate out of band signals before the LNA. Since there is no problem with image signal in the direct conversion receiver because the off-chip filter between LNA and mixer is not required.

Therefore, the output of the LNA drives on-chip load so that only input matching in the LNA is required. Also, a low pass filter with a bandwidth of half the symbol rate is suitable for channel selection and it can be implemented with an active on-chip filter [46].

The most serious problem of the direct conversion receiver after the down conversion stage is that of DC and time varying offset voltages [46-48]. Since the down converted band extends to zero frequency, static and time varying offset voltages can corrupt the signal [47-48]. The dc offset must be minimized to avoid the signal saturation. Even though automatic gain control can prevent the saturation of the incoming signal, the amplification will be very small. In such cases detection of a weak signal will be very difficult. If the offset is not removed, the DC offset component can be considered as in-band interferer.

One source of offset voltage involves transistor mismatches in the down converter and following baseband stages [48]. Such kind of offset voltage is constant and other dc offsets from the self-mixing of the local oscillator signal. This is caused by the leakage of local oscillator signal to the input of the mixers, which mixes with itself and produce a constant dc offset [48]. If local oscillator leak directly to the RF port of the mixers or to the input of LNA, the dc offset problem will be more serious [47-48]. The leaked local oscillator signal can also propagate to antenna because of the finite reverse isolation of the LNA and pre-selection filter and reflect back from the interfaces having mismatch. If the local oscillator radiates from the antenna and reflects from other objects back to the receiver, the offset due to self-mixing varies in time [47-48]. Figure 2.7 shows two cases of self mixing.

In case of Figure 2.7 (a) the local oscillator is mixed with itself, produce an offset voltage at the output of the down converter. This voltage is typically orders of magnitude larger than the desired signal, and if not removed, will cause saturation in subsequent stages [48]. As the antenna surroundings change over time and as leakage local oscillator reflect

from nearby moving objects, the local oscillator signal at the RF port of the down converter may vary with time and generate time varying offset voltage [48].

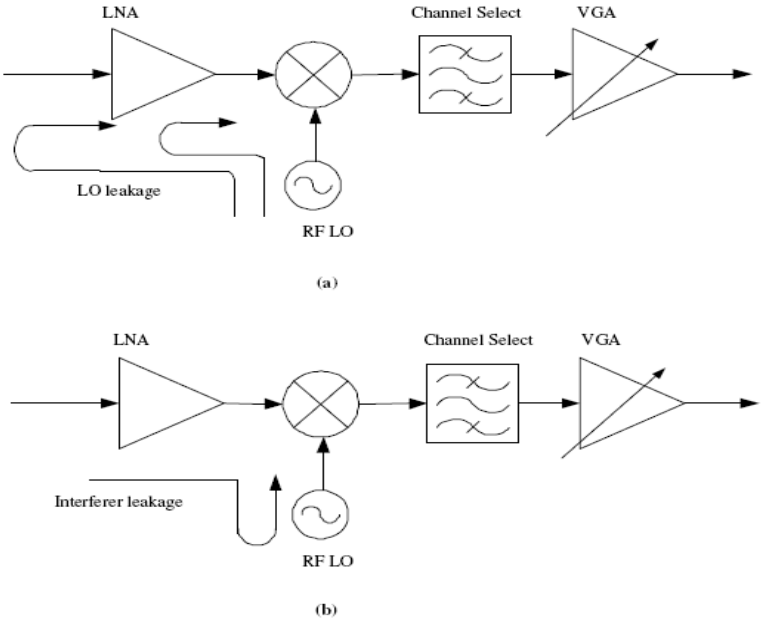


Figure 2.7 Two Different cases of Self Mixing

The other source of time varying offset voltage is self-mixing of a strong interfering signal as shown in Figure 2.7 (b). For example, the leakage signal from the transmitter itself mixed and creates a distorted signal at the baseband. This distorted signal will vary with time due to both the amplitude modulation of the transmitted signal and due to the power control in the up-link [47-48].

With better circuit design, magnitude of offset voltage can be reduced. Implementation of high pass filter or DC servo loop can remove the dc offset. However since the substantial information is contained at low frequency, the cutoff frequency of the high pass filter must be very low. This means that the capacitor in high pass filter must be very large.
Then the settling time of the filter will be slow that the high pass filter cannot remove the fast time varying dc offsets. The absence of passive IF filters places very stringent requirements on the active baseband filters. Both the linearity and the noise must be much lower than in a superheterodyne receiver as there is no significant amount of filtering or amplification in the IF. However flicker noise is high around dc and dc offset

is always present. Also mismatches between I and Q phase signal path cause significant problem. So the design of channel select filter in the direct conversion receiver should be done carefully.

2.4.3 Wide-Band IF receiver

Wideband IF receiver down converts a group of channels simultaneously [48] as shown in Figure 2.8. In most wide-band IF receiver, simple low pass filters are used at IF to suppress higher frequency components, allowing all channels to pass the second stage of down converters, where the required channel is converted to low intermediate frequency [48]. The second mixer and latter stages constitute a low-IF receiver [48]. A benefit of the wide-band architecture is the adaptation of a high IF in which the image is outside the pass band of the pre-selection filter. Another advantage of the wide-band IF receiver is that it eases full synthesizer integration [48]. The fixed frequency RF local oscillator is easier to implement, since a crystal controlled wide-band PLL with a high phase detector frequency can be used to clean up the phase noise spectrum of the VCO [48]. The requirements for high Q components are thus relaxed. The wide-band IF architecture uses the same frequency selection criteria as the first IF super heterodyne architecture. If the second mixer stage does not convert the signal directly down to base band, the secondary image can be a problem. However, most wide-band IF architecture use a zero IF after the mixers. As shown in the Figure 2.8, the low pass filters between the mixers are only necessary to suppress the up converted product generated in the first down conversion [46]. The channel selection filters are placed after the second down conversion. Typically, the limited output bandwidth of the RF mixers together with the interconnection to the second mixing stage attenuates the high-frequency products without any extra components [46]. In this architecture, the local oscillator to RF leakage is less important because the first local oscillator is outside the pass band of the preselection filter like in super heterodyne. The wide band IF topologies transfer the typical down conversion problems of a direct conversion into the second mixer stage [48], [46]. The distortion generated around dc in the first mixer is not significant because the portion, which passes the possible ac-coupling between the stages, is mainly up converted in the second mixers.

The most critical blocks are the second mixers which can handle all radio channels passing through preselection filter.

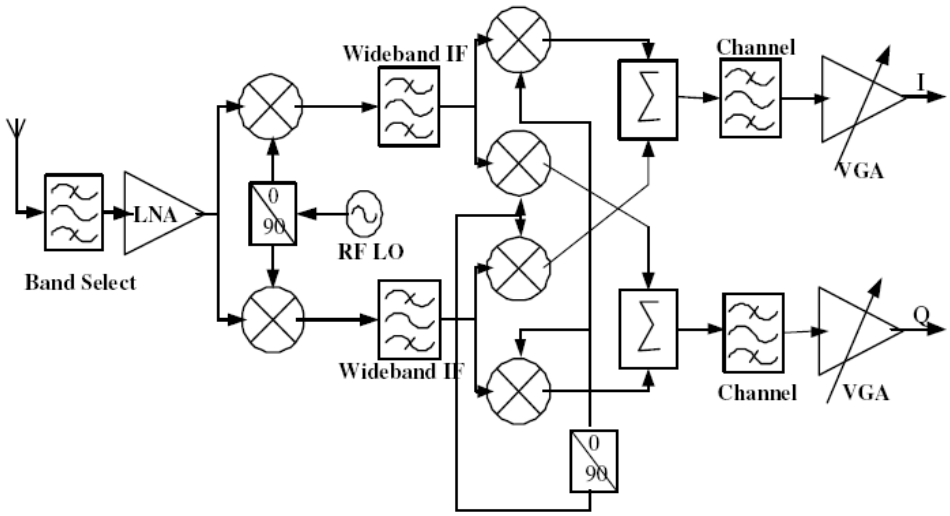


Figure 2.8 Wide Band IF Receiver

2.4.4 Digital IF receivers

Digital signal processing would provide significant benefits compared to analog circuitry [46]. When the down conversion to base band is performed digitally, dc offset, flicker noise or matching problems can be eliminated. However, due to the resolution or increased power consumption and sampling rate of ADC, direct RF to digital conversion is impossible with current technology. But low frequency operations, such as the second set of mixing and filtering in the dual IF heterodyne conversion, can be performed more efficiently in the digital domain. Figure 2.9 shows the digital IF receiver. In this Figure, the first IF signal is digitized, mixed with the quadrature phases of a digital sinusoid, and low pass filtered to yield the quadrature base band signals [49]. Problem of mismatch in I and Q is avoid by digital processing [49]. The issue in this architecture is the requirement of ADC. ADC dynamic range must be wide enough to handle the signal variations caused by path loss. Also band pass filter should have wide signal handling capability, dynamic range (DR) and need to suppress adjacent channel interferers effectively. Since the power consumption and requirement of ADC is too high for the mobile set receivers, this Digital IF receiver architecture is mainly used in the base station [49].

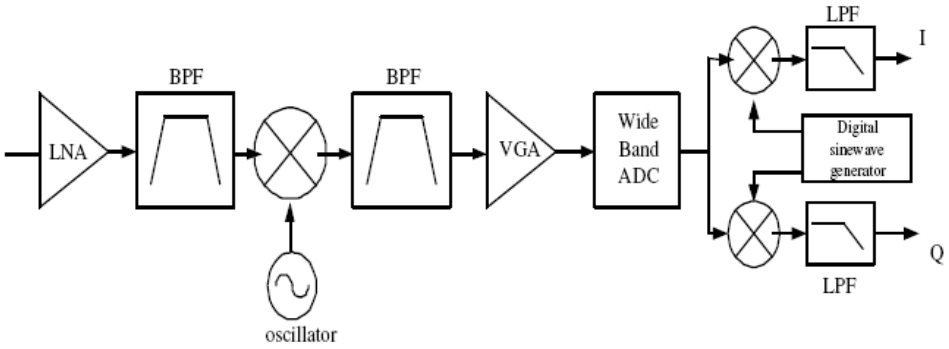


Figure 2.9 Digital IF Receiver

2.5 Channel Selection Filters

Channel selection filtering is dependent on the receiver's ability to suppress the adjacent channel interference and in-band blocking level. Received signal contains not only the desired channel but a multitude of neighboring channels or other interferers which must be attenuated before the detection [44].

The channel filtering can be done at an intermediate frequency, at base band or even over the A/D interface. In super heterodyne receivers, the channel filtering is performed at the intermediate frequency (IF) with a passive filter [44]. The passive filter is very linear and reduces the interferers without corrupting the desired signal. However, the passive filter must be used externally so it is not suitable for system on chip configure ration. In direct conversion or wide-band IF a receiver, the channel selection filtering is performed at the base band. The required quality factor of the filter is not high so that the channel selection filters can be integrated with other receiver blocks. However, the linearity requirement of the filter is high because adjacent channel interferers are unattenuated so that the filter must suppress the interferers without the production of significant intermodulation products [50].

When designing the channel selection filtering partition the filtering between the analog and the digital domain is main issue. Generally it is preferable to realize as much filtering as possible in the digital domain because this reduces the analog complexity. However, the penalty of pushing more filtering into the digital domain is that the requirements of ADC and digital complexity increase.

2.5.1 Channel Selection Filtering and ADC requirements

In modern communication system, the signal is eventually converted to a digital representation. Therefore, analog to digital converter (ADC) should be used to convert analog information to digital [47-48]. If the ADC is able to handle every interferers and noise generated by preceding blocks, channel selection can be done in digital domain [30], [47-48]. This is desirable case since digital filters are very accurate and do not require tuning circuitry. Also digital filters are readily integrated together with the front-end of the receiver [44]. However it is very difficult to design the ADC that has extremely high dynamic range (DR) and linearity with low power consumption. Even if the ADC can handle all the interferers, the power consumption would be very high due to the increased resolution requirements since the power of Nyquist rate ADC is proportional 2^N where N indicates number of bits [47]. Thus, this is not recommended for low power mobile receiver. In the other case, channel selection filtering can be done fully in analog domain. Since the channel selection filter in the analog domain reduces the power of interferers, the dynamic range requirement of the ADC is relaxed. As the order of analog channel selection filter increases, the requirement of ADC is more relaxed, but the increased order of analog domain filter increases signal delay and phase distortion [48]. Usually group delay and phase near the cut-off frequency are highly distorted than other region [48], [47], so the distortion should be compensated with extra circuitry such as all pass filter. Moreover, higher order filter increases the complexity of tuning circuit since the quality factor and attenuation rate of the filter are increased. In selecting analog low pass filters for the channel-selection filtering, three important parameters have to be determined: filter prototype function, 3 dB corner frequency, and filter order [48].

2.6 CMOS Continuous Time Filters

In CMOS technologies, the analog channel selection filter design techniques can be classified into continuous filters and sampled data filters [51-52]. The sampled data filters use many non-overlapping clock phases. Among the sampled data filters, switched capacitor filter is very popular. The main characteristics of the switched capacitor filters are determined by a clock frequency and by capacitor ratios [51-53]. The switched capacitor filter is used in low frequency such as audio frequency due to requirements of high speed clocks for switching and settling time of amplifier. In contrast to the sampled data filters, analog continuous time filters directly process analog signals. Owing to the continuous time nature, analog continuous time filters are most suitable for high frequency filtering [50]. A major disadvantage of continuous time filters is that the filter coefficients are sensitive to process and temperature variations along with aging. For this reason, tuning of the frequency is necessary. Regardless of the high sensitivity to the process and temperature variations, continuous time filter is receiving more interest due to fast data processing capability.

For the realization of fully integrated analog filters, there are many things which must be considered.

(I) First, the size of capacitor and resistor should be limited. Since integrated capacitors such as poly insulator poly capacitors or metal insulator metal capacitors occupy a large area so that the size of capacitor must be limited. For example, the capacitance can be expressed by

$$C = \varepsilon_r \varepsilon_0 \frac{A}{t}$$

----------(2.2)

Where A = area of the capacitor, t = thickness, "ε_0 = permittivity = 8.854×10−12F/m.

"ε_r = relative permittivity which is usually equal to 3.78 in CMOS. In CMOS, t is usually equal to 6×10−8m. To get the capacitance of 50 pF, an area of about $(300\mu m)^2$ is necessary [53], [45]. This area is relatively large compared to the area of other active

components. The capacitor also should not be too small because of the effect of parasitic capacitance [53]. Also large sizes of passive resistors often contain huge parasitic capacitances, which highly degrade the linearity of the filter. Therefore, optimum size of capacitors and resistors must be carefully decided.

(II) Frequency response of the filter must be stable. This means that every element in the filter should have accurate and stable values in the presence of fabrication tolerances and temperature variations, but this is almost impossible in an integrated circuit. In the integrated circuit, the ratio between same resistors or capacitors can be relatively accurate, but the absolute values are usually varied by ± 20 % [53]. This indicates that the RC time constant can be varied by ± 40 %. Furthermore, the quality factor of the filter is highly affected by small errors of the phase and component variation. Such process variations require tuning circuits for frequency and quality factor. This extra circuit often becomes a bottleneck in the realization of low power consumption and high dynamic range filter.

(III) Analog continuous time filters must be able to handle large signal because wide dynamic range required in radio receiver for large signal swings. However, these are increasingly difficult to achieve as power supply voltages are reduced and bandwidth is increased.

(IV) Analog IC filters are often located with data converters and digital circuits on the same chip. In this case, noise due to clock or switching is transferred to the analog filters through power supply line. This noise highly degrades dynamic range (DR) and signal to noise ratio (SNR) of the analog filter. Therefore, special design and layout techniques must require minimizing the effect of the noise [53].

In CMOS technologies, Active-RC, MOSFET-C and Gm-C filters are the most popular base band filters for wireless communication. Active RC filters usually apply lossy and lossless integrators to attenuate interferers. MOSFET-C filters have similar architecture

as Active-RC filters with replace passive resistors with a triode region transistor. Gm-C filters use transconductors and capacitors to attenuate interferers. Because of Gm-C open loop nature, it has been used for high frequency application. Each filter mentioned has its own advantages and disadvantages in terms of speed, linearity, and tunability.

2.6.1 Active RC Filter

The most popular continuous time filter is the active-RC filter which provides good dynamic range and low distortion. Thus, active RC filters are still widely used in low frequency application. However, low speed due to the negative feedback makes the filter difficult to apply for high speed wireless communication system. Usually, the gain bandwidth(GBW) of the amplifier for active RC filter needs to be around 20 - 30 times higher than the filter cut-off frequency to minimize phase error and any other non-idealities which occur near the GBW [54], [30], [47]. In the case of WLAN, this implies that the amplifier needs to have 300MHz GBW when the output load is connected. Active-RC filters are mostly applied in low frequency application even though the filters demonstrate superior performance.

Most active-RC filters are designed based on the active-RC integrator. In the active RC integrator, a capacitor is connected in negative feedback to function as the integrating element and a resistor is used to feed current into the capacitor [55]. Figure 2.10 shows the RC-OP amp integrator. If we assume an ideal operational amplifier is used, the relation between the input and output voltage in the s-domain is given by

$$\frac{V_{in}(t)-V^{-}(t)}{R}=C\frac{d[V^{-}(t)-V_{out}(t)]}{dt}$$

----------(2.3)

$$V_{out}=\frac{-1}{RC}\int_{0}^{\alpha}V_{in}(t)dt$$

----------(2.4)

$$V_{out} = -\frac{1}{RC}\int_{0}^{\infty} V_{in}(t)dt$$

----------**(2.5)**

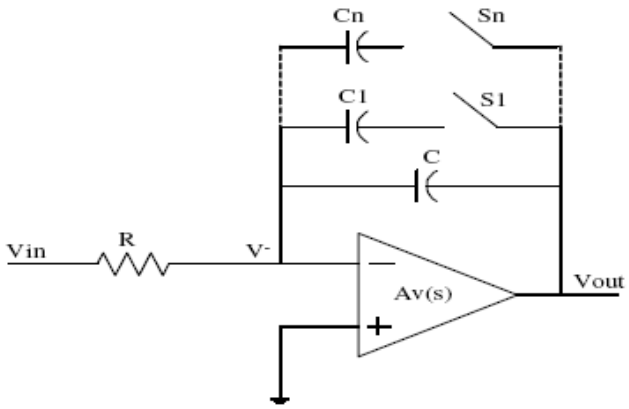


Figure 2.10 RC-OP amp Integrator

In the ideal integrator, the time constant is RC and the phase is 90 degrees. However, non-ideal op-amp gives an impact on the integrator transfer function and quality factor of the filter [55]. Since op amp has finite dc gain ADC and the finite gain bandwidth GBW, the transfer function of the op amp can be expressed as

$$A(s) = \frac{GBW}{S + \frac{GBW}{A_{DC}}}$$

----------**(2.6)**

$$V_{out(s)} \approx \frac{\frac{-1}{RC}V_{in(s)}}{(1+\frac{S}{GBW})(S+\frac{1}{RC}\frac{1}{A_{DC}})}$$

----------**(2.7)**

As an ideal integrator, GBW and DC gain of the amplifier must be infinite or very high [55]. However, it is difficult to obtain high GBW and DC gain at the same time since high DC gain is obtained with a multi-stage amplifier [56]. Therefore, the real integrator only works in a certain frequency range.

In an active RC integrator, the resistor transfers the input voltage into current, and the feedback capacitor integrates the input current because no current flows to the amplifier input [57],[55]. There are basically different integrators: lossy and lossless integrators. Figure 2.10 shows a lossless integrator with binary weighted capacitor array. Adding a resistor in parallel with integrating capacitor, lossy integrators are formed [57]. Usually op-amp is used as an active element, but OTA with high output impedance and large gm can also be used for an integrator [58]. In the ideal case, the active RC filter is insensitive to parasitic capacitance because it is connected to a virtual ground or driven by a voltage source [53]. But due to the limited DC gain, unity gain bandwidth, and output resistance, the parasitic capacitances affect the transfer function of the integrator slightly.

As shown in equation 2.5, with R and C the time constant of the integrator is determined. The time constant typically varies by ±50 %, due to variations in process and temperature. The time constant of an active RC integrator can be tuned using series or parallel capacitor or resistor matrices. The series resistor and parallel capacitor matrices occupy less area [59], [55]. In practice, parallel capacitors as shown in Figure 2.10 are used because the switch on resistance produces a LHP zero without shifting the integrator time constant [55]. The sizes of the switched capacitors are binary weighted in order to simplify the digital control of time constants. Whether the CMOS-switches locate at the input or the output of the amplifier based on the requirements. At the inverting input node, the switch on-resistance has almost no effect on the linearity, but the parasitic capacitances of the switch are added to the inverting input [47], [55]. Alternatively, at the output node, the switch on resistance degrades the linearity, particularly at high frequencies, but the parasitic capacitances of the switches have minimal effect on the performance of the integrator.

In the parallel capacitor array, the limited on-resistance of the CMOS switches used have a minimal effect on the high frequency performance of the integrator since any resistance which is in series with the integrating capacitor has a phase lead at high frequencies [55].

This phase lead reduces the high frequency phase lag deriving from the limited bandwidth of the amplifier [45].

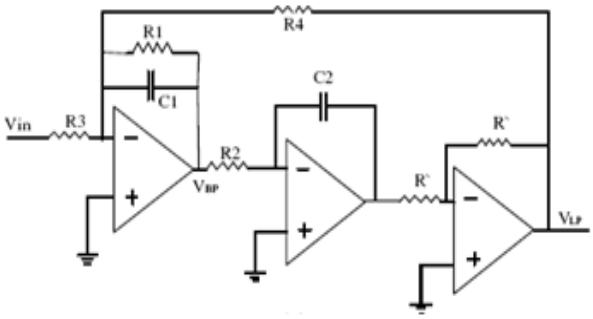
There are many different active RC filters. Among them, Tow-Thomas filter, Ackerberg Mossberg, and Sallen-key filter are the most well known filters. The second order Tow-Thomas and Ackerberg Mossberg filters are usually a combination of lossy, lossless integrators and adder. Adder is simply designed with parallel connection of input resistors at the integrator. Figure 2.11 shows the Tow-Thomas and Ackerberg Mossberg filters. The Sallen-Key filter uses one amplifier, resistors, and capacitors to realize 2nd order filter. Since the structure is simple and only one amplifier is necessary, Sallen-key filters are generally used as antialias filters. Figure 2.12 shows the Sallen-key filter.

2.6.2 MOSFET-C Filter

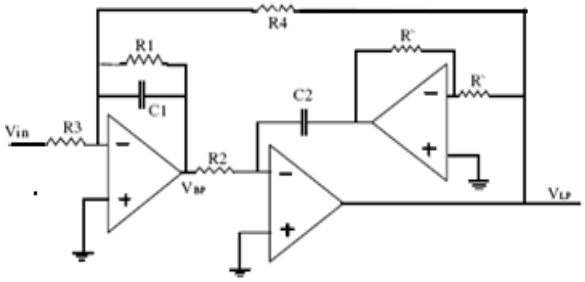
The MOSFET -C Filters are basically active RC filters but in place of resistor, tunable CMOS triode region transistors is placed. [47][53]. so, the time constant can be tuned by controlling the gate voltage Vc [53], [60].

The advantage of the MOSFET-C filter is that the resistance is controlled by a control voltage, V_C, resulting in an extended tuning range as the resistance increases to infinity [50], [61]. However, very high resistance values cannot be used in practice because of device mismatches and noise. In addition, rather high control voltage, V_C is required for the triode region operation of the transistor. Due to this, it is difficult to get large signal swing when supply voltage is low. Moreover, MOSFET-C filtering technique is based on voltage mode op-amp so that high-frequency operation is achieved [52], [60], [61].

The tunable CMOS resistors eliminate the use of capacitor matrices for time constant tuning. However, the triode region MOS resistor produces harmonics when the input signal is increased [53], [51]. Generally, the voltage difference between drain and source, V_{DS} should be smaller than 20 % of the voltage difference between gate and threshold voltage, $V_G - V_{TH}$ [53], for low harmonic components. If $V_G - V_{TH}$ is 1V, V_{DS} should be smaller than 200 mV. However, if a fully differential structure as shown in Figure 2.13 is used, the even order harmonics can be eliminated and increase the linearity [53], [45], [61]. In triode region, small signal current i^+_{DS} and i^-_{DS} are



(a)



(b)

Figure.2.11 (a) Tow-Thomas Filter (b) Ackerberg-Mossberg Filter

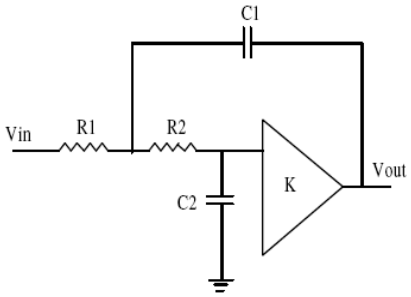


Figure.2.12 Sallen –Key Filter

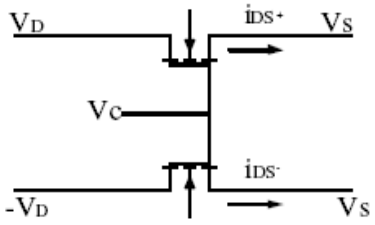


Figure.2.13 Fully-Differential MOS Resistor

$$i^{+}_{DC} = \mu C_{ox} \frac{W}{L}[(V_C - V_{th} - V_s)(V_D - V_S) - \frac{1}{2}(V_D - V_S)^2]$$

----------(2.8)

$$i^{-}_{DC} = \mu C_{ox} \frac{W}{L}[(V_C - V_{th} - V_s)(-V_D - V_S) - \frac{1}{2}(-V_D - V_S)^2]$$

----------(2.9)

$$i = i^{+}_{DS} - i^{-}_{DS} = \mu C_{ox} \frac{W}{L}(V_C - V_{DS})2V_{DS}$$

----------(2.10)

$$R = \frac{2V_{DS}}{i^{+}_{DS} - i^{-}_{DS}} = \frac{1}{\mu C_{ox} \frac{W}{L}(V_C - V_{th})}$$

----------(2.11)

So, the second order equation is cancelled and the current difference is proportional to V_{DS} and controlled by V_C. As long as the transistors are in the triode region, linear resistance can be achieved.

MOSFET-C filter is required with passive resistor which can be replaced with triode region MOSFETs [53][62] but parasitic capacitance of triode region transistor can affect the characteristic of filter. Filter architecture is insensitive to parasitic C_P which can be minimized when it is connected to virtual ground or output of Op-amp [45].Figure. 2.14 show the suitable filter structure for MOSFET-C filter realization. Charge and discharge of C_{P1} by V_S do not affect the performance. Also, the top and bottom plates of C_{P2} are connected to virtual ground and signal ground respectively. Therefore, this parasitic capacitance does not affect the performance. Output parasitic capacitance C_{P3} is connected to low impedance output node so the charge and discharge of the parasitic

capacitance do not affects the filter much. According to Figure 2.14, a Tow thomas filter or a Sallen-key filter is a generally used structure for MOSFET-C filter [53], [63].

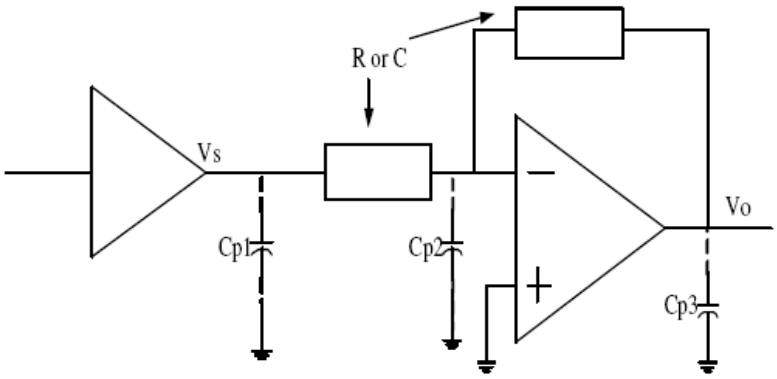


Figure.2.14 Filter Structure for MOSFET-C filter

2.6.3 OTA-C filter

OTA-C filters are more suited to high speed applications as opposed to the active RC and MOSFET-C filters described in the previous sections since they can be used in an open-loop configuration and it need not constrained by the stability requirement [64], [61], [31]. OTA-C filter is generally known as Gm-C filter. OTA is basically different from a transconductor. OTA is an op amp without a low impedance output stage, ideally operating with a virtual ground at its input and whose transconductance value is mostly irrelevant, because its voltage gain is high [61]. A transconductor is a simply voltage controlled current source [61]. However, OTA-C or Gm-C filters usually have identical filter structures and functions, OTA-C filter in this section also includes Gm-C filter.

The drawback of using OTA in an open loop configuration is that the circuit is limited to very small input levels which is required to operate the transconductor in linear region [65], [61]. Even though many different techniques have been reported to increase the

input range while maintaining linearity, these techniques often degrade the frequency response due to additional parasitic [52], [65]. Even with the linearization technique, the input signal swing range is still less compared to the active -RC filters. Another drawback of OTA-C filters is their dependence on the parameter gm which makes them highly susceptible to process variations. This drawback can be accounted by including some kind of automatic tuning [52].

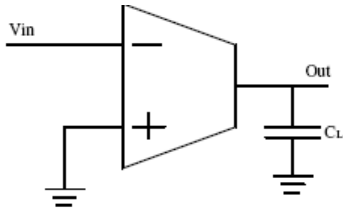


Figure.2.15 Gm-C Integrator

Gm-C integrator is a key block of the OTA-C filter. In a Gm-C integrator, the transconductance (gm) and integration capacitor C determine the unity gain frequency of the integrator. Instead of a simple transconductor, the operational transconductance amplifier (OTA) can be used. Figure 2.15 shows a Gm -C integrator. The input is fed into the transconductor of transconductance Gm and the output current of the transconductor is integrated by a capacitor.

$$V_o(s) = \frac{g_m}{sC_L} V_{in}(s)$$

----------(2.12)

In a Gm-C integrator, the integration is a passive operation because the Transconductor transforms the input signal into another form [44]. So, in case of summing operation, to add N inputs N transconductors required.

Figure 2.16 shows the 1st order OTA-C filters. One advantage of the OTA-C filter is that passive components like the resistor and inductor can be realized with OTA and capacitor [53], [45]. As shown in the Figure 2.16, the resistor is realized by connecting negative input of OTA to positive output and the function of inductor can be realized in certain frequency by using two OTAs and a capacitor. However performance of OTA is dependent on linearity of resistor and inductor, so when high linearity is required passive resistor is used. Figure 2.17 shows the fully differential OTA-C biquad filter. As shown

in the Figure 2.16, low pass and band pass functions can be obtained from the biquad OTA-C. In this filter, the passive resistor is replaced with OTA by negative feedback connection. This filter is 2nd order. For the higher order filter, this biquad filter can be cascaded.

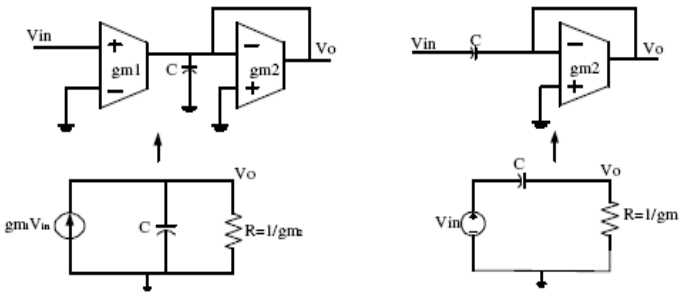


Figure.2.16 OTA-C filter

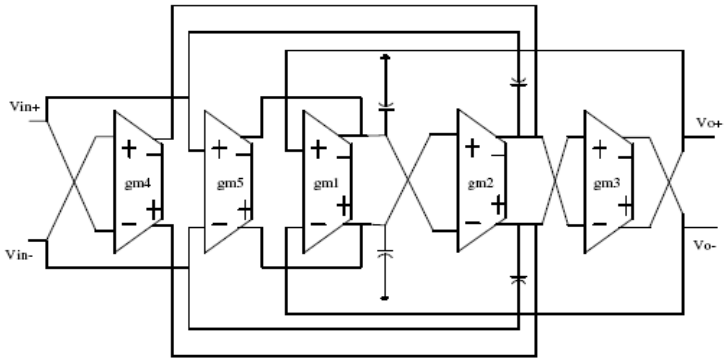


Figure 2.17 OTA-C Biaquad Filter

2.7 CMOS OTAs

CMOS technologies are very convenient for implementing OTAs because their MOSFETs are inherently voltage-controlled current devices. A variety of CMOS OTAs with different topologies have been designed and developed for different purposes so far. According to their input/output topologies though, they can be categorized into the previously mentioned three types, i.e., single input/output, differential-input single-output, and differential input/output. These three types of CMOS OTAs with their advantages and disadvantages are described below.

2.7.1 Single input/output OTAs

Figure2-18 presents some common CMOS topologies [66] to implement the single input/output OTAs. Figure 2-18(a) is a single-NMOS common-source transconductor. Although it is the simplest, it has relatively low output impedance due to its Miller effect (input-output coupling) and low linearity, deviating it from an ideal OTA. To alleviate this problem, a cascode topology in Figure 2-18(b) is suggested, where a common-gate transistor M_2 is introduced to provide isolation between the input and output. This unilateralization method increases not only the output impedance and linearity, but also the bandwidth and the available transconductance, at the expense of a higher voltage supply. The third topology in Figure 2-18(c) differs from the cascode topology in its common-gate transistor, where a PMOS transistor is applied instead of a NMOS one, resulting in a folded cascode topology. It provides the same isolation, but with a reduced voltage supply. Figure 2-18(d) is a regulated-cascode transconductor, which is an enhanced cascode transconductor. It replaces the gate DC bias of M_2 in Figure 2-19(b) with a negative feedback from its source. This feedback further improves the linearity and the output impedance by a factor of *(A+1)* compared to the cascode transconductor, where *A* is the feedback gain. The improvement mechanism behind the cascode and regulated cascode topologies will be further explained in the next chapter. The fifth one in Figure 2-18(e) utilizes a PMOS current mirror to convert a negative transconductor to a positive one.

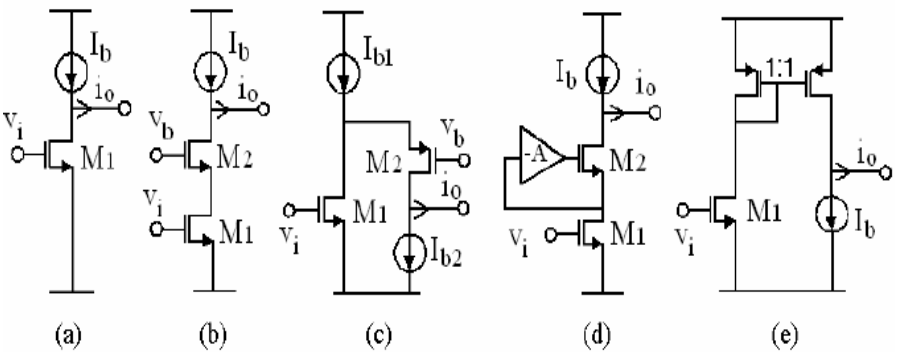


Figure 2.18 Single Input/output OTA [66] (a) Common Source Transconductor (b) cascade Transconductor (c) Folded Cascode Transconductor (d) Regulated Cascode Transconductor (e) Positive Transconductor

Ignoring the parasitic in cascode and regulated-cascode transconductors in Figure.2-18(b), (c), and (d), the output currents of their input common-source transistors (M_1) will propagate to their outputs (i_o) without any loss. Therefore, despite the different topologies of the transconductors in Figure 2-18, their transconductance g_m can be unified, where $g_{m,M1}$ is the transconductance of the input transistor M_1, and V_i and i_o are the input voltage and output current respectively. The sign ± is inserted to discriminate the positive transconductor in Figure 2-18(e) from the other negative ones. The transconductance in (2-1) can be tuned through the control of the DC current of each transconductor above. The more DC current, an OTA consumes, it has large tuning range and transconductance.

$$g_m = \frac{i_0}{v_i} \approx \pm g_{m,M1}$$

----------(2.13)

2.7.2 Differential OTAs

Figure 2-19 depicts two typical CMOS implementations of the second-type OTA with the differential-input single-output topology [66]. They both contain a source-coupled differential-pair input stage, which can provide high input impedance, high gain, and high common-mode rejection simultaneously without much sacrifice. A scrutiny of their signal paths after the input stages reveals the important role that current mirrors play in these two implementations.

In Figure 2-19(a), the current mirror CMp transfers the left output current of the input differential pair, i_d^+ , to the right to combine with its right output current i_d^- ,from which the transconductor output current is twice, so does its transconductance:

$$g_m = \frac{i_0}{v^+_i - v^-_i} = g_{m,M1}$$

----------(2.14)

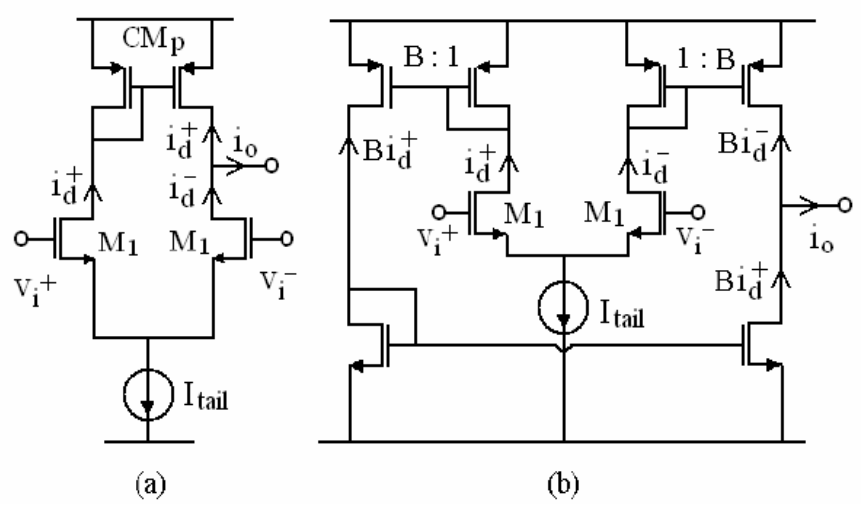


Figure 2.19 Differential Input and Single Output [66]
(a) Simple OTA (b) Balance OTA

The balanced implementation in Figure 2-19(b) is different from Figure. 2-19(a) in that two PMOS current mirrors are added after the input differential pair improves the balance between its differential inputs. Furthermore, these two PMOS current mirrors can be set in such way that they have a size ratio of B between their (i) reference transistor and (ii) controlled transistor. This boosts their output currents by B times [67]. The boosted currents are combined at the output using a NMOS current mirror at the bottom, resulting in a transconductance as large as B times of the previous one's:

$$g_m = \frac{i_0}{v^+_i - v^-_i} = -Bg_{m,M1}$$

----------(2.15)

The transconductance in (2-14) and (2-15) can both be tuned by changing the DC tail currents I_{tail} in Figure. 2-19(a) and Figure 2.19(b). Equations (2-14) and (2-15) manifest the significant improvements of the transconductance by using the current mirrors compared to those in which single output is taken. The two equations, assume the ideal combination so that the two differential output currents arrive there at the same time. It is not exactly the fact because the output current from the left in each implementation in Figure. 2-19 requires an additional current mirror to combine itself with the right one, which introduces a time-delay difference between the two combined currents. Therefore, equations (2-14) and (2-15) are valid only when the time delay of the current mirrors for

the current combinations is negligible compared with operating signal cycle. As the operating signal cycle decreases, the time delay will become comparable and the improvement from using the current mirrors will be lessened.

The CMOS OTAs in Figure 2-20 illustrate two OTA implementations for the third-type fully-differential topology [66]. One can see that their structures are similar to that in Figure.2-20(b), but their two output currents remain. The aforementioned size ratio of B can also be applied in the current mirrors to increase their transconductance and therefore their current efficiency. The two OTAs in Figure 2-20 have the same transconductance, as can be derived below,

$$g_m = \frac{i_0}{v^+_i - v^-_i} = Bg_{m,M1}$$

----------(2.16)

Again, the DC tail currents I_{tail} in Figure 2-20 can be used for the above transconductance tuning. Compared to the OTA in Figure 2-20(a), the one in Figure.2-20(b) has an additional common-mode feed forward (CMFF) circuit comprising M_{C1}, M_{C2}, and M_{C3} to further enhance its common-mode rejection. The sizes of M_{C1}, M_{C2}, and M_{C3} should be properly selected to achieve a common-mode transconductance gain of $Bg_{m,M1}$, in order to optimize its common-mode cancellation with the B-size PMOS transistors at the outputs, which have a common-mode transconductance gain of - $Bg_{m,M1}$.

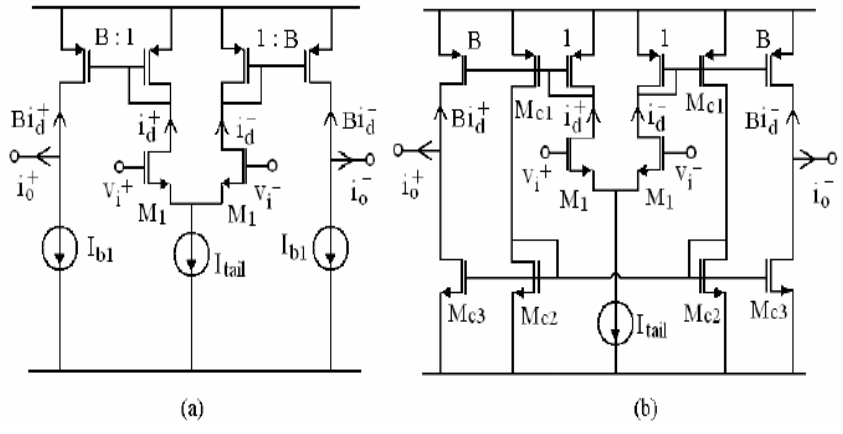


Figure 2.20 Differential Input/output OTA [66]

2.7.3 OTA Trends

Currently, high frequency, high linearity, and low power are the three main concerns of CMOS OTAs. With many efforts, researchers have made significant progress in these three aspects of CMOS OTAs, especially the latter two. Meanwhile, there are lots of problems in each aspect as well as in combining all three aspects. Tradeoffs have to be made among these aspects in designing practical OTAs. The current trends on these aspects are reviewed below.

2.7.3.1 High Frequency

As mentioned previously, OTAs are regarded as a good candidate to replace OPAMPs for high-frequency applications. OTAs that can operate up to several hundred MHz have been reported [68-78]. For higher frequencies, such as those above 1 GHz, new technologies and techniques are required.

CMOS scaling technology is one driving force behind the high-frequency OTAs. OTAs are built using transistors which mainly determine the OTA frequencies. Transistors with high cutoff frequency (f_T) and high maximum oscillation frequency (f_{MAX}) are desired. Most OTAs developed using long-channel CMOS technologies (>0.5 μm) had frequencies limited to 100 MHz or less according to [66] and its references. As the lengths of CMOS devices are scaled down, both channel delays and parasitic capacitances are reduced, which increases the cutoff frequencies of the transistors. Current CMOS 0.18 μm technology with f_{MAX} up to 40 GHz has been well commercialized [79], and 0.13 μm, 90 μm, 65nm, and even 45nm technologies are also available to researchers, all with much higher f_{MAX} than the 0.18-μm technology [80], [81]. These submicron and deep-submicron advanced technologies offer significant potential for various OTAs to be implemented at RF and even microwave frequencies. However, the study of RF/microwave OTAs circuits using these advanced technologies is still in its infancy.

Besides the scaling technology, OTA topologies are also very important for high-frequency OTAs. For an OTA in a given CMOS technology, capacitive parasitics can be

reduced by optimizing its topology in order to maximize its frequency. To this end, simpler topologies are preferable. Those OTAs with multiple stages [82-83] are complicated structures and not suited for high-frequency purpose. As previously discussed for the second-type OTAs, the use of current mirrors to combine one differential output current with the other results in different time delays for the two paths, which is also not suitable. The simplest topology is single-transistor common-source transconductor that probably has the least parasitics in all possible topologies which has been used in RF circuits. This simplest topology has low output impedance, low linearity and small transconductance. The described cascode topologies are a good solution, which have an excellent balance between complexity and performance. They have been widely used in low noise amplifier designs at RF and microwave frequencies [84]. It will be shown in the rest of this thesis that the cascode topologies are also very useful for high-frequency OTAs.

2.7.3.2 High Linearity

Linearity is a common issue of OTAs. When small input signals are applied then the output currents of a CMOS differential pair depend linearly on its input gate voltages only when small input signals are applied. Otherwise, high-order nonlinear terms must be included in the expression of the OTA output current [66],

$$i_0 = \sum_{i=1}^{\alpha} a_i v_1^{\,i} + \sum_{i=1}^{\alpha} b_i v_2^{\,i} + \sum_{1}^{\alpha}\sum_{1}^{\alpha} C_{ij} v_1^{\,i} v_2^{\,i}$$

----------(2.17)

These nonlinear terms cause significant distortion of the transconductance, which reduces the desired fundamental signal and presents harmful inter-modulation products at the output of the OTA [85], [86].

To reduce the nonlinear problem, several techniques have been proposed. One simple way is to directly put a voltage divider before an OTA, such that the input voltage of the OTA itself is kept small for its linear operation. However, it also reduces the available transconductance as a tradeoff. Source degeneration illustrated in Figure.2-21 is a

common way to reduce the nonlinearity, which also reduces transconductance usually by an order of the source degeneration factor N [66]. The two topologies presented in Figure.2-21(a) and Figure.2-21(b) utilizes degeneration resistors at the sources which realize the same transconductance and degeneration, and it can be exchanged. Shown in Figure.2-21(c), (d) and (e) are three active source-degeneration topologies based on topology as shown in Figure. 2-21(b). The degeneration resistor is simply replaced by a triode MOSFET in Figure.2-21(c). The one in Figure.2-21(d) also uses triode-MOSFETs, but with an additional internal mechanism that increases its transconductance for large signals, hence its linear range is expanded [87]. The last topology in Figure.2-21(e) utilizes two saturated transistors (M_2) for the degeneration with their drain connected to gates. Its third-harmonic distortion can be reduced by a factor of N_2, compared to its transconductance reduction of N due to the degeneration [87].

Some intelligent ways were also developed by means of an algebraic sum of nonlinear terms so that the nonlinear terms were automatically cancelled, yielding only a linear fundamental term in the ideal case [66]. Figure.2-22 shows two cross coupled topologies for the nonlinearity cancellation at the top and their practical implementations using MOSFETs at the bottom. Both topologies come from the high-order nonlinearity cancellation techniques for multipliers [66], [88].

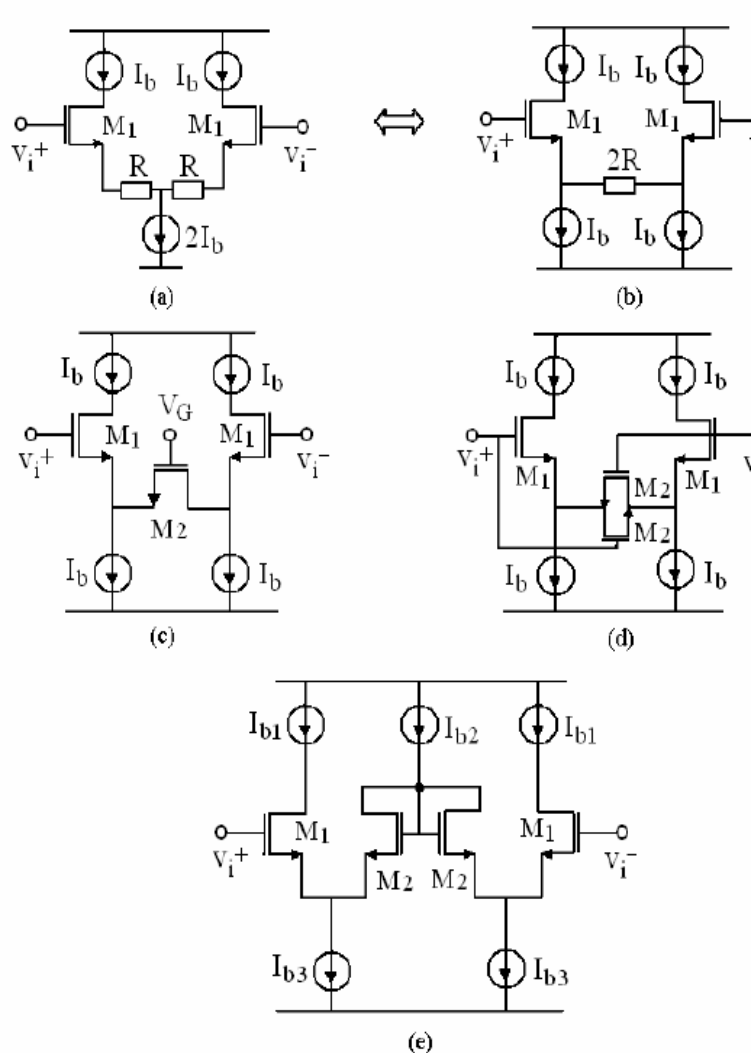


Figure 2.21 Source Degeneration Linear Technique [66]

$$(V_A V_1 - V_A V_2) - (V_A V_2 - V_A V_1) = 2V_A(V_1 - V_2)$$

----------(2.18)

$$[(V_1 + V_A)^2 + (V_2 - V_A)^2] - [(V_1 - V_A)^2 + (V_2 + V_A)^2] = 4V_A(V_1 - V_2)$$

----------(2.19)

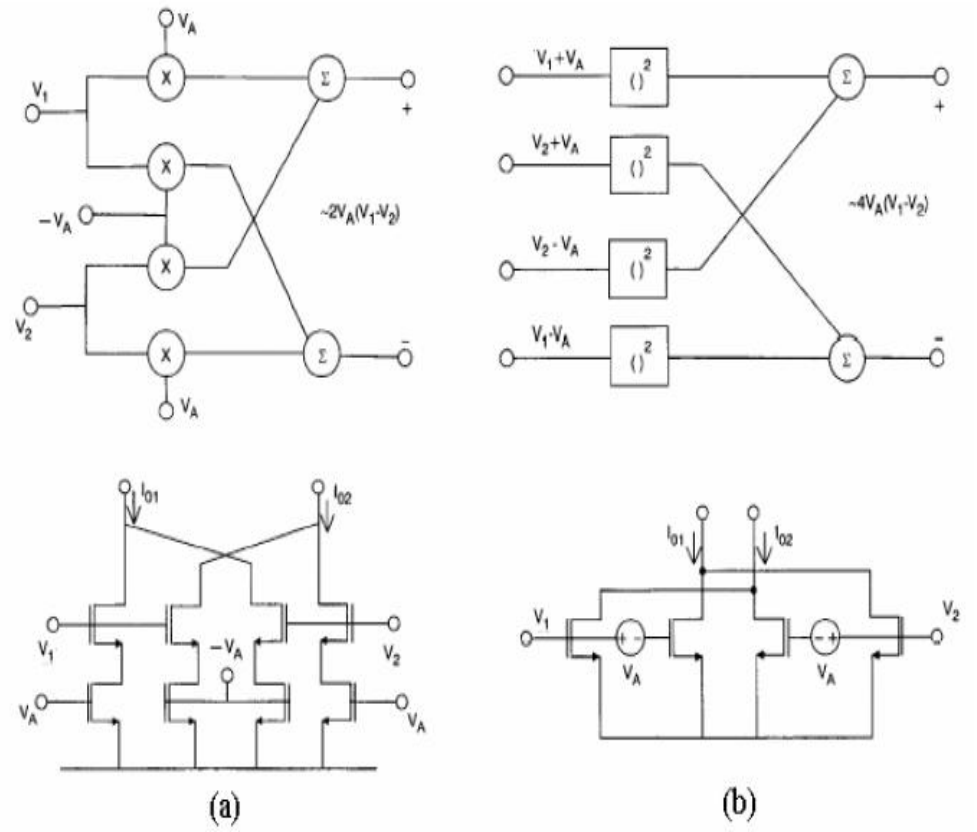


Figure 2.22 Linear techniques using nonlinear-term sum cancellation from [66]
(a) multiplication-sum technique, and
(b) squaring-sum technique (V1= -V2).

Techniques combining the above source-degeneration topologies and cross-coupled topologies also exist to further enhance the nonlinearity reduction [86-87]. Figure 2-23 presents one technique combining the topologies of Figure. 2-21(d), Figure. 2-21(e) and Figure 2-22, a complex combination technique. A byproduct of the linear techniques in Figure 2-22(d) and Figure 2-23 is a reduction in power consumption. The issue of power consumption is discussed in next section.

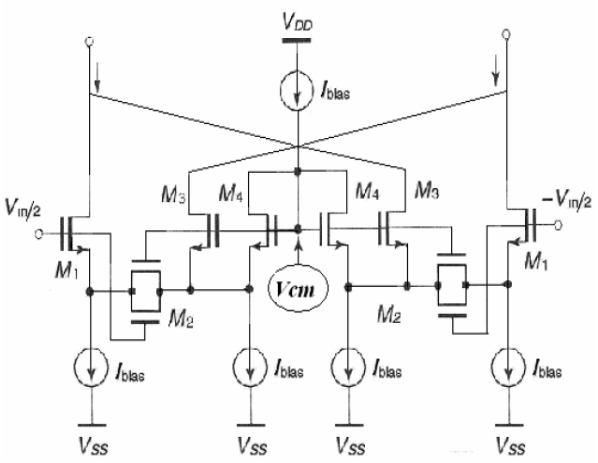


Figure 2.23 A complex combined linear technique from [87]

2.7.3.3 Low power

Mobile systems always require low power consumption in order to extend battery life. Non-portable devices also require low-power feature in order to save their energy costs as well as their thermal requirements. To use OTA circuits that contain several OTAs in such devices, low power operation of each OTA is required.

The power consumption of an OTA is determined by two factors: its DC voltage supply and its DC current. This indicates two possible choices to obtain low power requirement. The aforementioned CMOS scaling technology can enable low-voltage operations of the transistors, which allows the OTAs to operate at low voltage supplies, and it is one primary way to reduce the power consumption.

The other primary way is related to current-reduction techniques, which can reduce the DC currents flowing through the OTAs without change their transconductance, i.e., their power efficiencies can increase. Class-AB OTAs can accomplish this task. A class-AB OTA differs from a common OTA in that the class-AB has an adaptive bias circuit [67], [90-93]. A simplified class-AB OTA is shown in Figure. 2-24(a). The adaptive bias circuit can make the quiescent currents very low in order to dramatically reduce static power dissipation. When a large input signal is applied, it can automatically boost

dynamic currents well above the quiescent currents, yielding an intelligent way to make full use of the DC currents. Accordingly, the above linear topologies in Figure. 2-21(d) and Figure 2-23 are also class-AB OTAs. The adaptive bias circuit in Figure 2-24(a) is actually a local common mode feedback (LCMFB) network, which can be realized using the level-shifter in Figure. 2-24(b) The OTAs in [90-91] adopt two level-shifters with a cross-coupled structure for their two input transistors, while the work in [67] utilizes two level shifters to control the common-mode node of its input differential-pair. The latter has an advantage over the former in that the latter's lowest current in the differential pair is never less than the DC current of its level-shifter I_B, and input transistors is cutoff [67]. Using a single level-shifter also exists [92-93], but with a lower output current and a requirement for an extra common-mode sensing circuit.

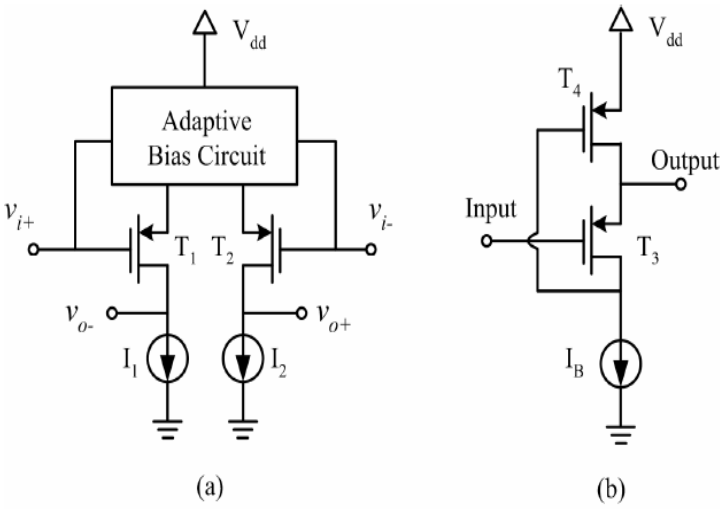


Figure: 2.24 (a) Simplified Class AB Amplifier and (b) Level Shifter [90-91]

2.8 OTA Topology

Operational Transconductance Amplifier (OTA) is usually an integral part of many analog and mixed-signal systems. OTA is a very important circuit that is used to realize functions ranging from DC bias generation to high-speed amplification or filtering depending on its levels of design complexities. There are numerous types of transconductor available in analog circuits; symmetrical CMOS OTA and folded cascode OTA are the two main types of OTA used widely in all designs. In this section, 3 types of OTA will be discussed.

2.8.1 Symmetrical CMOS OTA

A symmetrical CMOS OTA consists of one differential pair and three current mirrors as shown in Figure 2.25. The input differential pair is loaded with two equal current mirrors. The gain of such Op-amp is limited due to the gain per transistor can be quite small for nanometer MOS Transistor devices. The input devices see exactly the same DC voltage and load impedance, which give the best option in matching. Besides, this OTA gives large output swing as the output is only connected to a PMOS and a NMOS.

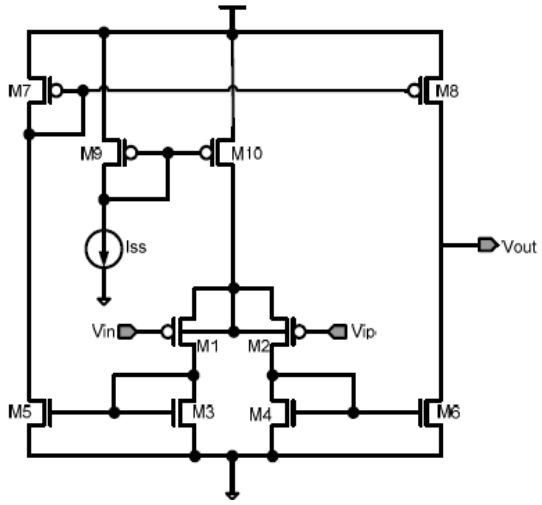


Figure 2.25 Symmetrical CMOS OTA

2.8.2 Telescopic CMOS OTA

In telescopic CMOS OTA, four cascode MOST are added M3-M6 in series with the input devices and current mirror to increase the gain as shown in Figure 2.26 Cascode M5 is included in the feedback loop around transistor M7 which allow larger output swing. Besides, telescopic has lower distortion at low frequencies and power consumption is not increase since there is only one biasing current source involved. However, the increased output impedance does not increase the GBW as the gain is increased but only at low frequencies.

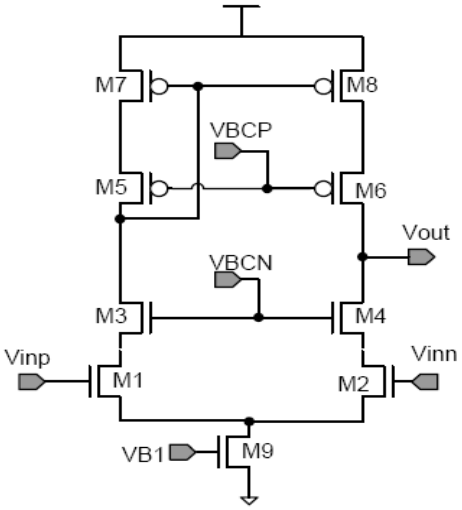


Figure 2.26 Telescopic CMOS OTA

2.8.3 Folded Cascode OTA

Folded cascode OTA consists of an input differential pair, two cascodes and one current mirror as shown in Figure 2.27. It utilizes the high swing current mirror hence output swing is higher than telescopic and high gain and GBW can be achieved because cascode at the output are used. However, the current consumption is twice of telescopic stage due to the additional current mirror. The main advantage of folded cascode OTA is that the input transistors can operate with their gate beyond the supply lines. The common mode input voltage range can include one of the supply rails and hence this can be used for single-supply systems.

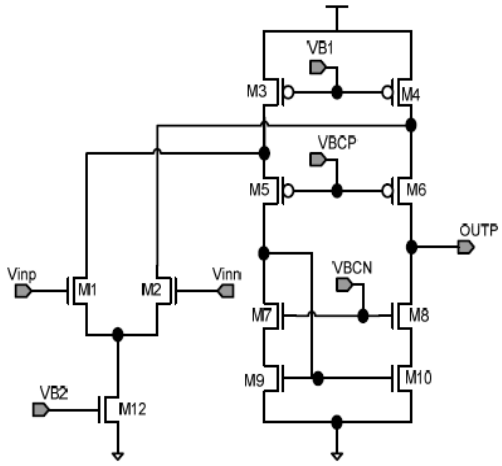


Figure 2.27 Folded Cascode OTA

The performances of 3 types of OTA can be summarized in Table 2.2. Folded cascode OTA is chosen as the base transconductance cell as it is compromising in overall performances.

Table 2.1 Comparison between various OTA Topologies

Topology	Gain BW	Output Swing	Power Dissipation	Noise
Symmetrical	**Medium**	**Highest**	**Medium**	**Highest**
Telescopic	**Medium**	**Low**	**Low**	**Low**
Folded Cascode	**High**	**Medium**	**Medium**	**Low**

2.9 Automatic Tuning Scheme

The frequency response of a filter is determined by the values of transconductances, resistances and capacitances. To maintain an accurate response of filter, absolute values of components are necessary. Absolute values on an integrated circuit can shift significantly due to process parameter variations, temperature and aging.

Depending on the accuracy of response desired, many schemes with varying complexities have been proposed and implemented. All these are collectively called "automatic tuning schemes." Since tuning of a high order filter is complex, integrated tuning schemes have generally relied on manipulating the response of basic filter building blocks like biquadratic sections. Tuning involves (i) Measure the filter response (ii) Compare the response with the desired response and (iii) Apply necessary tuning technique