# Chapter 5

**PRIMARY ZVS BASED FLYBACK CONVERTER WITH OUTPUT VOLTAGE DOUBLER**

<table>
<thead>
<tr>
<th>S.No.</th>
<th>Name of the Sub-Title</th>
<th>Page No.</th>
</tr>
</thead>
<tbody>
<tr>
<td>5.1</td>
<td>Introduction........................................................................................................... 132</td>
<td></td>
</tr>
<tr>
<td>5.2</td>
<td>Single output Flyback Converter........................................................................ 132</td>
<td></td>
</tr>
<tr>
<td>5.3</td>
<td>Multi-output Flyback Converter........................................................................... 134</td>
<td></td>
</tr>
<tr>
<td>5.4</td>
<td>Single output ZVS PWM Flyback Converter ......................................................... 149</td>
<td></td>
</tr>
<tr>
<td>5.5</td>
<td>Multi-output ZVS PWM Flyback Converter ................................................................ 160</td>
<td></td>
</tr>
<tr>
<td>5.6</td>
<td>Single output voltage doubler ZVS PWM Flyback Converter..................................... 165</td>
<td></td>
</tr>
<tr>
<td>5.7</td>
<td>Multi-output voltage doubler ZVS PWM Flyback Converter...................................... 175</td>
<td></td>
</tr>
<tr>
<td>5.8</td>
<td>Conclusion.............................................................................................................. 184</td>
<td></td>
</tr>
</tbody>
</table>
5.1 Introduction

A high frequency flyback isolated topology is well suited for most of the low voltage applications because of its lesser component count, simpler control, compact size and lesser weight. This topology finds its applications as power supplies in a Telemetry tracking transmitter.

This chapter deals with the hardware implementation of multi-output hard switched flyback converter, primary ZVS flyback converter (single output, multi-output) and primary ZVS flyback converter with output voltage doubler (single output, multi-output). Fluctuation in line and load affects the output voltage and hence the regulation of the converter. To overcome this issue, a closed loop control of the multi-output flyback converter with output voltage doubler is implemented with an analog controller IC and the results obtained are discussed in detail.

5.2 Single output Flyback Converter

The basic topology of a DC-DC flyback converter is as illustrated in Fig. 5.1. The circuit input is usually - unregulated DC voltage. The SMPS circuit is operated at a higher frequency, in the range of MHz. A fast switching device like a MOSFET switch (S) is used with fast dynamic control over the switch duty ratio for maintaining the desired output voltage. The transformer is used for voltage isolation between input and
output as well as for better matching of input and output voltage and current requirements.

![Diagram of Flyback Converter](image)

**Fig: 5.1 Basic Topology of Flyback Converter**

A flyback transformer works differently from a normal transformer, in the sense that the primary and secondary windings of flyback do not carry current simultaneously, whereas in a normal transformer, current is carried simultaneously. So, a flyback transformer is similar to two magnetically coupled inductors. Thus, the design of a flyback transformer is done in the same way as an inductor. When the gate pulse is applied, switch S is turned ON. The primary winding of the flyback transformer is directly connected to the input voltage source, causing the magnetic flux to increase in the transformer. The diode is reverse-biased since voltage across the secondary winding is negative. During this period, the output capacitor supplies energy to the load. When switch S is OFF, the energy stored in the transformer is transferred to the output. With additional secondary windings, this topology can be used to generate multiple outputs.
5.3 Multi-output Flyback Converter

Fig. 5.2 shows a 30W multi-output flyback converter topology for providing regulated voltage to the Telemetry Tracking Transmitter system. This topology is designed for converting the supply voltage (24V to 42V) into three different secondary voltages (+5V/5A, +15V/300mA, +12.5V/100mA).

Fig: 5.2 Multi-Output Flyback Converter

Fig. 5.3 shows the block diagram of the multi-output topology. The block diagram is same as shown in Fig 3.3 except for the transformer configuration which is flyback as illustrated in Fig. 5.3. As discussed in section 3.3, the low power output, that is, +12.5V/100mA is sensed and regulated using PWM controller IC UC1825. The regulated output provides supply for the PWM IC when the converter starts functioning.

5.3.1 Design

The design of the hard switched multi-output flyback converter is discussed in this section.
5.3.1.1 Specifications

Table 5.1 shows the design specifications for the multi-output flyback topology.

**Table 5.1 Electrical specifications for Design**

<table>
<thead>
<tr>
<th>Input Voltage</th>
<th>Min. ( V_{\text{min}} )</th>
<th>24 V</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max. ( V_{\text{max}} )</td>
<td>42 V</td>
<td></td>
</tr>
</tbody>
</table>

**Topology**: Hard switched multi-output Flyback using UC 3825A PWM Controller

<table>
<thead>
<tr>
<th>Switching Frequency ( f ) (kHz)</th>
<th>200 kHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>( D_{\text{max}} )</td>
<td>45% (as required by UC3825)</td>
</tr>
<tr>
<td>Efficiency ( \eta )</td>
<td>80%</td>
</tr>
<tr>
<td>Output Power ( P_{\text{out}} ) (W)</td>
<td>30.75 W</td>
</tr>
<tr>
<td>Outputs</td>
<td>+5V/5A</td>
</tr>
</tbody>
</table>

5.3.1.2 Continuous mode of operation

The design of flyback power transformer for continuous mode of operation is carried out according to the specifications given in Table 5.1.
**Primary current calculation:**

The Primary inductor, \( L_{pri} = \frac{(V_{\text{min}} - 1) \cdot V_{\text{in}} \cdot T_{\text{on}}}{25 \cdot P_{\text{out}} \cdot T} \) = 74.52\, \mu\text{H}

The Primary peak current, \( I_{\text{ppk}} = \frac{1.25 \cdot P_{\text{out}}}{V_{\text{in}} \cdot D_{\text{max}}} \) = 3.645 \, \text{A}

The Primary RMS current, \( I_{\text{rms}} = I_{\text{ppk}} \cdot \sqrt{D_{\text{max}}} \) = 2.445 \, \text{A}

Primary Turns, \( N_{\text{pri}} = 1000 \cdot \sqrt{\frac{L_{pri}}{L_{1000}}} \) = 35 \, \text{Turns}

Where,

\( P_0 \) – Output power (W)

**Secondary current calculation:**

Secondary peak current, \( I_{\text{spk}} = \frac{P_o}{V_o \cdot (1 - D_{\text{max}})} \)

\[ = 0.909 \, \text{A for } +5\text{V}/0.5\text{A output} \]
\[ = 0.545\, \text{A for } +15\text{V}/0.253\text{A output} \]
\[ = 0.181\, \text{A for } +12.5\text{V}/0.1\text{A output} \]

Secondary RMS Current, \( I_{\text{rms}} = I_{\text{spk}} \cdot \sqrt{(1 - D_{\text{max}})} \)

\[ = 6.741\, \text{A for } +5\text{V}/0.5\text{A output} \]
\[ = 0.404\, \text{A for } +12.5\text{V}/0.25\text{A output} \]
\[ = 0.134\, \text{A for } +12.5\text{V}/0.1\text{A output} \]

Secondary turns ratio,

\[ \frac{N_s}{N_{\text{pri}}} = \frac{(V_0+1) \cdot (1 - D_{\text{max}})}{(V_{\text{min}} - 1) \cdot D_{\text{max}}} \]

\[ = 19 \, \text{for } +5\text{V}/0.5\text{A output} \]
\[ = 32 \, \text{for } +12.5\text{V}/0.25\text{A output} \]
\[ = 26 \, \text{for } +12.5\text{V}/0.1\text{A output} \]

**5.3.1.3 Filter calculation:**

The output voltage equation of a flyback converter is given by:
Output capacitor, \[ C = \frac{I_o T_{on}}{V_r} \]  

Output ripple voltage \( V_r \) is considered as 100mV. Filter capacitances at the output of each load are tabulated in Table 5.2.

<table>
<thead>
<tr>
<th>Input voltage (24V-42V)</th>
<th>Output voltage-1 (5V/5A)</th>
<th>Output voltage-2 (15V/0.3A)</th>
<th>Output voltage-3 (12.5V/0.1A)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Filter capacitor</td>
<td>94( \mu F ) (two 47( \mu F ) in parallel)</td>
<td>44( \mu F ) (two 22( \mu F ) in parallel)</td>
<td>44( \mu F ) (two 22( \mu F ) in parallel)</td>
</tr>
</tbody>
</table>

From section 5.3, it is clear that continuous mode is preferred than discontinuous conduction mode, hence CCM is considered for analysis and design.

**5.3.2 Closed Loop Simulation and Implementation**

The hard switched multi-output flyback converter designed in section 5.3.1 is implemented and the closed loop implementation details are discussed in this section.

**5.3.2.1 PWM Controller design**

Design of UC1825 controller is carried out as explained in section 3.4.1. The values for \( R_t \) and \( C_t \) are calculated using equation (3.4) and
(3.5) and the design values obtained for $D_{\text{max}} = 0.9$ are, $R_t = 3.3\,\text{k}\Omega$; $C_t = 1\,\text{kpF}$.

### 5.3.2.2 Startup circuit design

PWM IC is initiated using startup circuit. The design of startup circuit is same as that explained in section 3.4.2 and the designed values are $R_8 = 9.76\,\text{k}\Omega \approx 10\,\text{k}\Omega$; $R_5 = 250\,\Omega$. Maximum power consumption of $Q_1$ is also the same as explained in section 3.4.2.

### 5.3.2.3 Stabilization of feedback loop

The design of compensation network is carried out in the same manner as that discussed in section 3.4.3. The open loop response of the converter, with a phase margin of 12.1 degree and gain margin of 23.6dB is shown in Fig. 5.4(a). The compensation network designed is a type-3 system which consists of three poles and two zeroes, including a pole at origin. In Fig. 5.4(a), crossover frequency $f_{\text{co}}$ occurs on the -2 slope of the output transfer function. The error amplifier is designed in such a way that the total gain crosses the $f_{\text{co}}$ at a -1 slope. For fixing the poles and zeros, its corresponding frequencies are fixed and the values of resistance and capacitance are calculated as given below.

i. A pole at the origin at a frequency of

$$f_{p_0} = 500\,\text{Hz}$$

ii. A first zero at a frequency of

$$f_{z_1} = 500\,\text{Hz}, \ C_2 = 18\,\text{kpF}, \ R_5 = 17.683\,\text{k}\Omega$$
iii. A second zero at a frequency of  

\[ f_{z2} = 1000 \text{Hz}, \quad C_1 = 10 \text{kpF}, \quad R_4 = 16 \text{k}\Omega \]

iv. A first pole at a frequency of  

\[ f_{p1} = 10 \text{ kHz}, \quad C_3 = 1 \text{kpF} \]

v. A second pole at a frequency of  

\[ f_{p2} = 50 \text{ kHz}, \quad R_{th} = 326 \Omega; \text{ where } R_{th} = R_2 \parallel R_3 \]

The error amplifier transfer function,

\[
G = \left( \frac{(R_5*C_2*s+1)(R_4*C_1*s+1)}{(R_4+R_{th})(C_2+C_3)*s\left[1+\frac{R_2*C_2*C_3+s}{C_2+C_3}\right] + \frac{R_4+R_{th}+C_1+s}{R_4+R_{th}}} \right)
\]

The open loop response and closed loop response of the converter are shown in Fig. 5.4(a) and (b) respectively. The phase margin is 38.1° and gain margin is 9.34dB in closed loop. The system is now a stable system.

![Bode Diagram](image1.png)  
![Bode Diagram](image2.png)  

Fig: 5.4 (a) Open loop response of converter (b) Closed loop response of flyback converter

### 5.3.3 Experimental Implementation

The experimental setup for 30W DC-DC converter is implemented and the output voltages and currents (5V/5A), (15V/0.3A) and
(12.5V/0.1A) for rated load condition obtained, are as shown in Fig. 5.5(a) – (c) respectively.

![Fig: 5.5 (a) Output-1 voltage and current (b) Output-2 voltage and current (c) Output-3 voltage and current](image)

5.3.3.1 Load transients

The load-1 is varied from 300mA to 5A under load regulation. It is observed that, compared to the cross regulation effect in secondary-1 with respect to load change in secondary-2, cross regulation effect is higher in secondary-2 with respect to load change in secondary-1. The corresponding waveforms are shown in Fig. 5.6(a), (b) and Fig. 5.7(a), (b).

![Fig: 5.6 Unregulated secondary-1 output for increase in (a) load-1 current (b) load-2 current](image)

The secondary-3 output voltage is regulated under the load variation of both secondary-1 and 2 with the feedback loop as noticed in
Fig. 5.8(a) and (b). This effect depends on the load resistance, leakage inductance and losses of transformer, which in turn affects the converter range of operation.

![Waveform](image1)

![Waveform](image2)

Fig: 5.7 Unregulated secondary-2 output for increase in (a) load-1 current (b) load-2 current

For the secondary-2 output the same analysis is carried out under load variation 100mA to 300mA and the corresponding waveforms are as shown in Fig. 5.6(b), Fig. 5.7(b) and Fig. 5.8(b). From Fig. 5.8 it is observed that secondary-3 output voltage is regulated for increase in load-1 and load-2. Similarly, the effects for load change of 300mA to 100mA in load-2 were also observed to have the same effects in all the other outputs.

![Waveform](image3)

![Waveform](image4)

Fig: 5.8 Regulated secondary-3 output for increase in (a) load-1 current (b) load-2 current
5.3.3.2 Line transients

Fig. 5.9(a), (b) and (c) shows the waveforms of unregulated secondary-1 output, secondary-2 output and regulated secondary-3 output with respect to increase in input supply from (28V to 42V).

Similarly, the waveforms of unregulated secondary-1 output voltage, secondary-2 output voltage and regulated secondary-3 output voltage with respect to the decrease in input supply is also observed to have the same effects.

5.3.3.3 Inference

Efficiency analysis of the designed converter for both load variation and line variation was carried out and it was observed that maximum efficiency is obtained at 2.5A under load variation; also the converter efficiency (equation 4.8) reaches 72% under line variation. From the hardware responses the average input voltage and current obtained are 42.3V, 1.22A, the average output voltage 1 ($V_{o1}$) and output current 1
(I_{o1}) are 6.56V and 5.03A and similarly average output voltage 2 (V_{o2}) and output current 2 (I_{o2}) are 13.9V and 0.3A.

From equation 4.8, Efficiency = \frac{\text{Output power (V_{oavg} I_{oavg})}}{\text{Input power (V_{inavg} I_{inavg})}} \times 100\% \\
= \sum_{k=0}^{n} \frac{V_{okavg} I_{okavg}}{(V_{inavg} I_{inavg})} \times 100\% \\
= \frac{37.1668}{51.606} \times 100\% = 72\% 

Secondary-3 output is fed back to the controller IC UC1825 for regulation as it is the power supply for the controller. The other two un regulated outputs can be used for applications like CMOS circuits and for motors used in robotic arms since these applications have ripple tolerance and precision is not a must. For applications where precision is a must (TTL logic circuits) these two unregulated outputs can be regulated by LDO post regulators and the implementation of the same for one of the output is discussed in the next section. Moreover, the cross regulation effects discussed in Fig. 5.6, 5.7 and 5.9 can be reduced by improving the coupling in the multi-output transformer and by reducing the transformer leakage inductance.

5.3.4 LDO Post Regulator

Linear voltage regulators are an important resource to power supply designers. Three terminal fixed-voltage linear regulators are widely used as ‘spot’ regulators and as post-regulation stages fed by
SMPS. They are inexpensive and simple to use, but have several performance limitations. Three terminal regulators are inefficient power converters and most monolithic regulators require an input-to-output voltage differential of at least 2 to 3V. Low drop out post regulator design is discussed in this section.

5.3.4.1 Post Regulator Controller UC1834

The UC 1834 is a programmable linear regulator control IC using which both positive and negative voltage are regulated. The output voltage and the reference voltage from LDO post regulator are compared in an error amplifier (pin 8 and 9). The circuit diagram of LDO post regulator is shown in Fig. 5.10.

![Circuit diagram of LDO post regulator](image)

Fig: 5.10 Circuit diagram of LDO post regulator

By using a voltage divider circuit ($R_3 = 1\,k\Omega$, $R_4 = 3.3\,k\Omega$, $R_5 = 3.8\,k\Omega$), the output voltage is reduced to 1.5V and is fed to the non-inverting terminal of the error amplifier. Reference voltage of 1.5V is fed from the third pin of the IC. The inverting terminal of IC is fed back with
this reference value. When Q1 (PNP 2N3019) is operated near saturation, error amplifier allows good dynamic regulation.

5.3.4.2 Load transients

Cross regulation effect is more in secondary-2 with respect to the load change in secondary-1. Hence, a LDO post regulator UC1834 is implemented to regulate the high power auxiliary output (+5V/5A) of the converter. Fig. 5.11(a & e) shows the waveforms of regulated secondary-1 & 3 output voltage with respect to increase in load change from 300mA to 5A in load-1 (17Ω to 1Ω) and vice versa in Fig. 5.11(b & f).
Fig: 5.11 Regulated secondary-1 & 3 output for (a & e) load-1 current increase  (b & f) load-1 current decrease; (c & g) load-2 current increase (d & h) load-2 current decrease.

Similarly, Fig.5.11(c & g) shows the regulated secondary-1 & 3 output voltage with respect to increase in load change from 100mA to 300mA in load-2 (150Ω to 50Ω) and vice versa in Fig. 5.11(d & h). As seen from Fig. 5.12(a) – (d), the unregulated secondary-2 output voltage
variation is less than 2.5V (within permissible limit considered as per the specifications).

### 5.3.4.3 Line transients

Fig. 5.13(a), Fig. 5.14(a) and Fig. 5.15(a) shows the waveforms of regulated secondary-1 output voltage, unregulated secondary-2 output voltage and regulated secondary-3 output voltage, with respect to increase in input supply from (28V to 42V). Likewise, Fig. 5.13(b), Fig. 5.14(b) and Fig. 5.15(b) show the waveforms for decrease in input supply from (42V to 28V).

**Fig: 5.13** Regulated secondary-1 output for input supply voltage
(a) increase (b) decrease

**Fig: 5.14** Unregulated secondary-2 output for input supply voltage
(a) increase (b) decrease
5.3.4.4 Analysis

A SMPS with lower output voltage ripple is designed for Telemetry transmitter application. Fig. 5.16(a) shows the waveform confirming that the output ripple is 88mV, which is greater by 30mV from the specification. To reduce this to the standard ripple voltage level of 50mV used in military avionics (tabulated in table 3.4), output filter is added at the regulated output port. Fig. 5.16(b) shows the hardware implementation of the converter.

To ascertain Load Regulation, load changes are applied. For a constant input voltage of 34V, load-1 is varied from 300mA to 5A and for
load-2 from 100mA to 300mA. In all these cases it is observed that the output voltage is regulated. The regulation for 70% to 100% load variations is calculated to be 1.12% to 0.31% in load-1 and 0.415% to 0.33% in load-2. The same analysis is carried out for Line regulation. Line voltage is varied from 28V to 42V with all loads maintained at rated conditions. Observations for both increase and decrease in line voltage verified the regulation to be 0.038% for load-1 and 2.27% for load-2, that is, they lie within the specification of ±5% of each output voltage. These calculated values of regulation in load-1 and load-2 are within the standard power supply specification (load regulation: 1.23% and line regulation: 0.826%) as given in table 3.4. The efficiency of the converter with LDO regulator circuit is 86% at rated load conditions.

### 5.4 Single output ZVS PWM Flyback Converter

To reduce the switching losses in hard switched converters at high switching frequencies, single output ZVS flyback converter is built with resonance introduced in the primary circuit. The converter design, modes of operation, simulation and hardware implementation details are discussed in this section.

#### 5.4.1 Principle of Operation

Circuit diagram of the ZVS flyback converter, shown in Fig. 5.17, is a modified version of the basic flyback converter depicted in Fig. 5.1.
Switch \(S_m\), diode \(D_1\), isolated transformer and output filter capacitor \(C_o\) form the basic conventional flyback converter part.

![Circuit diagram of ZVS PWM flyback DC-DC converter.](image)

The ZVS section added to this basic converter has two auxiliary diodes (\(D_2\) and \(D_3\)), resonant inductor \(L_r\), resonant capacitor \(C_r\), and auxiliary switch \(S_a\), as depicted by the dotted line in the Fig. 5.17. The working of the converter is discussed in detail in the following section.

### 5.4.2 Modes of Operation

To analyse the operation of the converter for one full switching cycle the assumptions are made are as stated in section 4.2.2.

The operation of the ZVS flyback converter is explained in the following eight modes for a single switching cycle. The modes of operation are shown in Fig. 5.18(a) – (h) and its corresponding waveforms [70] for all the modes are presented in Fig. 5.19.

\[
V_{cr}(t_0) = V_{cro}, \quad I_{Lr}(t_0) = 0, \quad I_{Lm}(t_0) = I_{Lm0}, \quad I_{Ls}(t_0) = 0.
\]
A. Mode 1

Switch $S_a$ is turned ON at $t = t_0$, ensuring ZCS. This creates a closed path for previously charged resonant capacitor $C_r$ to charge the resonant inductor through $S_a$, $D_3$, $L_r$, $V_{in}$ and $C_r$. This mode continues until the voltage across the resonant capacitor decreases to $V_{in} + nV_o$. 

(a) Mode 1

(b) Mode 2

(c) Mode 3

(d) Mode 4

(e) Mode 5

(f) Mode 6
The energy stored in the magnetising inductance of the transformer in the previous modes is “flied back” to the load during this mode.

B. Mode 2

During this mode, the stored energy in the magnetising inductance \( L_m \) is delivered to the output and hence the voltage across the
magnetising inductance $L_m$ can be viewed as a constant voltage source $nV_0$. Two closed paths are established in this mode; the first closed path is through the outer loop $D_2$, $L_s$, $nV_0$, $C_r$, $V_{in}$ and the second through the $nV_0$, $S_a$, $D_3$, $L_r$, $D_2$ and $L_s$. In this mode, the resonant voltage $V_{Cr}$ decreases and charges both the resonant inductor and leakage inductor and hence the currents ($I_{Lr}$, $I_{Ls}$) increase. When the resonant voltage $V_{Cr}(t)$ becomes zero, the body diode of the switch $S_m$ is turned ON thus ending this mode.

**C. Mode 3**

When the resonant voltage $V_{Cr}$ drops to zero, the body diode of the switch $S_m$ turns ON as confirmed in Fig. 5.18(c), that is, the voltage across the switch $S_m$ is clamped at zero. Switching ON the switch $S_m$ at this instant ensures ZVS of the switch. Due to the voltage $V_{in} + nV_o$, the leakage inductor $L_s$ is linearly charged, current $I_{Ls}$ is linearly increased and the resonant current $I_{Lr}$ linearly discharges through the input voltage. When the resonant current $I_{Lr}$ drops to zero, the diode $D_3$ is turned OFF and ends this mode.

**D. Mode 4**

When the resonant current $I_{Lr}$ drops to zero, the diode $D_3$ is reverse biased, blocking the current through switch $S_a$. When zero current switching occurs, the switch $S_a$ is turned OFF and the leakage inductor current $I_{LS}$ is continuously charged by the source voltage $V_{in}$.
and $nV_o$. The secondary diode continues to be in forward biased condition while the magnetising inductor $L_m$ supplies the output voltage.

**E. Mode 5**

In this mode, the circuit operation is similar to the conventional pulse width modulated flyback DC-DC converter operating at turn ON stage. Because of the input voltage source $V_{in}$, the magnetising inductor $L_m$ and the leakage inductor $L_s$ are linearly charged. Fig. 5.18(e) shows the operation of mode 5.

**F. Mode 6**

During this mode, switch $S_m$ is turned OFF under ZVS by the controller, since voltage across the resonant capacitor is zero and cannot change instantaneously. Because of the charging of the resonant capacitor $C_r$, the resonant voltage $V_{cr}$ increases linearly. When the resonant voltage $V_{cr}$ rises to $V_{in} + nV_o$ the secondary diode $D_1$ is forward biased. Mode 6 operation is shown in Fig. 5.18(f).

**G. Mode 7**

When the diode turns ON, the output voltage is supplied by the magnetising inductor $L_m$. As a result, $nV_o$ equals the voltage across the magnetising inductor $L_m$. The resonant leakage inductor $L_s$ discharges to resonant capacitor $C_r$ through the path $V_{in}$, $L_s$, $L_m$, and $C_r$. This decreases leakage inductor current $I_{Ls}$, while increasing resonant voltage $V_{cr}$. When the current $I_{Ls}$ drops to zero, diode $D_2$ is reverse biased and ends this mode. The resonant capacitor voltage $V_{cr}(t)$ reaches initial condition $V_{cro}$.
H. Mode 8

The mode 8 operation is similar to the operation of a conventional PWM flyback DC-DC converter operating at turn OFF state. The magnetising inductor $L_m$ continuously supplies the output. Both the resonant current $I_{Lr}(t)$ and leakage inductance current $I_{Ls}(t)$ return to zero and the circuit regains its initial state, before the start of the next cycle.

5.4.3 Design

The design procedure of ZVS PWM flyback converter is specified below.

5.4.3.1 Specifications

The specifications chosen for design are as tabulated in Table 5.3.

<table>
<thead>
<tr>
<th>Table 5.3 Electrical Specifications</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Voltage $(12 \pm 10%)$</td>
<td></td>
</tr>
<tr>
<td>Min. $V_{imin}$</td>
<td>10.8V</td>
</tr>
<tr>
<td>Max. $V_{imax}$</td>
<td>13.2 V</td>
</tr>
<tr>
<td>Switching Frequency $f$ (kHz)</td>
<td>50 kHz</td>
</tr>
<tr>
<td>$D_{max}$</td>
<td>47%</td>
</tr>
<tr>
<td>Output Power $P_{out}$ (W)</td>
<td>1.08 W</td>
</tr>
<tr>
<td>Output</td>
<td>-3.3V, -0.33A, 10 Ω</td>
</tr>
</tbody>
</table>

5.4.3.2 Resonant component design

To achieve soft switching of the switches, the design of $L_r$ and $C_r$ are carried out as per ZVS criteria using equations (4.1) – (4.4) and the designed values are:

$$f_r = 200kHz, Z_o = 30, L_r = 25\mu H \text{ and } C_r = 27.77nF$$

Where $f_s/f_r = 0.25 \quad (5.3)$
\( n_L = 2 \) where \( n_L \) is greater than 1

\( n_L = \frac{L_s}{L_r}, L_s = n_L \times L_r = 50 \mu H \)

Core selected for the inductor \( L_r \) is T-12 core with area = \( 0.51890 \text{ mm}^2 \) and SWG = 21.

### 5.4.3.3 Design of Transformer and Filter Capacitor

The design of the transformer is detailed for continuous conduction mode in this section. The design formulae are same as that stated in section 5.3.1.3 and the designed values are:

**Primary current calculation:**

The Primary inductor, \( L_{pri} = 81 \mu H \)

The Primary peak current, \( I_{ppk} = 0.985 \text{ A} \)

The Primary RMS current, \( I_{prms} = 0.675 \text{ A} \)

Primary Turns, \( N_{pri} = 36 \) Turns

**Secondary current calculation:**

Secondary peak current, \( I_{spk} = 1.886 \text{ A} \)

Secondary RMS Current, \( I_{srms} = 1.373 \text{ A} \)

Secondary turns ratio, \( \frac{N_s}{N_{pri}} = 0.54 \)

Secondary turns, \( N_s = 19 \)

**Filter capacitor**

Using equation (5.2), Output filter capacitance \( C_o \) is calculated as 100\( \mu \)F.
5.4.3.4 Open-loop Simulation Results

The open loop simulation of the converter shown in Fig. 5.17 is carried out in PSIM and the results are discussed in this section. Fig 5.20(a) presents the resonant waveforms.

![Resonant waveforms](image)

**Fig: 5.20 (a) Resonant waveforms (b) Output**

It is observed from the waveform that the current $I_{Lr}=0$ when the auxiliary switch is turned ON, thus ensuring ZCS. The voltage across the resonant capacitor ($V_{Cr}$) starts discharging from $V_s+nV_{Co}$ (100V to 0V), meanwhile charging the inductor $I_{Lr}$ to a maximum peak value of 2.9A before switch $S_m$ turns ON. When the main switch is ON, the current in the leakage inductor rises and reaches a peak of 1.9A. It is further observed that the main switch current increases from -2A to 2A when the
switch current is negative during the conduction of the body diode. This ensures zero voltage switching of main switch (when the body diode conducts, the voltage across the switch is zero). The OFF condition of switch $S_a$ also occurs at zero current, thus increasing the efficiency by reducing the switching losses. The output voltage -3.3V and current -0.33A obtained is as revealed in Fig 5.20(b).

**5.4.4 Experimental Results**

The single output ZVS flyback converter is built with designed values using IRF840 power switch and IN5819 diode. These devices are selected with the criteria of least rise and fall time. The pulses for the active devices are generated from an ARM processor. The pulses generated have maximum amplitude of 5V which is insufficient to drive the switches; hence an opto-coupler circuit with TLP250 is designed and built. This circuit served the twin purpose of (1) isolating the two switching pulse (2) amplification of the signal. The pulses at the output terminals of the opto-coupler are displayed in Fig. 5.21(a). It is observed from the waveform that the main switch has 40% pulse width, while that of the auxiliary switch is 20%. The output voltage and current obtained is depicted in Fig. 5.21(b). They were observed to be -3.3V and -0.33A. Fig. 5.21(c) shows the resonant capacitor voltage and switch pulse.
This figure confirms the zero voltage switching of the device. The peak voltage across the resonant capacitor is measured to be 68V from the figure shown.

The voltage and current in the main switch $S_m$, presented in Fig. 5.22(a), is observed as 70V (peak to peak), 475mA (rms). Fig. 5.22(b) shows the auxiliary pulse and resonant inductor current. The peak to peak and rms values of inductor current are 1.8mA and 386mA respectively. The auxiliary switch is turn OFF at ZCS, as observed from the figure. The Experimental prototype developed is displayed in Fig. 5.22(c). From the waveforms of the resonant inductor current, resonant capacitor current and leakage inductor current, the peak values noted are 1.8A, 547mA and 1.94A respectively.
Fig: 5.22 (a) Main switch voltage ($V_{dsm}$) and current ($I_{dm}$) with main switch pulse ($V_{gsm}$) (b) Resonant inductor current ($I_{Lr}$) with auxiliary switch pulse ($V_{gsa}$) (c) Hardware setup for the circuit

Single output converters fail to supply power to more than one load. Since communication systems and aerospace applications have many logic devices, LCDs, amplifiers, tuners, transmitters and receivers which work at different DC voltage levels, there is a need for multi-output converters. This issue is dealt in next section.

5.5 Multi-output ZVS PWM Flyback Converter

The demand for compact multiple output power supplies resulted in reduction of space, increased power density and high efficiency. The detailed design, analysis and implementation of the same are explained in detail in this section.

5.5.1 Principle of Operation

Power stage circuit diagram of the multi-output ZVS PWM flyback DC-DC converter is shown in Fig. 5.23. The circuit is similar to that
explained in section 5.4, except that the output sections are two in number. The elements newly added to the circuit shown in Fig.5.17 are diode $D_{02}$ and output filter capacitors $C_{o2}$, as presented in Fig.5.23.

![Circuit diagram of Multi-output ZVS flyback converter](image)

Fig: 5.23 Circuit diagram of Multi-output ZVS flyback converter

### 5.5.2 Modes of Operation

The multi-output topology works as a cascaded model of single output topology with higher power density, and hence the modes of single output topology hold good for multi-output topology as well. The modes of single output topology are explained in section 5.4.2.

### 5.5.3 Design

The design procedure of multi-output ZVS flyback converter is described below.

#### 5.5.3.1 Specifications

The specifications are similar to the details considered in section 5.4.3.1. The details of the outputs are $V_{o1} = -2.8V$, $I_{o1} = -0.282A$, $V_{o2} = -3.3V$, $I_{o2} = -0.33A$, $P_0 = 1.705W$. 

5.5.3.2 Resonant Component Design

The design of the resonant part in the converter is same as single output ZVS flyback converter, described in section 5.4.3.2.

5.5.3.3 Design of Transformer and filter capacitor

The designed values for the transformer secondary are as follows.

- Secondary-1 peak current, $I_{\text{scr1}} = 1.886A$
- Secondary-1 rms current, $I_{\text{sr1}} = 1.373A$
- Secondary-2 peak current, $I_{\text{scr2}} = 0.55A$
- Secondary-2 rms current, $I_{\text{scr2}} = 0.40A$
- No. of turns in secondary, $N_{s1} = 19$
- No. of turns in secondary, $N_{s2} = 12$
- Selected transformer core is EE 20/10/15
- Output filter capacitance $C_{01} = 100\mu F = C_{02}$.

5.5.4 Simulation Results

The open loop simulation results shown in Fig 5.24(a) reveal that the voltage across the resonant capacitor is greater than the single output topology by 50V, while the resonant inductor current increases by 1A. Similarly, the leakage inductance current is as high as 3A instead of 1.9A in single output topology. The main switch current oscillates between -3A to 3A while that of single output topology oscillates from -2A to 2A. The output voltages (-2.6V, -3.3V) and currents (-0.26A, -0.33A) of the multi-output ZVS flyback converter are obtained as illustrated in Fig. 5.24(b).
From the simulation results of the multi-output converter it is observed that, the resonant capacitor voltage and the current through the switch, leakage inductance current and resonant inductor current have increased, when compared with the single output converter. Moreover, the power handling capability increases, with the space and volume utilised remaining the same as single output topology.

### 5.5.5 Experimental Results

This section deals with the detailing of the experimental results obtained from the prototype developed in Fig. 5.26(c). Fig. 5.25(a), (b) and (c) shows the first output voltage and current (-2.54V, -0.248A), the second output voltage and current (-3.74V, -0.317A) and the obtained resonant capacitor voltage $V_{cr}$ respectively.
It is noticed that when the resonant capacitor voltage becomes zero, the main switch is turned ON and the peak voltage across the resonant capacitor is 62V, as proven in Fig. 5.25(c).

From Fig. 5.26(a) it is observed that the auxiliary switch is turned OFF when the resonant inductor current is zero (ZCS condition). The leakage inductor current with the main switch pulse is presented in Fig. 5.26(b).

The maximum switch voltage obtained is 64V. Switch voltage is less than the hardware result obtained from single output topology.
discussed in section 5.4.4. The peak values of resonant inductor current $I_{lr}$, leakage inductor current, resonant capacitor current and main switch current $I_{sm}$ are 720mA, 3.08A, 442mA and 2.02A respectively.

### 5.5.6 Analysis of the Converter

The voltage conversion ratio $\frac{V_o}{V_{in}}$ versus the duty ratio $D$ for various values of $f_s/f_r$ is shown in Fig. 5.27(a). It is observed from the graph that the converter operates linearly for $f_s/f_r = 0.3$ in the duty ratio of 0.4 to 0.5. Hence, the same is taken while designing the converter parameters. Fig. 5.27(b) shows the efficiency curve of the converter. It is observed that the efficiency is 80% at rated conditions.

![Fig: 5.27](image)

**Fig: 5.27** (a) Conversion ratio $V_o/V_{in}$ against duty cycle $D$ for various $f_s/f_r$  
(b) Efficiency of multi-output flyback converter

### 5.6 Single output voltage doubler ZVS PWM Flyback Converter

The primary resonant converter discussed in the previous two sections does not deal with the switching losses of the passive switches. Voltage doubler introduced in the secondary of the converter not only
reduces the switching losses in the passive switches, but also doubles the output voltage of the converter. In this section - the working, modes of operation, design and open loop simulation of single output voltage doubler ZVS PWM flyback converter is discussed in detail.

**5.6.1 Principle of Operation**

Fig. 5.28 shows the power stage circuit diagram of a single output voltage doubler ZVS PWM flyback DC-DC converter. The circuit has three sections. The first two sections are similar to the one explained in section 5.4.1. The third section is the voltage doubler which consists of a resonant capacitor $C_d$, and rectifier diodes $D_{11}$ and $D_{12}$. The voltage doubler circuit increases the power density of the converter and this, in turn, increases the efficiency of the converter on the whole; thus providing an advantage over single output ZVS flyback topology, discussed in section 4.4.1.

![Fig: 5.28 Circuit diagram of single output voltage doubler ZVS flyback converter](image)
5.6.2 Modes of Operation

The voltage doubler ZVS PWM flyback converter operation for one switching cycle is explained in eight modes of operation, as shown in Fig. 5.29. The theoretical waveform of the circuit is illustrated in Fig. 5.30.

A. Mode 1

During the initial condition $t = t_0$, the switches $S_m$ and $S_a$ are in OFF state. Mode 1 operation starts at $t = t_0$ when $S_a$ is turned ON at ZCS. As shown in Fig. 5.29(a), the resonant capacitor discharges through $V_{in}$, $C_r$, $S_a$, $D_3$, and $L_r$. As a result, the resonant capacitor voltage $V_{cr}(t)$ decreases and the resonant current $I_{Lr}(t)$ increases. Mode 1 ends when the resonant voltage $V_{cr}(t)$ reduces to $V_{in} + nV_o$, and the diode $D_2$ is forward biased and starts conducting. The output power is supplied by the magnetising inductance $L_m$. Diode $D_{11}$ is reverse biased and current flows through diode $D_{12}$ which is forward biased.

B. Mode 2

Energy stored in the magnetising inductor $L_m$ supplies the output continuously. The diode $D_{12}$ conducts and charges the output capacitor $C_o$ thus obtaining the output voltage. Voltage across the magnetising inductor $L_m$ is $nV_o$, which remains constant. The first closed path is through the outer loop $D_2$, $L_s$, $nV_0$, $C_r$, $V_{in}$ and the second is through $nV_0$, $S_a$, $D_3$ and $L_r$, $D_2$, $L_s$. Resonant voltage $V_{cr}$ decreases, resonant current $I_{Lr}$ charges and leakage inductor current $I_{Ls}$ increases. This mode ends by
naturally turning ON the body diode of switch $S_m$ as resonant voltage $V_{cr}(t)$ drops to zero.

**C. Mode 3**

Zero voltage switching occurs in $S_m$ when the voltage across the switch is clamped at zero by its body diode. For this, the switch is turned ON at that particular instant. The leakage inductor $L_s$ is linearly charged by voltage source $V_{in}$ and $nV_o$, while current $I_{Ls}$ linearly increases. The resonant inductor $L_r$ discharges linearly through the input voltage source $V_{in}$ and its current $I_{Lr}$ decreases linearly.

![Mode 1](image1)

(a) Mode 1

![Mode 2](image2)

(b) Mode 2

![Mode 3](image3)

(c) Mode 3

![Mode 4](image4)

(d) Mode 4
Fig 5.29 Equivalent circuits of Voltage doubler ZVS PWM flyback converter

Fig 5.30 Theoretical waveform of the Voltage doubler ZVS PWM flyback converter
As the resonant current $I_{Lr}$ drops to zero, diode $D_4$ gets reverse biased. Diode $D_{12}$ is reverse biased, diode $D_{11}$ is forward biased and the output resonant capacitor $C_d$ charges through it.

**D. Mode 4**

Fig. 5.29(d) shows the operation during mode 4. When the resonant current $I_{Lr}$ drops to zero, diode $D_4$ blocks the discharging path of resonant inductor $L_r$ to the input voltage source $V_{in}$, thus $S_a$ stops conducting at zero current. The voltage source $V_{in} + nV_o$ continuously charges the current $I_{Ls}$ in the leakage inductor $L_s$. The capacitor $C_d$ charges in this mode through the forward biased diode $D_{11}$. The output voltage is supplied by filter capacitor $C_0$.

**E. Mode 5**

In this mode, the working of the primary circuit is similar to the conventional PWM flyback DC-DC converter working in ON state. The input source voltage $V_{in}$ linearly charges the magnetising inductor $L_m$ and the leakage inductor $L_s$. Rectifier diode $D_{11}$ is reverse biased while diode $D_{12}$ is forward biased. Current flows through diode $D_{12}$ to the load from the secondary winding.

**F. Mode 6**

The voltage across the resonant capacitor cannot change instantly and so the voltage across the switch $S_m$ is equal to zero and can be
turned OFF under ZVS by the controller. Resonant capacitor $C_r$ charges linearly, increasing its resonant voltage $V_{cr}$ to $V_{in} + nV_o$. Output voltage is supplied by diode $D_{12}$.

**G. Mode 7**

Voltage across the magnetising inductor $L_m$ equals $nV_o$. The resonance of the leakage inductor $L_s$ and the resonant capacitor $C_r$ start through $V_{in}$, $L_s$, $L_m$, and $C_r$. The current $I_{Ls}$ in the leakage inductor $L_s$ decreases and the resonant voltage $V_{cr}$ increases to the initial voltage condition $V_{cro}$. Working of the secondary side is similar to that of the previous mode. This mode ends when the current $I_{Ls}$ drops to zero, reverse biasing diode $D_2$.

**H. Mode 8**

Working of this mode is similar to a conventional PWM flyback DC-DC converter operating at turn OFF state. The magnetising inductor $L_m$ continuously supplies the output as in the previous mode. Circuit operation returns to initial state by the end of this mode. The resonant voltage $V_{cr}(t)$ returns to initial value $V_{cro}$ and both the resonant current $i_{Lr}(t)$ and $i_{Ls}(t)$ return to zero.

**5.6.3 Design**

The design of the converter is same as explained for single output topology in section 5.4.3. But, the output voltage is increased with the
help of output resonant capacitor $C_d$ and rectifier diodes $D_{11}$ and $D_{12}$.

The increased output voltage and current are:

- Output voltage, $V_o = -5V$
- Output current, $I_o = -0.5A$
- Output power, $P_o = 2.5W$

Output resonant capacitor, $C_d \geq \frac{4(\pi n_s^2 D T_s)^2}{L_s} = 1000nF$ \hspace{1cm} (5.4)

where, $n_s$ is the turns ratio, $D$ is the duty cycle, $T_s$ is the total time period and $L_s$ is the leakage inductance.

### 5.6.4 Open-loop Simulation Results

The voltage doubler ZVS flyback converter is simulated in PSIM and the resonant waveform obtained is presented in Fig. 5.31(a). The resonant waveforms are similar to the waveforms of single and multi-output topologies and the values observed from the waveform are $V_{Cr-pk} = 50V$, $I_{Lr-pk} = 1.2A$, $I_{Ls-pk} = 1.5A$, $I_{switch-pk} = 1.9A$.

The values are observed to be lesser than the single output topology for the same specification. The peak amplitude of the secondary elements added to obtain voltage doubling effect are $V_{D_{11}-pk} = +2.5V$, $V_{D_{12}-pk} = 1.5V$, $V_{cd-pk} = 10V$. Fig. 5.31(b) depicts the output voltage and current obtained (-5V and -0.5A), which is 1.5 times the output obtained from single output topology.
5.6.5 Experimental Results

The hardware prototype of the single output ZVS PWM voltage doubled flyback converter developed is displayed in Fig. 5.33(c). Fig. 5.32(b) shows the resonant capacitor voltage $V_{Cr}$, current $I_{Cr}$ and Fig. 5.32(a) depicts the output -5.68V and -0.568A. The peak voltage across the resonant capacitor is 78V and when the resonant capacitor voltage becomes zero the main switch is turned ON. In Fig. 5.32(c) it is observed that the resonant current starts rising when auxiliary switches are turned ON, that is, at ZCS condition the auxiliary switch is turned ON and the same is observed at turn OFF also.
Fig: 5.32 (a) Output voltage and current (b) Resonant capacitor voltage ($V_{cr}$) and current ($I_{cr}$) with main switch pulse ($V_{gsm}$) (c) Resonant inductor current ($I_{Lr}$) with auxiliary switch pulse ($V_{gsa}$)

The main switch voltage, current and leakage inductor current are presented in Fig. 5.33(a) and (b) with main switch pulse. From the hardware waveform it is observed that resonant capacitor voltage obtained is 78V which is significantly higher than the 60V obtained from the single output model. The peak values of main switch current and resonant inductor current are 1.94A and 1.72A respectively.

Fig: 5.33 (a) Main switch voltage ($V_{dsm}$), and current ($I_{dm}$) with main switch pulse ($V_{gsm}$) (b) Leakage inductor current ($I_{Ls}$) with main switch pulse ($V_{gsm}$) (c) Hardware setup
The drawbacks of single output topology specified in section 5.4 is applicable for single output voltage doubler circuit also. This issue is addressed by multi-output converter in the next section.

5.7 Multi-output Voltage doubler ZVS PWM Flyback Converter

The most important advantage of multi-output voltage doubler ZVS flyback converter are the isolated multiple outputs obtained from the same sized converter with doubled output voltages. Instead of using two single SMPS, this converter would be a better option in terms of space utilization, power density and efficiency. This multi-output converter with primary and secondary resonance exhibit further advantages like lower switching losses in active and passive switches, high power density and low volume requirement, etc.

In this section, the circuit diagram of multi-output voltage doubler ZVS flyback DC-DC converter, simulation and hardware results are discussed in detail.

5.7.1 Principle of Operation

Fig. 5.34 shows the power stage circuit diagram of the multi-output voltage doubler ZVS flyback DC-DC converter. This circuit is similar to the circuit explained in the previous section but with additional devices like resonant capacitors $C_{d1}$ and $C_{d2}$, rectifier diodes $D_{11}, D_{12}, D_{21}, D_{22}$ and filter capacitors $C_{o1}, C_{o2}$.
The advantage of a voltage doubler circuit is that the power handling capacity of the converter is increased, diode losses and voltage stress are decreased and so it has better efficiency than the other four flyback converters explained in sections 5.3, 5.4, 5.5 and 5.6.

5.7.2 Modes of Operation

The multi-output topology works as a cascaded model with higher power density and hence the modes of multi-output voltage doubler topology are same as the modes of single output voltage doubler topology explained in section 5.6.2.

5.7.3 Design

The design of the resonant part of the converter is same as single output ZVS PWM flyback converter explained in section 5.4.3. The design of the secondary side of the converter is same as single output voltage
doubler and multi-output ZVS PWM flyback converter discussed in section 5.6.3 and 5.5.3 for outputs of -3.3V, -0.33A and -5V and -0.5A.

5.7.4 Open-loop Simulation Results

The simulation results are shown in Fig. 5.35(a) and (b). The values observed from the figures are \( i_{Lr-pk} = 4.2A, I_{Ls-pk} = 6A, i_{sw-pk} = 6A, V_{Cr-pk} = 150V, i_{D11-pk} = -5A, i_{D12-pk} = -3A, V_{Cd-pk} = 20V, V_{01} = -3.3V, I_{01} = -0.3A, V_{02} = -5A, I_{02} = -0.5A. \) The voltage across the capacitor is thrice that of the single output voltage doubler topology. Similarly, the current and voltage across the devices are of higher magnitude when compared with the single output voltage doubler topology.

![Resonant waveforms](image)

![Output currents and output voltages](image)

**Fig: 5.35 (a) Resonant waveforms (b) Output currents and output voltages**

5.7.5 Open Loop Hardware Results

The outputs \((-3.52V, -0.392A)\) and \((-5V, -0.5A)\) obtained from the hardware prototype are as shown in Fig. 5.36(a) and (b). The resonant
waveforms are similar to the waveforms obtained from the single output topology (with and without voltage doubler) and the multi-output topology. The ZVS and ZCS condition achieved are presented in Fig. 5.36(c) and 5.37(a) respectively.

The peak values obtained in the devices are $V_{Cr-pk} = 82V$, $i_{Lr-pk} = 720mA$, $I_{Ls-pk} = 3.06A$, $V_{dsmpk} = 84V$, $i_{Lam-pk} = 432mA$, $V_{Cdpk} = 12.4V$, $I_{Cd-pk} = 1.58A$, $V_{D11-pk} = 7V$, $I_{D11-pk} = 674mA$, $V_{D12-pk} = 7.4V$, $I_{D12-pk} = 654mA$. The hardware prototype is displayed in Fig. 5.38.
The difference in voltage and current magnitude across the capacitors and diodes in simulation (section 5.7.4) and hardware (section 5.7.5) is due to the fact that the devices and capacitors used in the simulation are ideal (i.e) ON state resistance of devices, ESR and ESL in capacitors are not considered in simulation.

**5.7.6 Closed Loop Implementation Using Analog Controller IC SG3525**

Simulation is carried out to study the closed loop response of the PI controlled converter. The simulation circuit and its closed loop response are as shown in Fig. 5.39(a) and (b). In spite of load variations the output is regulated 5V. Hence to implement the same in hardware a generic and readily available laboratory purpose analog controller IC SG3525 is used. The hardware circuit of the PI controller implemented with IC SG3525 is shown in Fig. 5.39(c). The design and implementation details are same as that explained in section 4.6.6.2. The regulated outputs are dealt in sections 5.7.6.4 – 5.7.6.5 in detail.
Fig: 5.39 (a) Closed loop PI simulation circuit (b) Closed loop output voltage and current (c) Implementation of Hardware circuit.

5.7.6.1 Line transients

The line voltage is varied for ±20% and Fig. 5.40(a) and (b) shows the effect of output voltage-1 and 2 for increase and decrease in supply voltage. It is observed that the output voltage-1 increases to 5.6V for an increase in supply in Fig. 5.40(a). Similarly the output voltage-1 decreases to 2V for decrease in supply in Fig. 5.40(b). Fig. 5.41(a) and (b)
shows the effect of output-2 voltage and current for increase and decrease in supply voltage. The regulated output voltage-2 is observed to be regulated within ±2% for both increase and decrease in supply voltage. The regulation percentage obtained can be reduced to <0.5% when the converter is ringed up in a PCB board and by reducing the length of the wires used between the connections. While the increase and decrease in supply voltage is reflected in increase and decrease in magnitude of the load current respectively.

![Figure 5.40 Output voltages for (a) increase in supply (b) decrease in supply voltage](image)

![Figure 5.41 Regulated output voltage and current (V_o2, I_o2) for line voltage (a) increases (b) decreases](image)

### 5.7.6.2 Load transients

Fig. 5.42(a) and (b) shows the effect on output voltages for increase and decrease in load-1. It is observed from Fig. 5.42(a) that the output
voltage-1 is increased to 6V for an increase in load of 20%. Similarly the decreasing effect is observed in Fig. 5.42(b) for decrease in load also. Fig. 5.42(a) and (b) further confirms that the output voltage-2 is regulated at 5V for the load variation of ±20%. Fig. 5.43(a) and (b) shows the effect on output-1 and 2 for increase in load-2. Output voltage-1 is decreased to 2V while output voltage-2 is regulated at 5V for ±20% variation in load-2. From these evaluations it is determined that the output voltage-2 is regulated for ±20% variation in both line and load variation.

![Fig: 5.42 Output voltages when R₀₁ is (a) increased (b) decreased](image1)

![Fig: 5.43 Load variations in R₀₂ (a) V₀₁, I₀₁ (b) V₀₂, I₀₂](image2)

### 5.7.6.3 Analysis

Fig. 5.44(a) shows the efficiency curve of the multi-output ZVS flyback converter with voltage doubler. The efficiency of the converter is 88% which is higher than that of the single output voltage. The hardware
prototype is shown in Fig. 5.44(b). The efficiency of single output and multi-output ZVS flyback converter with and without voltage doubler are compared in Table 5.4.

![Efficiency curve for multi-output voltage doubler converter from close loop](image1.png)

![Hardware prototype](image2.png)

**Fig: 5.44 (a) Efficiency curve for multi-output voltage doubler converter from close loop (b) Hardware prototype**

**Table 5.4 Efficiency comparison**

<table>
<thead>
<tr>
<th>Type of converter</th>
<th>Flyback auxiliary ZVS</th>
<th>Flyback auxiliary ZVS VD</th>
<th>Flyback auxiliary ZVS MO</th>
<th>Flyback auxiliary ZVS MO VD</th>
</tr>
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<tr>
<td>Hard switched MO Flyback</td>
<td>72%</td>
<td>75%</td>
<td>78%</td>
<td>80%</td>
</tr>
</tbody>
</table>

**Table 5.5 Performance Analysis**

<table>
<thead>
<tr>
<th>Type of losses (W)</th>
<th>Flyback auxiliary ZVS</th>
<th>Flyback auxiliary ZVS VD</th>
<th>Flyback auxiliary ZVS MO</th>
<th>Flyback auxiliary ZVS MO VD</th>
</tr>
</thead>
<tbody>
<tr>
<td>Parasitic C Losses = 0.5 * Cout * ( V_{IN}^2 * f_s )</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Switch S1</td>
<td>1.44*10^{-3}</td>
<td>1.44*10^{-3}</td>
<td>1.44*10^{-3}</td>
<td>1.44*10^{-3}</td>
</tr>
<tr>
<td>Switch S2</td>
<td>1.44*10^{-3}</td>
<td>1.44*10^{-3}</td>
<td>1.44*10^{-3}</td>
<td>1.44*10^{-3}</td>
</tr>
<tr>
<td>ON state losses = ( I_{S,Avg}^2 * R_{DS} ); ( R_{DS} = 0.85 \Omega )</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S1</td>
<td>0.0236</td>
<td>0.06659</td>
<td>0.04152</td>
<td>0.01521</td>
</tr>
<tr>
<td>S2</td>
<td>2.693*10^{-5}</td>
<td>5.44*10^{-5}</td>
<td>7.525*10^{-5}</td>
<td>5.44*10^{-5}</td>
</tr>
<tr>
<td>Diode conduction losses = ( I_{D,avg} * V_D ); ( V_D = 0.8 \text{ V} )</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>D1</td>
<td>0.11</td>
<td>0.212</td>
<td>0.11256</td>
<td>0.13584</td>
</tr>
<tr>
<td>D2</td>
<td>0.1</td>
<td>0.2164</td>
<td>0.11244</td>
<td>0.14256</td>
</tr>
<tr>
<td>D3 &amp;/ D4</td>
<td>0.1</td>
<td>0.2342</td>
<td>0.12</td>
<td>0.22</td>
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</tbody>
</table>
From the table it is observed that multi-output ZVS topology with voltage double has greater efficiency than the other topologies compared. Table 5.5 presents the switching losses and switch stress. From the table it is clear that multi-output ZVS topology with voltage double has less switch stress and switching losses when compared with other topologies.

### 5.8 Conclusion

The principle of operation, design procedure, modes of operation, simulation and experimental results are discussed in detail for hard switched flyback, primary ZVS (single output and multi-output) and output voltage doubler (single output and multi-output).

The control logic and implementation of the same in the converters are also dealt with. It is observed that the primary ZVS multi-output flyback converter with output voltage doubler yields a higher efficiency of 88%. The converter further has the advantage of compactness, lower switching losses and isolated multiple outputs. The efficiency can be increased further if the voltage stress across the ZVS switches is reduced. This issue is dealt in the next chapter with active clamp circuits.