CHAPTER - 3

8085 MICROPROCESSOR AND INTERFACING WITH THE PERIPHERALS
3.1 MICROPROCESSOR ARCHITECTURE

The microprocessor is a programmable logic device designed with registers, flip-flops and timing elements. The microprocessor has a set of instructions designed internally, to manipulate data and communicate with peripherals. This process of data manipulation and communication is determined by the logic design of the microprocessor, called the architecture. The microprocessor consists of the central processing unit, which contains an arithmetic logic unit, appropriate registers and control circuitry. Figure (3.1) illustrates the typical interconnections between building blocks of the microprocessor.

Intel 8085 is an 8-bit, NMOS microprocessor. It is a 40 pin I.C package fabricated on a single LSI chip. The Intel 8085 uses a single +5V d.c supply for its operation. Its clock speed is about 3 MHz. The clock cycle is of 320ns. It has 80 basic instructions and 246 opcodes. Figure(3.2) shows the functional block diagram of Intel 8085.

The 8085 contains a register array of

(i) 16-bit program counter which contains the memory address of the next instruction.

(ii) The 16-bit stack pointer to maintain a pushdown stack any where in memory.
FIG 3.1: TYPICAL INTERCONNECTION BETWEEN THE BUILDING BLOCKS OF MICRO PROCESSOR
FIG 3.2: FUNCTIONAL BLOCK DIAGRAM OF INTEL 8085A
(iii) Six 8-bit registers designated as B, C, D, E, H and L which can be used individually or in pairs. The permitted pairs are BC, DE and HL only.

(iv) 8-bit Accumulator register in which always one of the operand is stored.

(v) Five 1-bit flags namely Carry(CY), Zero(Z), Sign(S), Parity(P) and Auxiliary Carry(AC).

(vi) Two temporary registers which are not program addressable and are used only for internal execution of instructions.

3.1.1 ARITHMETIC LOGIC UNIT

The Arithmetic Logic Unit (ALU) performs arithmetic operations such as addition and subtraction of 8-bit operands together with logical operations such as AND, Exclusive OR etc. The operations such as multiplication and division are performed only by software. The result of an ALU operation is usually transferred to the accumulator. Associated with the execution of arithmetic and logical instructions in the ALU are five conditional flags. They are Zero, Sign, Parity, Carry and Auxiliary Carry. Each are represented by a 1-bit register in CPU.

ZERO (Z) : The zero status flag Z is set to '1', if the result of an arithmetic or logical operation is zero. For non-zero result, it is set to '0'.
PARITY (P) : The parity status flag is set to '1' when the result of the operation contains even number of 1s. It is set to zero when there is odd number of 1s.

CARRY (CS) : The carry status flag holds carry out of the most significant bit resulting from the execution of an arithmetic operation. If there is a carry from addition or a borrow from subtraction or comparison, the carry flag CY is set to 1, otherwise 0.

AUXILIARY CARRY (AC) : The auxiliary carry status flag holds carry out of bit 3 to 4 resulting from the execution of an arithmetic operation.

3.1.2 TIMING AND CONTROL UNIT

The timing and control unit is a section of the CPU. It generates timing and control signals which are necessary for the execution of instructions. It controls data flow between CPU and peripherals. It provides status, control and timing signals which are required for the operation of memory and I/O devices. It controls the entire operations of the microprocessor and peripherals connected to it. Thus it is seen that control unit of the CPU acts as the brain of the computer system.

3.2 VARIOUS SIGNALS OF 8085

Figure(3.3) shows the schematic diagram of Intel 8085. All the signals of 8085 microprocessor can be classified into six groups.

a. Address bus
FIG 3.3 : SCHEMATIC DIAGRAM OF INTEL 8085A
b. Multiplexed address/Data bus
c. Control and Status signals
d. Power supply and frequency signals
e. Interrupts and peripheral initiated signals and
f. Serial I/O ports.

(a) ADDRESS BUS : [A0 - A15]

The address bus is a group of sixteen lines i.e A0-A15. The address bus is unidirectional, i.e bits flow in one direction from the MPU to peripheral devices and used as the high order address bus. The microprocessing unit (MPU) uses the address bus to perform the first function i.e identifying a peripheral over the address bus, the microprocessor transmits the address of that devices which it desires to access.

(b) MULTIPLEXED ADDRESS / DATA BUS : [AD0 - AD7] The signal lines AD7-AD0 are bidirectional, they serve a dual purpose. They are used for the least significant 8-bits of the memory address or I/O address during the first clock cycle of a machine cycle. Again they are used for data during second and third clock cycles.

(c) CONTROL AND STATUS SIGNALS:

ALE: It is an Address Latch Enable signal. It goes high during first clock cycle of a machine cycle and enables the lower 8-bits of the address to be latched either into the memory or external latch.
IO/M: It is a status signal which distinguishes whether the address is for memory or I/O. When it goes high the address on the address bus is for I/O devices. When it goes low the address on the address bus is for the memory.

SO, SI: These are status signals sent by the microprocessor to distinguish the various types of operations such as instruction fetching, halt, reading or writing.

RD: It is a signal to control READ operation. When it goes low the selected memory or I/O device is read.

WR: It is a signal to control WRITE operation. When it goes low the data on the data bus is written into the selected memory or I/O location.

(d) POWER SUPPLY AND CLOCK FREQUENCY: The power supply and frequency signals are as follows:
Vcc: +5v power supply
Vss: Ground Reference
X1,X2: A crystal is connected at these two pins. The frequency is internally divided by two, therefore, to operate a system at 3MHZ the crystal should have frequency of 6MHZ.

CLK OUT: This signal can be used as the system clock for other devices.

(e) INTERRUPTS AND PERIPHERAL INITIATED SIGNALS:
The 8085 has five interrupt signals that can be used to interrupt a program execution.
The microprocessor acknowledges Interrupt Request by INTA signal. In addition to Interrupts, there are three externally initiated signals namely RESET, HOLD and READY. To respond to HOLD request, it has one signal called HLDA.

**INTR**: It is an interrupt request signal. When it goes high the program counter does not increment its content. The microprocessor suspends its normal sequence of instructions. It has the lowest priority.

**INTA**: It is an interrupt acknowledgment sent by the microprocessor after INTR is received.

**RESET IN**: When the signal on this pin goes low, the program counter is set to zero, the buses are tristated and the MPU is reset.

**RESET OUT**: This signal indicates that the MPU is being reset. The signal can be used to reset other devices.

**HOLD**: It indicates that another device is requesting the use of the address and data bus. Having received HOLD request the microprocessor relinquishes the use of the buses as soon as the current machine cycle is completed. Internal processing may continue. The processor regains the bus after the removal of the HOLD signal.
HLDA: It is a signal which indicates that the hold request has been received after the removal of a HOLD request, the HLDA goes low.

READY: It is used by the microprocessor to sense whether a peripheral is ready to transfer data or not. If READY is high, the peripheral is ready. If it is low, the microprocessor waits till it goes high. It is useful for interfacing low speed devices.

(f) SERIAL I/O PORTS: The 8085 has two signals to implement the serial transmission.

SID AND SOD: SID is a data line for serial input where as SOD is a data line for serial output. Serial transfer of data is transmitted bit by bit on a single line. This minimizes the interconnecting wires, thereby also reducing the number of line drivers and receivers.

3.3 INTEL 8085 INSTRUCTIONS

An instruction is a command given to the computer to perform a specified operation on given data. The instructions of 8085 have been classified as

1. DATA TRANSFER GROUP
2. ARITHMETIC GROUP
3. LOGICAL GROUP
4. BRANCH CONTROL GROUP
5. STACK I/O AND MACHINE CONTROL GROUP

(1) DATA TRANSFER GROUP: The transfer of data may be internally within the microprocessor chip, between the
memory and CPU or between different locations in the memory. The instructions must specify the direction of transfer in each case i.e; each instruction must identify the origination source and the final destination to which it must be transferred. Egs are: MOV, MVI, LXI, LDA, STA etc.

(2) ARITHMETIC GROUP: The instructions of this group perform arithmetic operations such as addition, subtraction, increment or decrement of the content of a register or memory. Egs are: AND, SUB, INR, DAD etc. In most cases one operand and the other is in the accumulator.

(3) LOGICAL GROUP: These instructions perform logical operations such as AND, OR, XOR, compare, rotate etc. The logic instructions perform a bit by bit boolean operations between two operands. One of the operand is in accumulator.

(4) BRANCH CONTROL GROUP: Decisions and branching are performed in the CPU by transfer of control instructions. These instructions could be either conditional or unconditional. Egs are: JMP, JC, JZ, CALL etc.

(5) STACK I/O AND MACHINE CONTROL GROUP: This group includes the instructions for input/output ports, stack and machine control. Egs are: IN, OUT, PUSH, POP, HLT etc.

3.4 TIMING AND MACHINE CYCLES OF 8085

When microprocessor is switched 'ON' and given some instructions, the instructions are stored in the memory
which is connected to the microprocessor. From the memory it fetches one instruction at a time and executes. Thus fetching and executing is repeated until it is given HLT instruction. The fetch operation is performed in fixed time slot and execute operation in variable time slot depending upon the instruction to be executed. The total time required to perform these two operations is known as INSTRUCTION CYCLE. So an INSTRUCTION CYCLE is a combination of both FETCH CYCLE and EXECUTE CYCLE as shown in the figure(3.4).

**FETCH CYCLE:** The time taken by the microprocessor to fetch the data from the memory is known as fetch cycle, and it is described by the following algorithm.

```
" begin
    send the address of the next instruction to memory;
    receive the instruction from the memory;
end"
```

when the fetch cycle starts the contents of the program counter are sent to the memory. The memory responds by reading the contents of the received address and transfers them to the microprocessor. Hence one clock cycle is required to send the address, two clock cycles for reading the instruction and transfer it to the microprocessor as shown in figure(3.5). In some cases the access time of the memory may be more than two clock cycles. So the microprocessor has to wait for more than two cycles before it receives the instruction operation code.
ETCH, EXECUTE AND INSTRUCTION CYCLES

FIG 3.4: FETCH, EXECUTE AND INSTRUCTION CYCLES

FETCH CYCLE
EXECUTE CYCLE
INSTRUCTION CYCLE

TIME ---

IDEAL CLOCK

1 C
FC
EC
IC
Fig 3.5: A Typical Fetch Cycle

- Receive Instruction from Memory
- Read Instruction from a Memory Location
- Send Address to Memory
- Transfer Instruction to Up

Ideal Clock
EXECUTE CYCLE: The time slot to execute the instruction by the microprocessor is known as execute cycle and it may be described by the following algorithm:

"begin
decode the instruction fetched;
if operand in memory then fetch operand;
execute instruction;
end"

The fetch and execute operations are carried out in synchronism with a clock. Several clock cycles elapse before a fetch or execute operation is performed. If the instruction contains data or address of the data, then one to two extra memory fetch cycles are needed. Figure (3.6) shows the execute cycle which is dependent of the instruction.

MACHINE CYCLE AND STATE: An Instruction cycle consists of an opcode fetch cycle followed by an execute cycle. The execute cycle itself consists of zero or more fetch cycles. All these operations are performed in different time slots known as machine cycles. An instruction cycle may consist of one or more machine cycles. One machine cycle itself consists of several clock cycles. Each of these clock cycles is known as T-state and are referred to as T1, T2--. Figure (3.7) shows a typical instruction cycle and machine cycles within it. It shows two machine cycles M1 and M2. M1 in which the operation code is fetched and decoded consists of 4 states, M2 in which the data is fetched and executed consists of 3 states.
FIG 3.7: A TYPICAL INSTRUCTION CYCLE
3.5 INPUT/OUTPUT PORTS

An input device is connected to the microprocessor through an input port and it is a place for unloading and loading of data. Data are transferred from the input device to the accumulator through input port.

An output device is connected to the microprocessor through an output port and the data are transferred to the output device. The figure (3.8) shows a microprocessor connected to the I/O device through the port.

The I/O ports may be used to reduce the chip count and external decoding logic in a microprocessor based system. An I/O port consists of several lines for data transfer and a few control lines. The data transfer lines may be used for input or output or both which are within the chip and are known as the outputs of latches and buffers.

An I/O port may be programmable or non-programmable. A non-programmable port connected in input mode, behaves as an input port, whereas a port connected in output mode acts as an output port. But a programmable I/O port can be programmed to act either as an input port or an output port.

The Intel 8212 is an 8-bit non-programmable I/O port and is shown in figure (3.9). It can be connected to the microprocessor either as an input port or an output port. The 8212 chip is selected if DS1.DS2 is true or if the D0-D08 lines are tristated. The port can be operated in two different modes using the mode control input.
FIG 3.8: DATA TRANSFER THROUGH AN I/O PORT
FIG 3.9: SCHEMATIC DIAGRAM OF INTEL 8212

DATA OUTPUT (D0 - D8)

CLEAR (CLR)

INTERRUPT (INT)

Vcc

GND

DATA INPUT (D11 - D18)

STROBE (STB)

DS1

MODE (MD)

DS2
(MD). When MD is high (output mode), the output buffers are enabled and the input data latching occurs using the DS1.DS2 signal. When MD is low (input mode), the input data is latched using the STB signal and the output buffers are enabled only when DS1.DS2 is true.

The port may be used to interrupt the microprocessor. The INT line goes low when the port is in the input mode and the STB goes high. The interrupt may be cleared by a low on the CLR line. Thus if INT line is connected to an active low interrupt of a microprocessor, the latter may be interrupted after the input data has been strobed in.

**programmable I/O ports**: A programmable I/O port can be programmable using IN and OUT instructions. A port may be programmable for one or more of the attributes namely
(a) Simple input or output mode
(b) strobed input or output mode
(c) control mode.

The port may latch input data from the input device or output data to the output device in the simple input or output mode, where as the data is loaded or unloaded using an external strobe signal in the strobed mode. In the control mode, the individual pins of a port are used for controlling data transfer to or from some other port.

### 3.6 PROGRAMMABLE PERIPHERAL INTERFACE

A programmable peripheral interface is a multiport device. The intel 8255A is a programmable peripheral
interface. It has three 8-bit ports, namely portA, portB and portC. The port 'C' has been further divided into two 4-bit ports. Port C upper and port C lower. Thus a total of 4 ports are available, two 8-bit ports and two 4-bit ports. Each Port can be programmed either as an input port or an output port.

SCHEMATIC DIAGRAM OF INTEL 8255A: Figure (3.10) shows the pin diagram of intel 8255A. It is a 40 pin I.C package, operating on a single 5V d.c supply.

CHIP SELECT (CS): It is a chip select signal. The low status of this signal enables communication between the CPU and 8255A.

READ (RD): When RD goes low the 8255A sends out data or status thus information to the CPU on the data bus.

WRITE(WR): When WR goes low the CPU writes data or control word 8255A.

A0 and A1: The selection of input port and control word register is done using using A0 and A1 in conjunction with RD and WR. These are normally connected to the least significant bits of the address bus.

BLOCK DIAGRAM OF THE 8255A: The block diagram of Intel 8255A is shown in figure(3.11). It has two 8-bit ports (A and B), two 4-bit ports, (pch, pcl), the data bus buffer and control logic.
FIG 3.10: SCHEMATIC DIAGRAM OF INTEL 8255-A
DATA BUS: Data is transmitted or received by the buffer upon execution of input or output instructions by the CPU. Control words and status information are transferred through the data bus buffer.

READ/WRITE AND CONTROL LOGIC: The control section has six lines namely RD, WR, RESET, CS, A0 and A1. It accepts input from the CPU address and control buses and internally issues commands to both of the control groups.

GROUP A AND GROUP B CONTROLS: The functional configuration of each port is programmed by the system software. In essence, the CPU outputs a control word to the 8255A. The control word contains information such as MODE bit set, bit set reset etc., that initializes the functional configuration of the 8255A. Each of the control blocks (Group A and Group B) accepts commands from the Read write logic, receives CONTROL WORD from the internal data bus and issues the proper commands to its associated ports.

CONTROL GROUP A- Port A and port C upper.

CONTROL GROUP B- Port B and port C lower.

The control word register can only be written into. Read operation of the control word register is not allowed.

8255A OPERATIONAL DESCRIPTION: The possible mode combinations by the system software is MODE 0, MODE 1 and MODE 2.
**MODE 0 : SIMPLE INPUT OR OUTPUT**

This functional configuration provides simple input and output operations for each of the three ports. No hand shaking is required. Data is simply written to or read from a specified port.

The input/output features in mode 0 are as follows;

1. Outputs are latched.
2. Inputs are not latched.
3. Ports do not have handshake or interrupt capability.

**MODE 1 : INPUT OR OUTPUT WITH HAND SHAKE**

This configuration provides a means for transferring I/O data to or from a specified port in conjunction with strobes or hand shaking signals. In this mode port A and port B use the lines on port C to generate or accept hand shaking signals.

**MODE 2: BIDIRECTIONAL DATA TRANSFER**

This configuration is used for communicating with a peripheral device on a single 8-bit bus for both transmitting and receiving data. Hand shaking signals are provided to maintain proper bus flow discipline in a similar manner to model interrupt generation and enable/disable functions are also possible.

**SINGLE BIT SET/RESET FEATURE:** Any of eight bits of port C can be SET or RESET using a single out instruction. This feature reduces software requirement in control based applications. When port C is being used as status/control for port A and port B these bits can be set or reset by using BITSET/RESET operation just as if they were data
INTERRUPT CONTROL FUNCTIONS: When the 8255A is programmed to operate in mode 1 or mode 2, control signals are provided that can be used as interrupt request inputs to the CPU. The interrupt request signals generated from port C, can be inhibited or enabled by setting or resetting the associated INTR flip-flop using the bit set/reset function of port C. This function allows the programmer to disallow or allow a specific I/O device to interrupt the CPU without affecting any other device in the interrupt structure.

3.7 PROGRAMMABLE INTERRUPT CONTROLLER

The programmable interrupt controller is used when several I/O devices transfer data using interrupt and they are to be connected to the same interrupt level of the microprocessor. The Intel 8259A is a single chip programmable interrupt controller. It is compatible with 8086, 8088 and 8085 microprocessors. It is a 28 pin dip I.C package and uses N-MOS technology. It requires a single +5v supply for its operation.

SCHEMATIC DIAGRAM OF INTEL 8259A:

The schematic diagram of Intel 8259A is shown in fig(3.12) Some of the details of the pins are as follows:

CS: It is a chip select signal.

WR: Write. A Low on this pin enables Intel 8259A to accept command word from CPU.
FIG 3.12 : SCHEMATIC DIAGRAM OF INTEL 8259A

Do - D7
CS
RD
WR
Ao
CASo-CAS2
SP / EN
INTA
IRo
IR1
IR7
Vcc
GND
INT
RD: Read. A Low on this pin enables Intel 8259A to send the various status signals on the data bus for CPU.

D0-D7: Bidirectional data bus. Control, status and interrupt vector information are transferred via this bus.

CAS0-CAS2: Cascade lines

SP/EN: Slave program/Enable buffer.

INT: Interrupt. It is used to interrupt CPU.

INTA: Interrupt acknowledge.

IR0-IR7: Interrupt requests. I/O devices send interrupt request through these lines.

A0: Address line. It acts in conjunction with RD, WR and CS. The Intel 8259 uses it to write a command word, to read a status and to determine the port address of the controller.

BLOCK DIAGRAM OF THE 8259A: The 8259A is upward compatible with its predecessor, the 8259 and its block diagram is as shown in figure(3.13). It includes eight blocks: control logic, Read/write logic, data bus buffer, three registers (IRR, ISR & IMR), priority resolver and cascade buffer.

READ/WRITE LOGIC: When the address line A0 is at logic 0, the controller is selected to write a command or read a status. The chip select logic and A0 determine the port address of the controller.
FIG 3.13: FUNCTIONAL BLOCK DIAGRAM OF 8259A
CONTROL LOGIC: This block has two pins namely INT (Interrupt) as an output, and INTA (Interrupt acknowledge) as an input. The INT is connected to the interrupt pin of the MPU. Whenever a valid interrupt is asserted this signal goes high.

INTERRUPT REGISTERS AND PRIORITY RESOLVER: The Interrupt Request Register (IRR) has eight input lines (IR0-IR7) for interrupts. When these lines go high, the requests are stored in the register. The In-Service Register (ISR) stores all the levels that are currently being serviced, and the Interrupt Mask Register (IMR) stores the masking bits of the interrupt lines to be masked. The Priority Resolver (PR) examines these three registers, and determines whether INT should be sent to the MPU.

CASCADE BUFFER / COMPARATOR: This block is used to extend the number of interrupt levels by cascading two or more 8259.

8259A OPERATIONAL DESCRIPTION: The 8259A should be first initialized by writing control words in the control register. The 8259A requires two types of control words:

a) Initialization command words (ICWS) and
b) Operational command words (OCWS).

After the 8259A is initialized, the following sequence of events occurs when one or more interrupt request lines go high.

1. The IRR stores the requests.
2. The priority resolver checks three registers, the IRR,
the IMR and the ISR. It resolves the priority and sets the INT high when appropriate.

3. The MPU acknowledges the interrupt by sending INTA.

4. After the INTA is received, the appropriate priority bit in the ISR is set to indicate which interrupt level is being served, and the corresponding bit in the IRR is reset to indicate that the request is accepted. Then, the opcode for the CALL instruction is placed on the data bus.

5. When the MPU decodes the CALL instruction, it places two or more INTA signals on the data bus.

6. When the 8259A receives the second INTA, it places the low-order byte of the CALL address on the data bus. At the third INTA, it places the high-order byte on the data bus. The CALL address is the vector memory location for the interrupt and this address is placed in the control register during the initialization.

7. During the third INTA pulse, the ISR bit is reset either automatically or by a command word and this is determined by the initialization command word (IWC).

8. The program sequence is transferred to the memory location specified by the CALL instruction.

3.8 PROGRAMMABLE DMA CONTROLLER

Direct Memory Access (DMA) is an I/O technique commonly used for high speed data transfer. The 8257 is a programmable, 4-channel, direct memory access controller. This means that four peripherals can request data transfer, and the request priorities are determined internally. It is a 40 pin I.C. package and requires a
single +5v supply for its operation. Four I/O devices can be interfaced to the microprocessor through this device. It is capable of performing three operations, namely read, write and verify. During the read operation data are directly transferred from the memory to the I/O device. During the write operation data are transferred from the I/O device to the memory. On receiving a request from I/O device, the 8257 generates sequential memory address which allows the I/O device to read or write directly to or from the memory.

**SCHEMATIC DIAGRAM OF INTEL 8257:** Figure (3.14) shows the schematic diagram of 8257.

**DRQ0-DRQ3:** These are DMA request lines. An I/O device sends its DMA request on one of these lines. A HIGH status of the line generates a DMA request.

**DACK0-DACK3:** These are DMA acknowledge lines. The Intel 8257 sends an acknowledge signal through one of these lines informing an I/O device that it has been selected for DMA data transfer.

**A0-A7:** These are address lines. A0-A3 are bidirectional lines. In the slave mode these lines are input lines. A4-A7 lines give tristated outputs generated by the 8257.

**D0-D7:** These are bidirectional three-state data lines while programming the controller, the CPU sends data for the DMA address register, the byte count register and the mode set register through these data lines.
FIG 3.14: SCHEMATIC DIAGRAM OF INTEL 8257
ADSTB: A HIGH on this line latches the 8 MSBs of the address, which are sent on data bus.

I/OW: I/O write. It is a bidirectional line. In output mode it allows the transfer of data to the I/O device during the DMA read cycle. Data is transferred from the memory.

BLOCK DIAGRAM OF THE 8257 DMA CONTROLLER: Figure 3.15 shows the block diagram of the 8257 DMA controller. It is a programmable device which has three blocks namely data bus buffer, Read / Write logic and four channels.

DMA CHANNELS: The 8257 has four identical channels, each with two signals DRQ(DMA Request) and DACK(DMA acknowledge). Each channel has two 16-bit registers. one for the memory address where data transfer should begin, and the second for a 14-bit count. Bits D15 and D14 of the count register specify the DMA function write, Read or verify.

SIGNAL AEN (ADDRESS ENABLE): The AEN output signal is used to disable the system data bus and control bus. This signal is necessary to switch the 8257 from the slave mode to the master mode.

DMA EXECUTION: The process of data transfer from the peripheral to the system memory under the DMA controller can be classified under two modes namely the slave mode, and master mode.

SLAVE MODE: In the slave mode the DMA controller is treated as a peripheral using the following steps:

1) The MPU selects the DMA controller through chip select.
FIG 3.15 : FUNCTIONAL BLOCK DIAGRAM OF INTEL 8257

DATA BUS BUFFER

CH-0 16-BIT ADDR CNTR

CH-1 16-BIT ADDR CNTR

CH-2 16-BIT ADDR CNTR

CH-3 16-BIT ADDR CNTR

DATA BUS BUFFER

READ / WRITE LOGIC

CONTROL LOGIC AND MODE REGISTER

A4 A5 A6 A7 READY HROD MEMR MEMW ANE ADSTB MARK TC

1/DR 1/DN CLK RESET A0 A1 A2 A3
2) The MPU writes the command mode and terminal count in channel register by accessing the register through Ao-A3 and through the control signal IOR and IOW.

**MASTER MODE**: In master mode, the 8257 keeps checking for a DMA request, and the steps in data transfer can be as follows:

1) When the peripheral is ready for data transfer, it sends a high signal to DRQ.

2) When the DRQ has been received and the channel enabled, the control logic sets HRQ high.

3) In the next cycle, the MPU relinquishes the buses and sends the HLDA signal to the 8257.

4) After receiving the HLDA signal, the control logic generates DACK and sends the acknowledgement to the peripheral.

5) Meanwhile, the 8257 enables the Signal AEN (ADDRESS ENABLES). AEN disables the MPU demultiplexed address bus A7-A0. The entire bus, A7-A0, of the 8257 becomes output.

6) The low-order byte of the memory location is placed on the A7-A0 of the 8257.

7) When the AEN signal is high, the ADSTB (address strobe) signal goes high and places the high-order byte of the memory location on address bus A15-A8. Data transfer continues until the count reaches zero.
3.9 PROGRAMMABLE COMMUNICATION INTERFACE

The Programmable communications interface is used for serial data transmission. The intel 8251A is a Programmable communication interface. It is universal synchronous/Asynchronous Receiver/transmitter, (USART). It is compatible with 8085, 8086, 8088, and 8748 system. The I.C chip is fabricated using N-channel silicon gate technology. The 8251A can be used to transmit/receive serial data. It accepts data in parallel format from the microprocessor and converts them into serial data for transmission. It also receives serial data and converts them into parallel and sends the Data in parallel format to the CPU.

SCHEMATIC DIAGRAM OF INTEL 8251A: Figure (3.16) shows a schematic diagram of intel 8251A. The description of some important pins are as follows:

C/D : (control/Data): When it is low data is transmitted on Data bus. When it is high control signal are transmitted on the Data bus.

RD : (Read). When it is low the CPU reads Data from intel 8251A.

WR : (Write). When it is low the CPU reads data from Intel 8251A.

CTS : A low on this pin enables 8251A to transmit serial data.

TXC : (Transmitter clock). It governs the rate of data transmission.
INTEL 8251A

TXD
TXRDY
TXE
RXD
RXRDY
RXC
SYNDET /RDRDET
CS
CLK
RESET
RD
WR
c/5

Do-D7
DSR
DTR
CTS
RTS
Vcc
GND
TXE: (Transmitter empty). TXE goes high when 8251A has no characteristic to transmit. It indicates the end of transmission.

RXC: (Receiver clock). It governs the rate at which characters are received.

BLOCK DIAGRAM OF THE INTEL 8251A: The 8251A is the enhanced version of its predecessor, the 8251 and is compatible with the 8251. Figure (3.17) shows the block diagram of the 8251A. It has five sections namely Read/Write Control logic, Transmitter, Receiver, Data bus Buffer, and modem control.

READ/WRITE CONTROL LOGIC AND REGISTERS: This section includes Read/Write control logic, six input signals i.e. CS (chip select), C/D (control/Data), WR (write), RD (READ), RESET (reset) and CLK (CLOCK), CONTROL LOGIC, and three buffer registers namely data register, control register, and status register.

TRANSMITTER SECTION: The transmitter section converts a parallel word received from the MPU into serial bits and transmitts them over the TXD line to a peripheral. It has two registers namely
a) A buffer register to hold eight bits and
b) An output register to convert eight bits into a stream of serial bits.

RECEIVER SECTION: The receiver accepts serial data on the RXD line from a peripheral and converts them into parallel data. The section has two registers: the receiver input
FIG 3.17 : FUNCTIONAL BLOCK DIAGRAM OF 8251A

TRANSMIT BUFFER

RECEIVE BUFFER

DATA BUS BUFFER

TRANSMIT CONTROL

RECEIVE CONTROL

INTERNAL DATA BUS

READ / WRITE CONTROL LOGIC

MODE M CONTROL

RESET

CLK

D7-Do

RXD

TXD

TXRDY

RXRDY

TXE

TXC

RXC

SYNCET

CS

DSR

DTR

CTS

RTS
register and the buffer register.

When the RXD line goes low, the control logic assumes it as a START bit, waits for half a bit time, and samples the line again. If the line is still low, the input register accepts the bits, forms a character, and loads it into the buffer register. Subsequently the parallel byte is transferred to the MPU when requested. In the asynchronous mode, two i/p signals and one o/p signal are necessary i.e RXD - Receive Data, RXC - Receiver clock and RXRDY - Receiver Ready.

3.10 PROGRAMMABLE INTERVAL TIMER

A programmable Counter / Interval Timer is used for timing and counting function. Programmable interval timer chips are Intel 8253 and 8254. The 8253 operates in the frequency range of d.c to 2.6 MHz whereas 8254 in the range of d.c to 10 MHz. Both are operated in the six modes namely,

mode 0 : Interrupt on terminal count
mode 1 : Programmable one - shot
mode 2 : Rate generator
mode 3 : Square wave mode
mode 4 : Software triggered mode
mode 5 : Hardware triggered mode

SCHEMATIC DIAGRAM OF INTEL 8253: The 8253 is 24-pin IC and operates at 5V d.c. It contains three independent 16-bit counters. It operates under software
control. Figure (3.18) shows its pin diagram. Some of the pins are,

a. CLK0, CLK1, and CLK2 are clocks for counter 0, counter 1 and counter 2 respectively.
b. GATE0, GATE1, and GATE2 are gate terminals,
c. OUT0, OUT1, OUT2 are output terminals.

**BLOCK DIAGRAM OF THE 8253:** Figure (3.19) shows the block diagram of the 8253. It contains three counters (0, 1 and 2) and each counter has two input signals - CLOCK (CLK) and buffer, Read/write control logic, and a control register.

**DATA BUS BUFFER:** It is within 8253. It is a 3-state, bidirectional, 8-bit buffer. It is used to interface 8253 to the system data bus through D0 - D7 lines.

**Read/Write control logic:** The control section has five signals (a) RD (Read), (b) WR (Write) (c) CS (chip select) and the (d) Address lines A0 and A1. This control section accepts input from the system bus and then generates control signals for the operation of 8253.

**CONTROL WORD REGISTER:** This register is selected when lines A0 and A1 are at logic 1. It is used to write a command word which specifies the counter to be used, its mode and either a Read or a Write operation. The control word is stored in control word Register.

**OPERATIONAL DESCRIPTION OF 8253:** The 8253 contains three independent edge triggered presettable 16-bit
FIG 3.18 — SCHEMATIC DIAGRAM OF INTEL 8253
FIG 3.19 : FUNCTIONAL BLOCK DIAGRAM OF 8253
down counters namely, counter 0, counter 1 and counter 2. These counters are independent, and they can have separate mode configuration and counting operation. The clock of 8253 should be less than 2.6 MHz, since the clock O/P of 8085 is about 3 MHz.

**MODE 0 : (INTERRUPT ON TERMINAL COUNT)** MODE 0 is used for the generation of accurate time delay under software control. The mode is set by loading the control word into the control word register. After mode set operation the counter is loaded by the desired count N and the counting starts if GATE is high. The counter output remains low while the counting is going on. When the count reaches 0, the output becomes high and remains high until the count is reloaded or new count is loaded. If GATE is made low during counting operation counting stops.

**MODE 1 : (PROGRAMMABLE ONE - SHOT)** In MODE 1 the counter acts as a retrigerable and programmable one - shot. The low to high transition of the signal applied to GATE acts as a trigger signal. When the mode is set, OUT becomes high and the counter is loaded by a count value of N. Then the counter decrements count, and the output goes low for N - clock cycles for every low to high transition of the GATE input. It goes high on the terminal count i.e counter content = 0. If the GATE input is made low to high again, the counter is reloaded by the count value N. The counter starts decrementing the count again and the output goes low for N clock pulses again. Thus one - shot mode of operation is retrigerable.
MODE 2 : (RATE GENERATOR) In MODE 2 the counter acts as a simple divide by N counter. When this mode is set, the output of the counter becomes high and the counter is loaded by a count of value N. For this operation GATE is kept high. In this mode the output remains high for \((N-1)\) clock pulses and then high again and the count \(N\) is automatically reloaded into the counter. In this way the whole process is repeated as long as the GATE input is high.

MODE 3 : (SQUARE WAVE GENERATOR) In MODE 3 the counter acts as a square wave generator. After mode set operation the counter is loaded by a count of value \(N\) and GATE is kept high. For even values of \(N\) the output remains high for \(N/2\) clock pulses and then goes low for next \(N/2\) clock pulses, and the process is repeated.

MODE 4 : (SOFTWARE TRIGGERED STROBE) In mode 4 operation the output of the counter becomes high after the mode is set and the GATE is kept high. The counter begins counting immediately after the count is loaded into the count register, when the counter reaches terminal count, the output goes low for one clock period, then it returns to high. The output signal may be used as strobe.

MODE 5 : (HARDWARE TRIGGERED STROBE) In this mode of operation GATE input acts as a trigger. After the mode is set, the output becomes initially high when a count value of \(N\) is loaded into the counter. The counting begins at the first negative edge of the clock after the rising edge of the GATE input, on terminal count the output goes low for
one clock period, then it goes high again. As the low to high transition of the GATE input causes triggering this mode is called as hardware triggered strobe.

### 3.11 ANALOG SUBSYSTEMS

**ANALOG INPUT SUBSYSTEMS:** An Analog input subsystem has an ADC (Analog to Digital) as only one of its components.

Intel's SBC 711 Analog input Board and Burr Brown's MP20 Analog input microperipheral are two examples. These two are compatible with 8085 based systems.

**SBC 711 ANALOG INPUT BOARD:** The SBC 711 is a single board device. It may be used for monitoring up to 16 process variables in a single-ended mode and up to 8 in a differential mode. It can be interfaced and addressed in a memory mapped mode. The ADC on the board gives a 12-bit digital equivalent of the analog input on the selected input channel. Figure (3.20) shows a block diagram of the board.

**OPERATION OF THE SBC 711:** The 16 single-ended input or 8 differential input channels are input to an analog multiplexer (MUX). By programming the MUX register any one of these input channels may be multiplexed to the programmable gain amplifier (PGA). The PGA gain can be set to 1, 2, 4 or 8 by programming the 2 most significant bits of the gain register.
FIG 3.20 : BLOCK DIAGRAM OF SBC 711 I/O SIGNALS
The ADC provides four voltage ranges +5v, -5v, +10v, -10v. Depending on the input signal voltage, a suitable gain value may be selected so that the input to the ADC, which is the output of the PGA, lies in a suitable range. The output of the PGA is applied to the sample and hold (S/H) amplifier and is shown in the block diagram of figure (3.21) SBC 711.

The latter continuously tracks the input voltage until a trigger signal is received. The trigger signal may be generated on board or from an external source or initiated by the program. When the trigger is received S/H amplifier enters the hold mode and the A/D conversion process begins.

The output of the ADC is 12-bit approximation of the input voltage. It may be either in straight binary code or in two’s complement binary code depending on how the jumper wires have been configured. This output may be read by the processor one byte a time.

OPERATING MODES: The analog input multiplexer can be jumper programmed to operate in one of three modes - random channel input, single repetitive channel input and sequential channel input.

ANALOG OUTPUT SUBSYSTEMS: The digital output from the µP has to be converted to a proportional analog output for driving electrical subsystems. The Digital to - Analog convertors (DACs) are used for this purpose. Intel’s SBC724 known as the Analog output Board and Burr
FIG 3.21: PARTIAL BLOCK DIAGRAM OF SBC 711 ANALOG INPUT BOARD

- INPUT PROJECT
- ANALOG INPUTS
- CHANNEL ADDRESS
- GAIN
- S/H
- 12-BIT ADC AND CONTROL
- OUTPUT BUFFER
- DAT0-DAT7
- FIG 3.21: PARTIAL BLOCK DIAGRAM OF SBC 711 ANALOG INPUT BOARD

- INPUT PROJECT
- ANALOG INPUTS
- CHANNEL ADDRESS
- GAIN
- S/H
- 12-BIT ADC AND CONTROL
- OUTPUT BUFFER
- DAT0-DAT7

- INPUT PROJECT
- ANALOG INPUTS
- CHANNEL ADDRESS
- GAIN
- S/H
- 12-BIT ADC AND CONTROL
- OUTPUT BUFFER
- DAT0-DAT7

- INPUT PROJECT
- ANALOG INPUTS
- CHANNEL ADDRESS
- GAIN
- S/H
- 12-BIT ADC AND CONTROL
- OUTPUT BUFFER
- DAT0-DAT7

- INPUT PROJECT
- ANALOG INPUTS
- CHANNEL ADDRESS
- GAIN
- S/H
- 12-BIT ADC AND CONTROL
- OUTPUT BUFFER
- DAT0-DAT7
Brown's MP10 are two cards which are compatible with Intel's 8080 and 8085 CPUs.

**SBC 724 ANALOG OUTPUT BOARD:** The SBC 724 consists of 4 DAC modules each capable of converting a 12-bit input to an analog output. The output voltage range can be jumper configured to any one of the following four: +10V, -10V, +5V, -5V. The Up communicates with the board by means of memory write commands. The board may be assigned any base address which is a multiple of 8 by suitably connecting the jumper wires. The data sent out by the Up is latched by the addressed DAC and the conversion begins. The latching is done when the high byte is transferred. The low byte is initially stored in a hold register which is common to all DACs. It is transferred to the latch associated with the addressed DAC when the high byte is received.

**OUTPUT WIRING:** The output of each DAC may be applied across a load as shown in figure (3.22). The minimum resistance value can be determined from the output voltage range and the maximum output current of the DAC. Short circuit protection is provided for each DAC.
Fig 3.22: Output wiring for each DAC

FIG 3.22 : OUTPUT WIRING FOR EACH DAC