CHAPTER 2

HARDWARE OF RFID BASED LIBRARY MANAGEMENT SYSTEM
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2.1. INTRODUCTION

RFID stands for Radio Frequency Identification. It is an electronic technology whereby digital data encoded in an RFID Tag (or transponder) is retrieved utilizing a reader. In contrast to bar code technology [1], RFID systems do not require line-of-sight access to the tag in order to retrieve the tag's data, and they are well suited to harsh environments.

An RFID tag consists of an integrated circuit attached to an antenna. In the case of the tags used with the DLP-RFID1, the antenna is in the form of conductive ink "printed" on a material that allows for connection to the integrated circuit. This type of passive (battery-free) tag is commonly referred to as an "inlay".

The RFID reader is typically a microcontroller-based radio transceiver that powers the tag with a time-varying electromagnetic radio frequency (RF) field. When the RF field passes through the tag's antenna, AC voltage is generated in the antenna and rectified to supply power to the tag [2]. Once powered, the tag can receive commands from the reader.

The information stored in the tag can then be read by the reader and sent back to the host PC for processing. The data in the tag consists of a hard-coded, permanent serial number (or UID) and user memory that can be written to, read from and locked if desired. Once locked, user data can still be read but not changed.
RFID in Library

Figure 2.1: RFID based library management system

A library is a collection of information, sources, resources, books, and services, and the structure in which it is housed and access points for maps, prints or other documents on various storage media such as microform (microfilm/microfiche), audio tapes, CDs, LP's, cassettes, videotapes and DVDs. Libraries have materials arranged in a specified order according to a library classification system[3], so that items may be located quickly and collections may be browsed efficiently. Reference stacks are different which has only reference books and only selected members.

The following are the tasks to be performed in the library.

- Circulation: handling user accounts and issuing/returning and shelving of materials.
- Collection, development, order materials, maintain materials’ budgets.
- Technical Services work behind the scenes cataloguing and processing new materials and de accessioning weeded materials.

Basic tasks in library management include the planning of acquisitions of materials, arranging the acquired materials according to the library classification, preservation of materials the DE accessioning of materials, patron borrowing of materials, and developing and administering library computer systems[4]. Among these, the proposed system will automate the following tasks using RFID technology,
• Accessing number of books at a time
• Searching a particular book to check its presence in the library
• Locating the physical location of the book
• Accounting/Stock verification of the materials

The RFID based LMS facilitates the fast issuing, reissuing and returning of books with the help of RFID enabled modules. It directly provides the book information and library member information to the library management system and does not need the manual typing. It also provides monitoring and searching system. The monitoring module will continuously monitor the movement of books across the gates, so that the books taken out without prior issuing will be traced out easily and will alarm the librarians [5]. The searching module provides the fast searching of books using RFID handheld reader. The physical location of the books can be easily located using this module.[6]

Utmost care has been taken to provide following features to the Library using RFID technology:

• To remove manual book keeping of records
• Traceability of books and library members as they move
• Improved utilization of resources like manpower, infrastructure etc.
• Less time consumption as line of sight and manual interaction are not needed for RFID- tag reading.
• To provide 2 meters read range antennas
• To minimize the manual intervention
• To minimize the manual errors
• To provide the long lasting labels
• To provide fast searching of books
The block diagram RFID based library management system is shown in figure 2.1 and photograph 1. The system consists of the following elements, they are:

1) RFID Read/Writer
2) RFID TAG
3) Serial to USB converter
4) Personal computer

2.2. **RFID Read/Writer (DLP RFID1)**

The block diagram of DLP RFID1 Read/Writer is shown figure 2.2 which consists of RFID Read/Writer (TRF 7960), Microcontroller (MSP430F2370), USB interface (FT 232RL), Personal Computer [6].

![Block diagram of DLP RFID1 Read/Writer](image)

**Figure 2.2 : Block diagram of DLP RFID1 Read/Writer**

Each DLP-RFID1 contains a unique, 32-bit, hard-coded serial number that cannot be altered by any means. The serial number can be read via the USB interface and used to identify the reader via the host software.
The specification of the system is given below.

**SPECIFICATIONS**

**Reader Frequency** 13.56MHz

**Output Power** 200mW MAX

**Range (Integral Antenna)** 4 Inches MAX

**Tags/Protocols Supported** Tag-It*, ISO18000-3, ISO15693

**Communications Interface** USB 1.1/2.0 Compatible, Mini-B 5-Pin Connector

**Operational Power – Active** 120mA

**Operational Power – Idle** 15mA

**Antenna** On-Board Antenna, SMA Position Available**

**USB Driver Support** Windows XP, XPx64, Server2003, 2000, 98, ME

**Physical Dimensions – OEM** PCB: .20x2.17x3.12" typ. (5.1x55.1x79.3mm)

**Physical Dimensions – Retail** Enclosure: .83x2.3x3.25" typ. (21.1x58.4x82.6mm)

**Operating Temperature** 0-70°C

**2.2.1 Microcontroller (MSP 430F2370)**

The Texas Instruments MSP430F2370 is ultra-low-power microcontroller consist of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with five low-power modes, is optimized to achieve extended battery life in portable measurement applications [7]. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency.
The digitally controlled Oscillator (DCO) allows wake-up from low-power modes to active mode in less than 1 μs.

The MSP430F2370 series is an ultra-low-power microcontroller with two built-in 16-bit timers, one universal serial communication interface (USCI), a versatile analog comparator, and 32 I/O pins. Universal Serial Communication Interface are Enhanced UART Supporting Auto Baud rate Detection (LIN), IrDA Encoder and Decoder, Synchronous SPI, I2C, etc. The pin diagram of MSP430F2370 is as shown in figure 2.4 and functional block diagram in figure 2.5.

- Low Supply Voltage Range: 1.8 V to 3.6 V
- 32KB + 256B Flash Memory,2KB RAM
- Ultra-Fast Wake-Up From Standby Mode in Less Than 1 μs
- 16-Bit RISC Architecture, 62.5-ns Instruction Cycle Time
- 16-Bit Timer_A, Timer_B With Three Capture/Compare Registers
- On-Chip Comparator for Analog Signal Compare Function or Slope A/D Conversion
- Internal Frequencies up to 16 MHz With Four Calibrated Frequencies to ±1%: Internal Very Low Power LF Oscillator, 32-kHz Crystal, High-Frequency Crystal up to 16 MHz, Resonator, External Digital Clock Source, External Resistor
- Serial Communication Interface (USART), Brownout Detector, Supply Voltage Supervisor/Monitor, Bootstrap Loader
- Enhanced UART Supporting Auto Baud rate Detection (LIN), IrDA Encoder and Decoder, Synchronous SPI, I2C™
Figure 2.4: Pin configuration of MSP430F2370

Figure 2.5: Functional block diagram of MSP430F2370

a. CPU

The MSP430™ CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand. The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock. Four of the registers, R0 to R3, are dedicated as program
counter, stack pointer, status register, and constant generator respectively. The remaining registers are general-purpose registers. Peripherals are connected to the CPU using data, address, and control buses and can be handled with all instructions. And about the peripherals are explained below.

b. Operating Modes

The MSP430 microcontrollers have one active mode and five software-selectable low-power modes of operation. An interrupt event can wake up the device from any of the five low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program. The following six operating modes can be configured by software:

- Active mode (AM) – All clocks are active.
- Low-power mode 0 (LPM0) – CPU is disabled, ACLK and SMCLK remain active. MCLK is disabled.
- Low-power mode 1 (LPM1) – CPU is disabled ACLK and SMCLK remain active. MCLK is disabled, DCO dc-generator is disabled if DCO not used in active mode.
- Low-power mode 2 (LPM2) – CPU is disabled, MCLK and SMCLK are disabled, DCO dc-generator remains enabled, ACLK remains active.
- Low-power mode 3 (LPM3) – CPU is disabled, MCLK and SMCLK are disabled, DCO dc-generator is disabled, ACLK remains active.
- Low-power mode 4 (LPM4) – CPU is disabled, ACLK is disabled, MCLK and SMCLK are disabled, DCO dc-generator is disabled, Crystal oscillator is stopped.

c. Oscillator and System Clock

The clock system is supported by the basic clock module that includes support for a 32768-Hz watch crystal oscillator, an internal very-low-power low-frequency oscillator, an
internal digitally-controlled oscillator (DCO), and a high-frequency crystal oscillator. The basic clock module is designed to meet the requirements of both low system cost and low power consumption. The internal DCO provides a fast turn-on clock source and stabilizes in less than 1μs. The basic clock module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32768-Hz watch crystal, a high-frequency crystal, or the internal very-low-power LF oscillator.
- Main clock (MCLK), the system clock used by the CPU.
- Sub-Main clock (SMCLK), the sub-system clock used by the peripheral modules.

d. Digital I/O

There are four 8-bit I/O ports implemented—ports P1, P2, P3, and P4:

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt condition is possible.
- Edge-selectable interrupt input capability for all eight bits of port P1 and P2.
- Read/write access to port-control registers is supported by all instructions.
- Each I/O has an individually programmable pull-up/pull-down resistor.

e. Comparator_A+

The primary function of the comparator A+ module is to support precision slope analog-to-digital conversions, battery-voltage supervision, and monitoring of external analog signals.

f. Timer_A3

Timer_A3 is a 16-bit timer/counter with three capture/compare registers. Timer_A3 can support multiple capture/comparers, PWM outputs, and interval timing. Timer_A3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.
g. Universal Serial Communications Interface (USCI)

The USCI module is used for serial data communication. The USCI module supports synchronous communication protocols like SPI (3 or 4 pin), I2C and asynchronous communication protocols such as UART, enhanced UART with automatic baud rate detection (LIN), and IrDA. USCI_A0 provides support for SPI (3 or 4 pin), UART, enhanced UART, and IrDA. USCI_B0 provides support for SPI (3 or 4 pin) and I2C.

h. JTAG fuse check mode

MSP430 devices that have the fuse on the TEST terminal have a fuse check mode that tests the continuity of the fuse the first time the JTAG port is accessed after a power-on reset (POR). When activated, a fuse check current, a fuse check current, ITF, of 1 mA at 3 V, 2.5 mA at 5 V can flow from the TEST pin to ground if the fuse is not burned. Care must be taken to avoid accidentally activating the fuse check mode and increasing overall system power consumption.

RFID Reader IC (TRF7960/61)

Description

The TRF7960/61 is an integrated analog front end and data-framing system for a 13.56-MHz RFID reader system. Built-in programming options make it suitable for a wide range of applications for proximity and vicinity RFID systems [8]. The reader is configured by selecting the desired protocol in the control registers. Direct access to all control registers allows fine tuning of various reader parameters as needed.

![Figure 2.6: Top view of TRF796x Pin Assignments](image)
A parallel or serial interface can be implemented for communication between the MCU and reader. Transmit and receive functions use internal encoders and decoders with a 12-byte FIFO register. For direct transmit or receive functions, the encoders/decoders can be bypassed so the MCU can process the data in real time. The transmitter has selectable output power levels of 100 mW (20 dBm) or 200 mW (23 dBm) into a 50-Ω load (5-V supply) and is capable of ASK or OOK modulation. Integrated voltage regulators ensure power-supply noise rejection for the complete reader system.

Data transmission comprises low-level encoding for ISO15693, modified Miller for ISO14443-A, high-bit-rate systems for ISO14443 and Tag-it coding systems. Included with the data encoding is automatic generation of SOF, EOF, CRC, and/or parity bits.

The receiver system enables AM and PM demodulation using a dual-input architecture. The receiver also includes an automatic gain control option and selectable gain. Also included is a selectable bandwidth to cover a broad range of input subcarrier signal options. The received signal strength for AM and PM modulation is accessible via the RSSI register. The receiver output is selectable between a digitized subcarrier signal and any of eleven integrated subcarrier decoders (two for ISO15693 low bit rate, two for ISO15693 high bit rate, two for ISO14443, three for ISO14443 high bit rates, one for Tag-it, and one for HF-EPC system). Selected decoders also deliver bit stream and a data clock as outputs.

The receiver system also includes a framing system. This system performs CRC and/or parity check, removes the EOF and SOF settings, and organizes the data in bytes. Framed data is then accessible to the MCU via a 12-byte FIFO register and MCU interface. The framing supports ISO14443 and ISO15693 protocols.

The TRF7960/61 supports data communication levels from 1.8 V to 5.5 V for the MCU I/O interface, while also providing a data synchronization clock. An auxiliary 20-mA regulator (pin 32) is available for additional system circuits.
2.2.2. HF-I PLUS Transponder inlays miniature rectangle

DESCRIPTION

Texas Instruments Tag-it™ HF-I plus transponder inlays consist of 13.56-MHz high-frequency (HF) transponders that are compliant with the ISO/IEC 15693 and ISO/IEC 18000-3 global open standards[9]. These products offer a user-accessible memory of 2048 bits, organized in 64 blocks, and an extensive command set available in six different antenna shapes, with frequency offset for integration into paper, PVC, or other substrates.

The Tag-it HF-I plus transponder inlays are manufactured with TI’s patented laser tuning process to provide consistent read performance. Prior to delivery, the transponders undergo complete functional and parametric testing in order to provide the high quality that customers have come to expect from TI.

Figure 2.7 : HF-PLUS tag (RI-I03-112A-03)

The Tag-it HF-I plus transponder inlays are well suited for a variety of applications including, but not limited to, product authentication, library, supply-chain management, asset management, and ticketing/stored value applications.

HF-I Plus Transponder Chip/Inlays Implemented Commands Table 2.1 shows the list of implemented and reserved (RFU) commands and the corresponding request modes of these commands as implemented in TI’s ISO15693 compliant Tag-it HF-I Plus Transponder Chip/Inlays [9]. The request mode defines the set of transponders that shall answer to the request.
Table 2.1: Tag-it HF-I plus Transponder Chip/Inlays Implemented Commands

Memory Architecture

The physical memory structure is byte oriented and is organized in blocks of fixed size (see Figure 2.8).

User Memory

The available user memory size is 64 blocks of 32 bits each. This results in a capacity of 2 Kbits available user memory.

Additional Blocks

- Two blocks wide (64 Bit) factory programmed memory to store the UID.
• One wide factory programmed memory to store the IC Reference and the Physical memory info:
  - IC-Ref: 0x8x (0x081 is the Current version of the IC)
  - Block Size: 0x03 (Count from 0, =4 Bytes)
  - Number of Blocks: 0x3F (Count from 0, =64 Blocks)

• One blocks wide user programmable memory to store the DSFID field.

• One blocks wide user programmable memory to store the AFI field.
  
  Each user block has two Lock Bits attached, allowing individual block locking.

HF-1 Plus Supported Commands

The syntax of the ISO defined commands can be found in the ISO/IEC 15693-3. The syntax of the TI Custom commands is described below.

Custom Commands

The format of Custom Commands is generic and allows unambiguous attribution of Custom Command Codes and procedures to each Transponder (IC) Manufacturer. For the execution of a Custom Command the Transponder (IC) Manufacturer Code has to be included in the Request. The manufacturer code for TI is 0x07. The implemented TI custom commands can be seen in Table 2.2.

<table>
<thead>
<tr>
<th>FUNCTION</th>
<th>COMMAND CODE</th>
<th>REQUEST MODE</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>HEX</td>
<td>BINARY (LSB)</td>
</tr>
<tr>
<td>RFU</td>
<td>0xA0</td>
<td>1010 0000</td>
</tr>
<tr>
<td>RFU</td>
<td>0xA1</td>
<td>1010 0001</td>
</tr>
<tr>
<td>Write_2_Blocks</td>
<td>0xA2</td>
<td>1010 0010</td>
</tr>
<tr>
<td>Lock_2_Blocks</td>
<td>0xA3</td>
<td>1010 0011</td>
</tr>
<tr>
<td>RFU</td>
<td>0xA4-0xDF</td>
<td></td>
</tr>
</tbody>
</table>

✓ = Implemented, - = Not applicable

Table 2.2 : Custom Commands Table
Command Write_2_Blocks (0xA2)

When receiving the Write 2 Block Command, the Transponder shall program the requested blocks with the data contained in the Request and report the success of the operation in the Response. Is a shown table 2.3.

If one or both of the addressed blocks are locked the Transponder shall not execute the write operation and return the Error code 0xA2.

The transmitted LSB block data are written to the LSB of the even addressed block (Bytes 0-3) and the MSB transmitted data to the odd addressed block (Bytes 4-7).

<table>
<thead>
<tr>
<th>TRANSMITTED DATA</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>LSB</td>
<td></td>
</tr>
<tr>
<td>EVEN BLOCK</td>
<td>ODD BLOCK</td>
</tr>
<tr>
<td>0 1 2 3</td>
<td>4 5 6 7</td>
</tr>
</tbody>
</table>

Table 2.3 : Write_2_Blocks, Order of Blocks

Command Lock_2_Blocks (0xA3)

When receiving the Lock_2_Block Command, the Transponder shall lock the addressed blocks and report the success of the operation in the Response. The addressed pair of Blocks should contain one even and one odd Block (e.g., Block number 2 and 3 or Block number 6 and 7). The start block address should be always the block with the even address (e.g., #2, #4, #6 etc.). If in the start block the odd address is used the Transponder shall not execute the Lock Block operation and return the Error code 0xA1. If one or both of the addressed blocks are locked the VICC shall return the error code 0xA2.

Command Execution in “Inventory Mode”

The ISO Inventory Mode command (0x01) has been defined in the standard as a stand-alone command to address a defined set of Transponder’s information to be included in the response. The Response data for the Inventory command are DSFID and UID.
Experiments on Position of Tags in Books

Placement of currently deployed high frequency (HF) tags is a critical factor affecting system performance (see Figure 2.9 below). When tag placement in one item directly overlays another placement and both items are in very close proximity, readability is compromised [10]. The antenna component of each tag interacts and changes the radio frequency, making it difficult for the RFID readers to communicate with the tag. This is analogous to tuning your FM receiver just a little bit away from the channel you are trying to receive, diminishing the quality of the reception. A way to avoid this is the process of staggering tags in like items that are shelved in close proximity.

Figure 2.9 : Placement of HF RFID Tags

While RFID tags operate with high reliability and readability on most items, principally books, there are still challenges in regards to some forms of media. Size constraints and
presence of metal are core issues to overcome. These constraints apply equally to all applications of RFID.

2.2.3. USB to Serial converter

Functional Block Diagram

![FT 232R Block Diagram](image)

**Figure 2.10: FT 232R block diagram**

**Functional Block Descriptions**

a. **3.3V LDO Regulator** - The 3.3V LDO Regulator generates the 3.3V reference voltage for driving the USB transceiver cell output buffers. It requires an external decoupling capacitor to be attached to the 3V3OUT regulator output pin. It also provides 3.3V power to the 1.5kΩ internal pull up resistor on USBDP. The main function of this block is to power the USB Transceiver and the Reset Generator Cells rather than to power external logic. However, external circuitry requiring a 3.3V nominal supply at a current of around 50mA could also draw its power from the 3V3OUT pin, if required.

b. **USB Transceiver** - The USB Transceiver Cell provides the USB 1.1 / USB 2.0 full-speed physical interface to the USB cable. The output drivers provide 3.3V level slew rate control signaling, whilst a differential receiver and two single ended receivers provide USB data in, SEO and USB reset condition detection. This Cell also incorporates internal USB series resistors on the USB data lines and a 1.5kΩ pull up resistor on USBDP.
c. **USB DPLL** - The USB DPLL cell locks on to the incoming NRZI USB data and provides separate recovered clock and data signals to the SIE block.

d. **Internal 12MHz Oscillator** - The Internal 12MHz Oscillator cell generates a 12MHz reference clock input to the x4 Clock multiplier. The 12MHz Oscillator is also used as the reference clock for the SIE, USB Protocol Engine and UART FIFO controller blocks.

e. **Clock Multiplier / Divider** - The Clock Multiplier / Divider takes the 12MHz input from the Oscillator Cell and generates the 48MHz, 24MHz, 12MHz, and 6MHz reference clock signals. The 48Mz clock reference is used for the USB DPLL and the Baud Rate Generator blocks.

f. **Serial Interface Engine (SIE)** - The Serial Interface Engine (SIE) block performs the Parallel to Serial and Serial to Parallel conversion of the USB data. In accordance to the USB 2.0 specification, it performs bit stuffing / un-stuffing and CRC5 / CRC16 generation / checking on the USB data stream.

g. **USB Protocol Engine** - The USB Protocol Engine manages the data stream from the device USB control endpoint. It handles the low level USB protocol (Chapter 9) requests generated by the USB host controller and the commands for controlling the functional parameters of the UART.

h. **FIFO TX Buffer (128 bytes)** - Data from the USB data out endpoint is stored in the FIFO TX buffer and removed from the buffer to the UART transmit register under control of the UART FIFO controller.

i. **FIFO RX Buffer (256 bytes)** - Data from the UART receive register is stored in the FIFO RX buffer prior to being removed by the SIE on a USB request for data from the device data in endpoint.

j. **UART FIFO Controller** - The UART FIFO controller handles the transfer of data between the FIFO RX and TX buffers and the UART transmit and receive registers.
k. UART Controller with Programmable Signal Inversion and High Drive - Together with the UART FIFO Controller the UART Controller handles the transfer of data between the FIFO RX and FIFO TX buffers and the UART transmit and receive registers. It performs a synchronous 7 / 8 bit Parallel to Serial and Serial to Parallel conversion of the data on the RS232 (RS422 and RS485) interface. Control signals supported by UART mode include RTS, CTS, DSR, DTR, DCD and RI. The UART Controller also provides a transmitter enable control signal pin option (TXDEN) to assist with interfacing to RS485 transceivers. RTS / CTS, DSR / DTR and X-On / X-Off handshaking options are also supported. Handshaking, where required, is handled in hardware to ensure fast response times. The UART also supports the RS232 BREAK setting and detection conditions. A new feature, programmable in the internal EEPROM allows the UART signals to each are individually inverted. Another new EEPROM programmable feature allows high signal drive strength to be enabled on the UART interface and CBUS pins.

l. Baud Rate Generator - The Baud Rate Generator provides an x16 clock input to the UART Controller from the 48MHz reference clock and consists of a 14 bit pre scalar and 3 register bits which provide fine tuning of the baud rate (used to divide by a number plus a fraction or "sub-integer"). This determines the Baud Rate of the UART, which is programmable from 183 baud to 3 million baud.

The FT232R [11] supports all standard baud rates and non-standard baud rates from 300 Baud up to 3 Mega baud. Achievable non-standard baud rates are calculated as follows -

Baud Rate = 3000000 / (n + x)

Where n can be any integer between 2 and 16,384 (= 214) and x can be a sub-integer of the value 0, 0.125, 0.25, 0.375, 0.5, 0.625, 0.75, or 0.875. When n = 1, x = 0, i.e. baud rate divisors with values between 1 and 2 are not possible.
This gives achievable baud rates in the range 183.1 baud to 3,000,000 baud. When a non-standard baud rate is required simply pass the required baud rate value to the driver as normal, and the FTDI driver will calculate the required divisor, and set the baud rate. See FTDI application note AN232B-05 for more details.

m. RESET Generator - The integrated Reset Generator Cell provides a reliable power-on reset to the device internal circuitry on power up. A RESET# input pin is provided to allow other devices to reset the FT232R. RESET# can be tied to VCCIO or left unconnected, unless it is a requirement to reset the device from external logic or an external reset generator I.C.

n. Internal EEPROM - The internal EEPROM in the FT232R can be used to store USB Vendor ID (VID), Product ID (PID), device serial number, product description string, and various other USB configuration descriptors. The internal EEPROM is also used to configure the CBUS pin functions.

2.2.4. Personal Computer

Personal Computer with the following features and for the RFID based Library Management System is given below.

- Intel® Pentium® DUAL CPU
- 512MB RAM
- 40GB Hard disk drives
- 1.44MB Floppy disk drives
- Two Serial port
- One Parallel Port
- 3 USB ports

Normally PC has two COM ports. Both COM ports have RS232-type connectors. Many PCs use one each of the DB25 and DB9 RS232 connectors. The COM ports are designated as
COM1 and COM2 and A-type USB serial ports. We can connect the DLP RFID1 Read/Writer communicates with PC through the USB to Serial converter (FTDI drivers).

**Working of RFID LMS**

The hardware details of the DLP RFID1 Read/Writer are as shown in figure. The heart of the system is DLP RFID Reader/Writer which handles the total process of reading/writing the UID on to tag and analyses with the personal computer have the following tasks.

1. Write the book/student information on to the tag
2. Read the book/student information from the tag
3. Add the new books to the library/department
4. Issuing and returning of books
5. Status of the book
6. Database management

The database maintained with MySQL using MATLAB, which is much secured and user friendly.

When books are issued to student, the books are deleted from the department book database and added to the student data base, and also record the issued date and return date of the book on to student database along with student and book information. In the same way to return the books, books are add to department book database and deleted from student data base along with due date fine.

Searching of books using UID will search the information of Book UID, Book Title, Book Author and Book Publisher. Similarly using Student search Book UID, student UID, student Name. All will process and analyzed using RFID Read/Writer by implementing MATLAB GUI for Library Management System easily and efficiently.
REFERENCE


8. Embedded Systems Design using the TI MSP430 Series


11. USB to Serial communication drivers http://www.dlpdesign.com/#Drivers