Realization of active-RC integrators

5.1 Introduction

Integrators are inherently stable networks and are indispensable building blocks in the construction of analog computers and for signal processing purposes. Integrator networks which are advantageous from the viewpoint of IC construction are extensively used for wave shaping applications.54-61

A basic passive-RC circuit1-5 that performs approximately the operation of an integrator is illustrated in Fig. 5.1. A study of this circuit allows one to write the following equation in the time domain

\[ V_0 = \frac{1}{CR} \int (V_i - V_0) \, dt \] ..(5.1)

A study of eqn. (5.1) indicates that the circuit implements integrator function provided the following inequality constraint is satisfied

\[ |V_0| \ll |V_i| \] ..(5.2)
Combining eqns. (5.1) and (5.2), one obtains
\[ V_0 = \frac{1}{RC} \int V_i dt \quad \ldots(5.3) \]

Thus, the circuit functions properly as an integrator if inequality expressed by (5.2) is satisfied.

If \( V_i(t) \) represents a step function

\[ i.e. \quad V_i(t) = \begin{cases} 0 & t < 0 \\ 1 & t > 0 \end{cases} \quad \ldots(5.4) \]

Then ideally we have
\[ V_0(t) = \int_0^t dt = t \quad \ldots(5.5) \]

The eqn. (5.5) is represented by dashed curve of Fig. 5.2. However, experimental response of the circuit to a unit step function is given by the solid curve of Fig. 5.2. Hence approximation is valid for small values of time. When \( V_0 \) becomes large, inequality (5.2) is no longer valid and eqn. (5.3) is in an error. The improvement in the passive integrator response can be achieved by increasing the passive component values but, however, the increase in the value of \( R \) or \( C \) or both will reduce the signal-to-noise ratio which is undesirable besides the increase in the value of passive components itself is undesirable in IC technology.
because large value components are not economically fabricated in this technology.

Because of these problems encountered in the passive-RC integrator networks, a need to develop active-RC integrator configurations which realize a large time-constant with tunable facility and employ a grounded capacitor has been felt by the circuit designers. The active-RC tunable integrator circuits are well known for their wide range of applications in the fields of signal processing and wave shaping.

In this chapter, CCII, FTFN-based active-RC integrator circuits are proposed. Some of the proposed circuits have the additional advantage of having dual-input facility and high input impedance. The novelities of the proposed circuits are (1) usage of grounded capacitor (2) tunable time-constant, (3) large value of time-constant without using large value components (4) suitable for low frequency applications, and (5) high input impedance. It needs to be mentioned here that integrator circuits reported in the literature besides yielding low input impedance are suitable for high frequency applications owing to the fact that the time-constant realized by these circuits is very small, but however, large time-constant can be achieved in
these circuits by using the components which have more spread than is desirable in IC design. Besides, the signal to be integrated or shaped will be obscured by using high value components.

5.2 CC II-based single input integrators

Circuit 1.

A new configuration for realizing integrator function using a single second-generation current-conveyor (CC II (+)) and five passive components is shown in the Fig. 5.3. The circuit employs a grounded capacitor and facilitates independent control of time-constant through a grounded resistor. Using the terminal characteristics of a positive CC II, the proposed circuit yields the following voltage transfer ratio:

\[
\frac{V_o}{V_i} = \frac{R_1/R_2 - R_3/R_4}{S C R_1 \left( 1 + R_3/R_4 \right)}
\]

A study of eqn. (5.6) reveals that the transfer function characterizing the integrator network is inherently free from the perfect integrator condition. The time-constant \(T\) of the circuit is given by

\[
T = \frac{C R_1 \left( 1 + R_3/R_4 \right)}{R_1/R_2 - R_3/R_4}
\]
The inequality constraint \((R_1/R_2) > (R_3/R_4)\) imposed by eqn. (5.7) for the realization of positive time-constant can be easily realized in practice. The tuning of the time-constant can be accomplished by adjusting the magnitude of any of the components involved in the expression representing the time-constant. It is feasible to tune the time-constant to the desired value by adjusting either of the grounded resistors \(R_2\) or \(R_4\) leading to voltage and microprocessor control of the circuit. A large value of time-constant can be achieved without employing large value components by adjusting the difference term \((R_1/R_2 - R_3/R_4)\) to a small value. However, the increase in the value of time-constant is at the cost of higher sensitivities. Since the circuit can realize large value of time-constant, therefore, the circuit is suitable for low frequency applications.

Circuit 2

A novel integrator circuit\(^5\) using a single CCII(+) and four passive components is presented in Fig.5.4. The circuit employs a grounded capacitor and is free from perfect integration condition. The time-constant of the circuit is independently tunable through a grounded resistor. A straightforward analysis of the circuit yields the following voltage transfer function:
The time-constant $T$ is given by:

$$T = CR_3(1 + R_1/R_2) \quad \ldots (5.9)$$

An examination of eqn. (5.9) reveals that tunability of the time-constant is achievable through all the passive elements employed in the circuit but it is feasible to adjust the value of $T$ through grounded resistor $R_2$ or $R_3$ which also facilities voltage and microprocessor tunability of the circuit parameter.

Circuit 3

The inverting integrator circuit proposed in Fig. 5.5 employs a single CCII(+), a single resistor and a grounded capacitor. The circuit is free from realizability condition and time-constant is tunable through floating resistor $R$ and grounded capacitor $C$. The expressions for voltage transfer function and time-constant $T$ are obtained as:

$$\frac{V_o}{V_i} = -\frac{1}{SCR} \quad \ldots (5.10)$$

$$T = CR \quad \ldots (5.11)$$
The circuit can be used for high frequency applications because the value of time-constant the circuit can realize without using large value components is small.

Circuit 4

The CC II-based integrator circuit using two active devices and four grounded passive elements is forwarded in Fig. 5.6. The circuit utilizes a grounded capacitor and is free from condition of realizability. The circuit also enjoys the feature of independent control of time-constant through grounded resistors. The time-constant of the circuit can be linearly enhanced to a large value through grounded resistors \( R_1 \) or \( R_3 \). Thus, the circuit can be utilized for low frequency applications. The expressions for voltage transfer ratio and time-constant are manipulated as follows:

\[
\frac{V_0}{V_i} = \frac{1}{sc \frac{R_1 R_3}{R_2}} \quad \ldots (5.12)
\]

\[
T = C \frac{R_1 R_3}{R_2} \quad \ldots (5.13)
\]

Circuit 5

The integrator circuit advanced in Fig. 5.7 is built around two CC II(+) and five passive components. The
circuit employs a grounded capacitor and is free from perfect integration condition, therefore, its time-constant is controllable besides $C$ through grounded resistors $R_2$, $R_3$ and $R_4$. The dependence of the time-constant on grounded resistors can also lead to voltage and microprocessor control of the circuit. A routine analysis of the circuit leads to the following expressions for voltage transfer ratio and time-constant $T$:

$$\frac{V_o}{V_i} = \frac{R_{1}R_{3}+R_{2}R_{3}-R_{2}R_{4}}{scR_{4}(R_{1}+R_{2})}$$  \hspace{1cm} (5.14)

$$T = \frac{cR_{3}R_{4}(R_{1}+R_{2})}{R_{1}R_{3}+R_{2}R_{3}-R_{2}R_{4}}$$  \hspace{1cm} (5.15)

An examination of eqn. (5.15) reveals that a large value of time-constant can be achieved without employing large value components by adjusting the difference term $R_3(R_1+R_2)-R_2R_4$ to a small value.

Circuit 6

The integrator circuit reported in Fig.5.8 is constructed around two CC IIs(+) and four passive elements. The circuit besides using a grounded capacitor is free from realizability condition. The circuit also facilitates independent control of time-constant
through grounded resistor $R_3$. The analysis of the circuit yields the following voltage transfer ratio:

\[
\frac{V_o}{V_i} = \frac{R_2}{sc R_1(R_3-R_2)} \quad \ldots (5.16)
\]

The time-constant $T$ is given by

\[
T = \frac{CR_1 (R_3-R_2)}{R_2} \quad \ldots (5.17)
\]

The eqn.(5.17) suggests that the circuit implements positive integrator function if $R_3 > R_2$ which of course can easily be implemented in practice.

5.3 CCII-based dual-input integrators

Circuit 7

A novel dual-input integrator circuit based on CCII(+) is proposed in Fig.5.9. The circuit comprises of two active devices and five passive components. The circuit has dual-input facility and realizes large value of time-constant without much increase in the value of passive components. Using the terminal characteristics of positive second-generation current-conveyor, the voltage transfer function can be derived as follows:
The realizability condition for the dual-input integrator and the time-constant are evaluated as under:

\[
\frac{R_3}{R_1} = 1 
\]

\[
T = CR_2 (1 + R_3/R_4) 
\]

The eqn. (5.20) indicates that the time-constant of the circuit can be linearly enhanced through C and R₂ without upsetting eqn. (5.19). One can select \( R_3/R_4 \gg 1 \) so as to obtain large enhancement in time-constant. For example, one can select \( R_3 \) in kilo-ohm range whereas \( R_4 \) can be chosen in ohm range to obtain an enhancement of the order of hundreds. The dependence of time-constant \( T \) on grounded resistor \( R_2 \) leads to the electronic and microprocessor controlled operation of the circuit.

Circuit 8

A dual-input high impedance integrator circuit based on CC II(+) is advanced in Fig 5.10. The circuit comprises of two active devices and three passive components. The merits of the circuit are: dual-input facility with both the inputs essentially offering in finite impedance, independent control of time-constant.
through grounded capacitor and least component count. The analysis of the circuit allows one to write the following expressions for voltage transfer ratio, realizability condition and time-constant.

\[
\frac{V_0}{V_2 - V_1 \frac{R_2}{R_1}} = \frac{1}{sC_R^2} \quad \ldots(5.21)
\]

\[
\frac{R_2}{R_1} = 1 \quad \ldots(5.22)
\]

\[
T = CR_2 \quad \ldots(5.23)
\]

The eqn. (5.23) reveals that the time-constant \( T \) is tunable through grounded capacitor \( C \) independent of realizability condition.

**Circuit 9**

The CC II(+)—based realization scheme comprising two active devices and three passive components implements dual-input integrator function and is presented in Fig.5.11. The circuit facilities tuning of time-constant through floating resistors \( R_1 \) and \( R_2 \) and grounded capacitor \( C \). The remarkable feature of the circuit is that it is inherently free from the integration condition besides enjoying less component count. Being free from the realizability condition the circuit
has offered saving in components. The voltage transfer ratio for the circuit is derived as:

\[
\frac{V_0}{V_2 - V_1} = -\frac{1}{\text{sc} \frac{R_1 R_2}{R_1 + R_2}} \quad \text{...(5.24)}
\]

The time-constant is obtained as:

\[
T = C \frac{R_1 R_2}{R_1 + R_2} \quad \text{...(5.25)}
\]

Circuit 10

A new dual-input integrator circuit given in Fig.5.12 comprises of a single CC II(+) and two passive components only. The circuit has the advantages of: dual-input capability, least component count; inherently free from the realizability condition and having tuning facility of time constant through grounded capacitor and floating resistor. The voltage transfer ratio for the circuit is obtained as:

\[
\frac{V_0}{V_2 - V_1} = \frac{1}{\text{sc} R} \quad \text{...(5.26)}
\]

and time-constant \(T\) is given by:

\[
T = CR \quad \text{...(5.27)}
\]
A new scheme for realization of dual-input integrator function is forwarded in Fig. 5.13. The scheme involves two CC IIIs(+) and three passive components. The circuit performance factor $T$ is tunable only through grounded capacitor $C$. The analysis of the circuit leads to the following voltage transfer ratio:

$$\frac{V_0}{V_1 - V_2} = \frac{1}{R_1/R_2} \quad \text{Sc} \quad (5.28)$$

The condition for integration and time-constant $T$ are given by:

Realizability condition, $R_1/R_2 = 1$ \quad \text{(5.29)}

Time - constant, $T = C R_1$ \quad \text{(5.30)}

A new dual-input CC II(+) based integrator configuration depicted in Fig. 5.14 employs two active devices and four passive elements. The time-constant $T$ is tunable through grounded capacitor $C$ and floating resistor $R_3$. The time-constant $T$ can be tuned over a wide range through resistor $R_3$ without much spread in the value of grounded capacitor $C$. Usual analysis of the circuit yields the following equations of interest:
Realizability condition, $R_1/R_2 = 1$  

Time - constant, $T = CR_3$  

Circuit 13

A new CC II-based active RC dual-input integrator realization scheme is proposed in Fig.5.15. The circuit has been developed using two active devices and four passive components. The novel features of the circuit are: free from realizability condition; dual-input capability; very large time-constant without requiring large values of $R$ and $C$ and one of the inputs exhibits essentially infinite input impedance. Usual analysis of the circuit yields the following transfer function:

$$\frac{V_0}{V_1 - V_2} = \frac{1}{sCR_1R_2}$$  

The integrator time-constant $T$ is given by:

$$T = CR_1\left(1 + \frac{R_3}{2R_2}\right)$$  

The eqn.(5.35) indicates that the time-constant is tunable over a wide range and can be linearly adjusted.
to large value through resistor $R_1$. By selecting the ratio $R_3/2R_2 \gg 1$, the circuit can achieve large value of time-constant.

5.4 FTFN-based single input integrator

Circuit 14

A single-input integrator network based on FTFN(+) is proposed utilizing a single active device and four passive components and is given in Fig. 5.16. The time-constant is adjustable through all the passive elements employed in the configuration as it is free from integration condition. However, it is feasible to tune the time-constant through grounded resistor $R_3$ leading to the voltage and microprocessor controlled operation of the circuit. The circuit has an interesting feature of being free from the realizability condition leading to the saving in components and to the simplified design procedure. The analysis of the circuit leads to the following voltage transfer ratio:

$$\frac{V_0}{V_i} = -\frac{R_2 + R_3}{sc R_1 R_3}$$

The time-constant $T$ is given by:
T = C \frac{R_1 R_3}{R_2 + R_3} \ldots (5.37)

Circuit 15

The single input integrator configuration depicted in Fig. 5.17 uses a single FTFN(+) and four passive components. The circuit is free from the realizability condition and hence the time-constant of the circuit is tunable through all the passive components present in the circuit. A large value of time-constant can be realized by adjusting the term \( \frac{R_3}{R_2} \gg 1 \) as is evident from eqn. (5.39). The time-constant can also be linearly enhanced through floating resistor \( R_1 \) and \( C \). A routine analysis of the circuit leads to the following equations of interest.

\[
\frac{V_v}{V_i} = -\frac{1}{sc R_1 (1 + R_3/R_2)} \ldots (5.38)
\]

\[
T = C \frac{R_1}{1 + R_3/R_2} \ldots (5.39)
\]

A study of eqn. (5.39) reveals that the term \( (1 + R_3/R_2) \) acts as a multiplier and thus helps in achieving large value of time-constant. Thus, large time-constant is realized without using such components whose magnitude exceeds the permissible limits imposed by IC fabrication. As a result the circuit is
suitable for IC construction.

Circuit 16

A novel realization scheme comprising a single FTFN(+) and four passive components implements an integrator function and is shown in Fig. 5.18. The time-constant of the circuit is tunable through all the passive elements involved in the circuit. However, the main features of the circuit are as follows:

i) The circuit is free from the realizability condition leading to simplified design procedure and saving in components.

ii) The time-constant of the circuit is linearly tunable to a large extent through a grounded resistor $R_3$ leading to voltage and microprocessor controlled operation of the circuit.

A simple analysis of the circuit leads to the following equations of interest:

$$\frac{V_o}{V_i} = \frac{1}{scR_3(1 + R_1/R_2)} \quad (5.40)$$

$$T = cR_3(1 + R_1/R_2) \quad (5.41)$$
5.5 Sensitivity Considerations

The T-sensitivities of the integrator circuits forwarded in this chapter are given in Table 5.5.

Table 5.5: Sensitivities with respect to passive components.

<table>
<thead>
<tr>
<th>Circuit No.</th>
<th>C</th>
<th>R₁</th>
<th>R₂</th>
<th>R₃</th>
<th>R₄</th>
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<td>1</td>
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<td>1</td>
<td></td>
<td></td>
<td></td>
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<tr>
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<td></td>
<td></td>
</tr>
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<td>1</td>
<td></td>
<td>0</td>
<td>0</td>
</tr>
<tr>
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<td>1</td>
<td>1</td>
<td></td>
<td>-1</td>
<td>0</td>
</tr>
<tr>
<td>5</td>
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<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>1</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>1</td>
<td>0</td>
<td></td>
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</tr>
</tbody>
</table>
It is obvious from the examination of T-sensitivity that the circuits in general possess low sensitivities.
5.6 Experimental results

The integrator circuits of Chapter 5 have been experimentally tested for $V_{cc} = \pm 15V$. A square wave of amplitude 200 mv has been applied to the circuits and the triangular waveforms produced by integrator circuits have been photographed. The circuit 1 is tested for $C = 0.01\mu F$, $R_1 = 5.6k$, $R_2 = 1.2k$, $R_3 = 4.7k$ and $R_4 = 4.7k$ and output waveform obtained at 45KH$\_2$ is shown in Fig. 5.19a. The circuit 2 employs components of values $R_1 = R_2 = 500\Omega$, $R_3 = 1.2k$ and $C = 0.01\mu F$ and the output waveform obtained at 34KH$\_2$ is shown in Fig. 5.19b. The circuit 3 is tested for $C = 0.01\mu F$ and $R_1 = 1.2k$ and output triangular waveform is obtained as shown in Fig. 5.19c for frequency of 80KH$\_2$. The Circuit 4 is tested using the component values, $C = 0.01\mu F$, $R_1 = R_2 = 4.7$ and $R_3 = 1.2$ and the output waveform obtained at 90 KH$\_2$ is shown in Fig 5.19d. The circuit 5 is tested for $C = 0.01\mu F$, $R_1 = 4.7k$, $R_2 = 4.7k$, $R_3 = 560\Omega$ and $R_4 = 560\Omega$ and its output waveform at 13 KH$\_2$ is shown in Fig. 5.19e. The Circuit 6 is tested for $R_1 = R_2 = 560\Omega$, $R_3 = 1.2k$ and $C = 0.01\mu F$ and the output waveform is shown in Fig. 5.20a for a frequency of 40KHz. The circuit 7 is tested for one of its inputs grounded and resistor values as $R_2 = R_3 = 7.7k$, $R_3 = 560\Omega$, $R_4 = 560\Omega$ and $C = 0.1\mu F$ and the output waveform
obtained for 10 KH\(_2\) is shown in Fig. 5.20b. The circuit 8 is tested for \(R_2 = 560\Omega\) \(C = 0.01\mu F\) and integrated waveform obtained at 15KH\(_2\) is shown in Fig. 5.20c. The circuit 9 is tested for \(C = 0.01\mu F\) and \(R_1 = 1.2\ k\) and the output waveform obtained at 60 KH\(_2\) is shown in Fig. 5.20d. The circuit 10 is tested for \(c = 0.01\mu F\), and \(R = 1.2\ k\) and output waveform obtained at 90KH\(_2\) is shown in Fig. 5.20e. The Circuit 11 is tested for \(c = 0.01\mu F\), and \(R_1 = R_2 = 560\Omega\) and output waveform depicted in Fig. 5.21a is obtained at 9KH\(_2\). The circuit 12 has been put to experimentation for \(R_1 = R_2 = 4.7k\), \(R_3 = 560\Omega\) and \(C = 0.01\mu F\) and the output waveform of Fig. 5.21b is obtained at 140KH\(_2\). The circuit 13 is tested for \(R_1 = R_2 = R_3 = 1.2k\) and \(C = 0.01\mu F\) and the output waveform is obtained at 80 KH\(_2\) which is shown in Fig. 5.21c. It is noteworthy here that the passive components chosen for experimental study purposes have tolerances \(\pm 5\%\).
Fig. 5.1

Fig. 5.2