CHAPTER 8
HARDWARE IMPLEMENTATION
KVAr CONTROL SYSTEM AND COMPONENTS
8.1 Introduction:

This chapter describes the various components for KVAR sensing used in the controller. The basic difference between SVC and proposed KVAR controller is that former handles the voltage regulation problem through TSC-TCR scheme while the latter performs smooth control with exact matching of reactive power resulting in improved voltage. This facilitates compensation of (lagging) reactive power by TSC-TCR scheme termed as SVC (KVAR controller). It includes KVAR sensor, ADC converter, zero crossing detectors, gate pulse generation for thyristor controlled reactor as well as capacitor switching ON/OFF circuit with the help of microcontroller 89C51. The block diagram and its implementation in the form of a TSC-TCR type SVC on 11KV/433V, DY11, 125KVA, 3phase, 50Hz transformer at Walchand College has been brought out in subsequent sections.

8.2 General Schematic Diagram of SVC cum KVAR Controller:
At the point of common coupling, on the a 125 KVA transformer, all the laboratory loads are connected as explained earlier in Chapter -3.3 (Study of Existing System). The actual KVAR at PCC is found by sensing current and voltage through CT and PT. This KVAR sensor gives the output current signal in the range of 4-20mA. Then by using I to V converter current signal is transformed in to 0-5 volts d. c. and given to ADC, which ultimately converts this signal in to digital signal compatible for acceptance by microcontroller. Based upon this KVAR value, switching of capacitor bank steps takes place. The excess leading KVAR is absorbed by TCR block for which firing angle (\(\alpha\)) timings are generated by microcontrollers. Details of each block are explained in the following sections.

8.3 KVAr Measuring System :

This measuring system provides necessary inputs for SVC controller to initiate appropriate control actions. The generation of a VAR signal is based up on sensing the reactive power either by 3-phase 3-wire or 3-phase 4-wire system through CTs of 300/5 Amp and voltage signals.

![Diagram of 3 Phase 4 Wire System](image-url)
The CORNEL4380 is a multifunction meter which displays the various parameters after measuring for monitoring purpose as follows.

It gives digital display of various system parameters such as all line voltages, line currents, active and reactive powers (average, as well as per phase) and phase angle in degrees. It has two analog outputs of 0-1mA and 0-20mA which can be programmed to provide as lead/lag and KVAR signal. This 4-20 mA current KVAR signal can be converted into 0-5 V d. c. signal.

8.4 I-V Converter:

4-20 mA current signal obtained through sensor is converted into 0-5 volt d. c. by using op-amp. This 0-5 volt d. c. signal is proportional to 0-100 KVAR lagging. This analog signal is once again converted to digital by using 0808 ADC.
It is an 8-channel input IC.
Channels CH-3 to CH-7 are grounded (Pins – 1, 2, 3, 4, and 5)
Three analog inputs are given to CH-1 and CH-0 (Pins 27 and 26)
SOC – Start of conversion – Pin -6
EOC – End of conversion – Pin -7
OE – Output enable – Pin -9
Clock input of 200 KHz – Pin-10 (This clock has been generated by timer IC555)
Channel CH-2 connected to a pot, which given a analog signal for setting the KVAR externally. This facilitates operator intervention for setting of reactive power to leading side at PCC which in turn will take care of inductive power drawn by transformer. Ultimately it can give rise to exact matching of reactive power on HT side also so as to maintain power factor near unity at the metering point.

The output of ADC varies from 00h to FFh for input variation of 0-5 volt d. c. (o. e. 100kVAR lag) this numerical hex value gives the exact
requirement of leading KVAR. This value of KVAR is used for capacitor switching strategy. Resultant switched capacitor KVAR is purposely kept on the leading side. This leading KVAR is then compensated by adjusting the conduction duration $\sigma$ in the thyristor controlled reactor.

8.6 Zero Crossing Detection of Line Voltages:

The entire control and switching strategy for both TCR and capacitor bank respectively depend on the instant of zero crossing of the a. c. supply voltage. The three phase a. c. signals are derived from three PTs followed by comparator (ILLM324) and zener diode. The output will be a square pulse at 50 Hz.

8.7 TCR- Thyristor controlled reactor

The air cored reactors as designed in the Chapter 2.2.2 are connected in delta as shown in fig 8.6. Instead of thyristors, phase
controlled solid state relays (SSR’s) are used. They have inbuilt snubber circuit and optocoupler. These are four terminal devices upper two terminals are used for current terminals and lower two are used for providing gate triggered pulses with ± marketings. The two coils are arranged in series, so that applied line voltage of 440 V is divided in to 220 volts each. As the firing angle increases beyond $90^0$ by an angle of $\alpha$, the magnitude of fundamental component goes on varying as shown in fig. 5.5. Lagging KVAR is calculated by microcontroller and from lookup tables stored in the memory corresponding firing angle $\alpha$ is obtained. The lookup table provides the information regarding required KVAR and the corresponding firing angle $\alpha$.

8.8 Thyristor Switched Capacitor Bank:

![Diagram of Thyristor Controlled Reactor](FIG.8.6-THYRISTOR CONTROLLED REACTOR)

- L1 = 310mH, 10.6ohms
- L2 = 332mH, 11.5ohms
- L3 = 316mH, 10.87ohms
- L4 = 332mH, 10.9ohms
- L5 = 325mH, 11.23ohms
- L6 = 329mH, 10.7ohms
The capacitor banks are arranged in binary sequence form i.e. in the multiplicity of 16, 8, 4, 2, 1 code. Therefore, $C_5 = 16C_1$; $C_4 = 8C_1$; $C_3 = 4C_1$, and $C_2 = 2C_1$

**8.9 LCD Display:**
A conventional LCD display has been interfaced through the port-1. It displays the firing angle $\alpha$ for TCR.

**8.10 Microcontroller 89C51:**
This microcontroller has three timers. These are used for generation of time delay pulses.

*Pin configuration used:*
- P1 – Port 1 for ADC data bytes 1, 2, 3, 4, 5, 6, 7
- P0 – Port 0 for LCD
- 30, 31, 32 for output enable, SOC/ALE and EOC of ADC
24, 25, 26, 27, 28 – For capacitor switching lines
21, 22, 23 – LCD control lines
15, 16, 17 – are TCR thyristor control pulses

**Brief Algorithm:**

- Read lagging KVAR from system
  - Select channel CH-2
  - Convert analog signal to digital form
  - Find the KVAR required from capacitor
  - Say KVARc
- Read leading KVAR set from channel
  - Select channel CH-1
  - Convert analog set point to digital form
  - Find corresponding leading KVAR to be set a PCC, say KVARset
- Do the addition of KVARc + KVARset
- For the requirement of capacitor KVAR. Find the appropriate capacitor ON switching while selecting capacitor ON switching and keep the total switched capacitor KVARc slightly higher than lagging KVAR lag.
  i. e. \((KVAR_c - KVAR_{lag}) \leq 2.5 \text{ KVAR} < 0\)
- Generate the corresponding control signals for TCR.
- Repeat the process periodically, at every two minutes.
8.11 Experimental Results:

All the above components are fabricated, tested and implemented at PCC of a 125 KVA, 433 volts distribution transformer. The load was increased from 30 Amp to 150 Amp. It is observed that without controller p.f. varies from 0.8 to 0.85 while with developed static Var compensator, it was in between 0.99 lag to 0.99 lead. The details of the system performance with and without SVC are given in the Table No.8.1 and Table No. 8.2 respectively.

Table 8.1 System performance without SVC

<table>
<thead>
<tr>
<th>Sr. No.</th>
<th>Avg. Load Current In Amp</th>
<th>Avg. P.F.</th>
<th>Avg. Voltage In volts</th>
<th>Active Power In Kw</th>
<th>Reactive Power In KVAr</th>
<th>Apparent Power In KVA</th>
<th>Percent Voltage Regulation</th>
<th>Losses In watts</th>
<th>Feeder Efficiency In %</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>30</td>
<td>0.8</td>
<td>430</td>
<td>17.9</td>
<td>13.4</td>
<td>22.36</td>
<td>0.66</td>
<td>48.6</td>
<td>99.69</td>
</tr>
<tr>
<td>2</td>
<td>60</td>
<td>0.82</td>
<td>428</td>
<td>36.4</td>
<td>25.35</td>
<td>44.35</td>
<td>1.16</td>
<td>194.4</td>
<td>99.39</td>
</tr>
<tr>
<td>3</td>
<td>90</td>
<td>0.83</td>
<td>426</td>
<td>55.1</td>
<td>37.19</td>
<td>66.48</td>
<td>1.63</td>
<td>437.4</td>
<td>99.11</td>
</tr>
<tr>
<td>4</td>
<td>110</td>
<td>0.83</td>
<td>424</td>
<td>67.0</td>
<td>45.24</td>
<td>80.84</td>
<td>2.09</td>
<td>653.4</td>
<td>98.94</td>
</tr>
<tr>
<td>5</td>
<td>135</td>
<td>0.84</td>
<td>422</td>
<td>82.8</td>
<td>53.28</td>
<td>98.46</td>
<td>2.56</td>
<td>984.1</td>
<td>98.73</td>
</tr>
<tr>
<td>6</td>
<td>150</td>
<td>0.85</td>
<td>419</td>
<td>92.5</td>
<td>56.6</td>
<td>108.44</td>
<td>3.25</td>
<td>1215</td>
<td>98.48</td>
</tr>
</tbody>
</table>
### Table 8.2 System performance with SVC

<table>
<thead>
<tr>
<th>Sr. No.</th>
<th>Load Current In Amps</th>
<th>Capacitor Bank steps Used</th>
<th>TCR Value KVAR</th>
<th>TCR Current Amps</th>
<th>Line Losses In watts</th>
<th>PCC Voltage In Volts</th>
<th>Percent Voltage Regulation</th>
<th>Feeder Efficiency In %</th>
<th>Increased Load Capability In Amps</th>
<th>KVA Relief</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>24</td>
<td>10+5</td>
<td>1.6</td>
<td>2.5</td>
<td>31</td>
<td>432</td>
<td>0.23</td>
<td>99.8</td>
<td>6</td>
<td>4.46</td>
</tr>
<tr>
<td>2</td>
<td>49</td>
<td>20+5</td>
<td>0.0</td>
<td>0.1</td>
<td>130</td>
<td>431</td>
<td>0.46</td>
<td>99.27</td>
<td>11</td>
<td>7.95</td>
</tr>
<tr>
<td>3</td>
<td>74</td>
<td>20+10+5+2.5</td>
<td>0.39</td>
<td>0.5</td>
<td>295</td>
<td>430</td>
<td>0.69</td>
<td>99.15</td>
<td>16</td>
<td>11.38</td>
</tr>
<tr>
<td>4</td>
<td>91</td>
<td>40+5</td>
<td>0.0</td>
<td>0.1</td>
<td>447</td>
<td>429</td>
<td>0.9</td>
<td>99.00</td>
<td>19</td>
<td>13.84</td>
</tr>
<tr>
<td>5</td>
<td>113</td>
<td>40+10+5</td>
<td>1.62</td>
<td>2.7</td>
<td>689</td>
<td>428</td>
<td>1.15</td>
<td>98.9</td>
<td>22</td>
<td>15.66</td>
</tr>
<tr>
<td>6</td>
<td>127</td>
<td>40+10+5+2.5</td>
<td>0.9</td>
<td>1.5</td>
<td>870</td>
<td>426</td>
<td>1.61</td>
<td>98.8</td>
<td>23</td>
<td>15.94</td>
</tr>
</tbody>
</table>

Note: This table of values is for the same 6 cases of active powers considered in Table 8.1
**Fig. 8.8 Voltage Improvement**

**Fig. 8.9 Voltage Regulation**
Fig. 8.10 Feeder Losses with and without SVC

Fig. 8.11 Feeder Efficiency
8.12 Discussion on Experimental Results:

An experimental setup is considered for the earlier selected six different loading conditions on the distribution transformers, 3Ø phase, 50 Hz, 125 KVA, Dy 11, 11 KV/433 volts. For the load increase of 30 Amp to 150 Amp, the actual power factor variation was observed to be 0.8 to 0.85 lagging corresponding to with the apparent power variation between 25 to 108 KVA. The desired power factor at the point of common coupling has been set in the range of 0.99 lag to 0.99 lead. This is the narrow band considered for regulation purpose so as to maintain the resultant power factor nearer to unity always for the entire range of load variation. The values recorded are presented in Tables 8.1 and 8.2. The voltage improvement, reduction in regulation, reduction in feeder losses, efficiency of feeder and relief obtained in KVA demand are depicted in Fig. 8.1 to Fig. 8.5 respectively.

Fig. 8.12 KVA Relief with SVC
8.13 Economic Justification:

In the college campus installation MSEDEL has been imposing penalties due to poor power factor and excessive maximum demand. The scheme that is proposed eliminates these penalties and college can avail the benefits of incentives by maintaining the power factor nearer to unity. On an average the college is paying the penalties to the tune of Rs 25000/- per month. The overall installation cost of the proposed scheme is as follows:

1. Capacitor bank cost having 77.5 KVAR = 8,000/-
2. a) Reactor coils (Six in Number) = (6*15Kg*Rs350 per Kg)
   b) Labour charges = 6500
   
   Total = 38,500/-
3. Solid State Relays (18 in number) = 18*1200 = 21600/-
4. Controller Design & Development = 10,000/-
5. C.T.s and P.T.s and other sensors = 5,000/-
6. Control panel = 10,000/-

   Total Capital investment = 92,600/-
7. Interest on capital investment @ 12% = 11,112/- per year
8. Considering life of expectancy of 10 years, depreciation charges = 10000/- per annum
9. Maintenance charges = 5000/- per annum
10. Total expenditure per year = 118,712/-

Monthly savings due to incentives offered by MSEDCL for improvement in the power factor from .96 to unity p.f. is of 5 to 6
% of the monthly bill. The average monthly bill is around 5 lacks. Hence straight way monthly incentives obtained are of around 17,000/-. Also incentives are obtained due to reduction in maximum demand charges approximately Rs. 3000/-.  

11. Payback period in months = \( \frac{118712}{20000} \approx 6 \) months for the two transformers.

**Hence the payback period for one transformer of 125 KVA capacity comes out to be approximately 12 months only.**

Thus, the proposed scheme is quite beneficial to the college to avoid penalties and to take advantage of the incentives being offer by the MSEDCL. Indeed it is advisable to install such controllers on the other two transformers as well and arrange for centralized co-ordinated control in the campus to realize the full benefits for all the time.

**8.14 Conclusions:**

The hardware implementation with microcontroller and ancillary components for reactive power variation, are presented in this chapter. The general schematic diagram of SVC with microcontroller 89C51 is given highlighting the flow of data from one block to another block. KVR sensing is presented with Cornel 4380 digital multifunction meter, ADC interfacing; ZCD and square wave generation are dealt. The control signals for TCR and switching signals for capacitor steps are specified. The algorithmic steps are given for control purpose both for capacitor bank switching and TCR level maintenance. This entire assembly is installed on LV side of the distribution transformer at the point of common coupling. It is hooked up to the system to carry out the operations in real time mode at a periodicity of every two minutes. For
the sake of comparison, the values are metered and recorded for the same six levels of active power which were considered both in analytical and simulation studies. The results obtained are observed to be closely matching with those reported in the earlier chapters both from analytical and simulation studies.