3. DESIGN OF INSTANT CONTROLLED SWITCHING CIRCUITS

3.1 INTRODUCTION

As discussed in the previous chapter an instant-controlled switching (ICS) circuit is required for switching a circuit or a phase (of load) at a predetermined and precisely set switching instant (SI) on the voltage wave. Different types of ICS circuits developed here for 1-phase as well as 3-phase applications. Initially a digital circuit was designed and realized based on counting of high frequency pulses. An improvement was then made by realizing an analogue circuit for the same purpose which was frequency invariant and much simpler. Finally, a hybrid circuit was evolved which was much more versatile and useful for many other purposes. For the later two types of devices a measurement of phase-angle was needed. To accomplish this a frequency-invariant phase-angle meter was also developed.

3.2 DIGITAL ICS CIRCUIT

A control pulse generated at the required SI or angle, in each cycle of the supply voltage, may be used to trigger a switching device which in turn closes the main power switch. The two possible methods for obtaining such a control pulse are as
follows:

(i) Generating a pulse at the positive zero-crossover instant (PZI) and then delaying it for a known period using a monostable or a delay network.

(ii) Counting, starting from the PZI, a precalculated number of high-frequency (HF) pulses and then generating the control pulse.

In the first method the presence of a monostable may lead to undesirable operation due to noise and stray pulses. Moreover it is difficult to set the delay period precisely. In the proposed scheme, therefore, the latter technique is adopted. The block diagram of the scheme is shown in Fig. 3.1. The counter starts counting the HF (6 KHz) pulses from the PZI. Each pulse at this frequency corresponds to 3° of a 50 Hz cycle and gives a sufficient resolution. Only 6 bits of the binary counters (7493) output are needed for counting the 60 HF pulses corresponding to half of the 50 Hz cycle. The parallel outputs of the counter are connected to a combinational logic block which produces the control pulse at the terminals A, B, C, ..., N after counting the appropriate number of the HF pulses. In order to produce the control pulses at 0°, 30°, 60°, 90°, 120°, 150° and 180°, i.e. after 0, 10, 20, 30, 40, 50 and 60 counts, a combinational logic circuit, comprising of three AND gates (IC chip 7408) is connected at the output of the counter. Only combinational logic has to be changed for triggering at any instant other than the above. Moreover, with the help of different combinational logic, a 3-phase circuit or different circuits can be switched on sequentially.
FIG. 3.1. BLOCK DIAGRAM

H.F. OSCILLATOR

ENABLE CIRCUIT

COUNTER

COMBINATIONAL LOGIC

SELECTOR SWITCH

DRIVER & BUFFER CKT.

POWER SWITCHING BLOCK

FIG. 3.2. POWER SWITCHING BLOCK

SELECTOR SWITCH

DRIVER & BUFFER CIRCUIT

MAIN POWER SWITCHING BLOCK

FIG. 3.3. ENABLE CIRCUIT
The selector switch SI can be set to tap any one of the combinational logic outputs according to the desired SI (Fig. 3.2). This output triggers an auxiliary SCR through a driver and buffer circuit (DBC), which provides the permanent gate supply needed to switch on the triac and keep it on during subsequent cycles. An isolator switch in parallel with the whole switching circuit may be used to replace the switching circuit after the switching-on operation. To ensure that the counter starts counting only from the PZI, an "Enable circuit" is used. It has a pulse-forming circuit (PFC) and a SR flip-flop (FF) as shown in Fig. 3.3. The PFC generates a sharp positive pulse at the PZI of the applied voltage which when allowed (by opening the switch S2) sets the FF through the AND gate and enables the counter to start counting the HF pulses from the PZI.

Experiments were carried out to switch a 50 Hz power supply to a resistive load at different instants in a cycle. Photographic records were obtained (Fig. 3.4) and carefully examined. The SIs were found to be in close agreement with the pre-set values.

3.3 ANALOGUE ICS CIRCUIT

The circuit described in the previous section was basically a delay type of circuit and they are susceptible to variation in power frequency. The same function was realized by an analogue circuit which is not only simpler and cheaper but also independent of frequency variations. The block diagram of the proposed circuit is shown in Fig. 3.5. In order to obtain switching at any required instant or angle, a, first a voltage
Fig. 3.4. Photographs at different switching instants: (a) 0°, (b) 30°, (c) 60°, (d) 90°, (e) 150°, (f) 180°.

Fig. 3.5. Block diagram of the switching circuit.
signal, Va, shifted in phase from the supply voltage by the same angle is produced. The phase shift is accomplished by an AC thyatron-type circuit [12], as shown in Fig. 3.6. The advantage of this circuit is that it can easily give a phase-shifted voltage signal of constant magnitude and any phase-angle between 0 and \( \pi \) (leading or lagging) and can be achieved simply by varying the resistance R. The value of \( a \) is given by

\[
a = 2 \tan^{-1}(wCR) \tag{3.1}
\]

The range of \( a \) can be extended from \( \pi \) to \( 2\pi \) by interchanging, the input terminals of the transformer or of the operational amplifier, or by the positions of C and R. The complete switching circuit is shown in Fig. 3.7. On opening the switch S1, the pulse from the PFC at an angle \( a \) with respect to the supply voltage \( Va \), is passed over to the gate of the auxiliary SCR and it is continuously triggered. This in turn triggers the triac as shown in Fig. 3.8. Thus supply to the load is switched in at the angle 'a'.

To set the switching angle accurately, a simple solid-state phase-angle meter is designed as shown in Fig. 3.9. The phase-difference between two AC signals A and B can be measured in terms of the time elapsed between their PZIs. Sharp positive pulses, corresponding to the PZIs are obtained using a PFC. The pulse A sets and B resets the FF. The phase-difference between A and B is equal to the duration for which the output Q of the FF remains 'high'. This duration can be measured by converting it to a DC level using period-to-voltage converter and measuring it by
Fig. 3.6 AC thyatron-type phase-shifting network and its phasor diagram

Fig. 3.7 Complete switching circuit

Fig. 3.8 Wave shapes at various points of the circuit
a voltmeter. The voltage during this period is amplified, clipped and the average DC voltage measured by a moving-coil instrument (micro-ammeter in series with a high resistance of 30 K-ohms). The timing diagram of the circuit is shown in Fig. 3.10. If "t" is the duration corresponding to the phase difference and "T" the time-period of the input signals then the average DC voltage to be measured depends on the ratio t/T and is independent of the frequency. The output characteristic is shown in Fig. 3.11. The phase-angle meter was tested to confirm that a variation in frequency from 4 Hz to 5 Khz neither affected the accuracy nor the calibration. For the measurement of the power-factor, the normal range of interest lies between 90° leading and 90° lagging. Therefore an inverted B signal can be used instead of B to give the deflection of the voltmeter in the range -180° (leading) to 180° (leading) as shown in Fig. 3.12.

3.4 HYBRID ICS (MASTER-CONTROLLER) CIRCUIT

Different types of firing angle controllers for converters and inverters are available in literature since last three decades. However these firing circuits are either meant for a particular application or are quite complex involving large hardware. A number of techniques for polyphase converter/inverter control had been discussed in detail [13,14]. Le and Berg had reported a 3-phase triggering circuit where three sets of active phase-shifter circuits (PSC) are employed [15]. However each PSC requires four operational amplifiers in addition to some combinational logic gates. Similarly other firing angle
Fig. 3.9 Proposed circuit diagram for the phase-angle measurement.

Fig. 3.10 Waveshapes at different stages. (a) AC signals, (b) output pulses of PFC, (c) output Q of the flip-flop, (d) output of amplifier, (e) clipped and averaged DC voltage.

Fig. 3.11 Characteristic of phase-angle meter.

Fig. 3.12 Characteristic of power-factor meter.
controllers (including the integral-cycle power control/zero-voltage switching) are also reported for three phase systems by phase-locked loop and microprocessor based methods [16,17,18]. In these cases also lengthy circuitry is involved.

The principles of the ICS by the digital and analogue circuits are extended to develop a versatile master-controller circuit (MCC) for different applications. It is equally useful for converters, inverters, choppers, ICS, zero-voltage switching and integral-cycle control using thyristors, BJTs, FETs and MOSFETs etc. in the power circuits. Moreover it is successfully tested as a phase-comparator by phase-sequence detection techniques for realizing various distance characteristics for the protection of the transmission line. It easily controls as well as generates polyphase reference sinewave over wide frequency range (5Hz-40 KHz) which is otherwise difficult to be realized by simple circuits for cycloconverters and PWM inverters in speed control application over a frequency range within 100 Hz [14].

The block diagram of the MCC is shown in Fig. 3.13. Which has phase-shifting or phase-split circuits (PSC) as it is used in analogue ICS circuit (Fig. 3.8). Several phase-shifted signals (leading or lagging) are generated by adding more RC series branches at the secondary of the center-tapped auxiliary transformer (audio-interstage coupling transformer, Delta 13A74A) as shown in Fig. 3.14. Different voltage signals V1, V2 and V3 of required phase-shifts θ1, θ2 and θ3 respectively, are generated with respect to the reference sinusoidal voltage, V. The PFCs give sharp positive pulse at PZIs to set or reset the different
FIG. 3.13. BLOCK DIAGRAM OF MCC.

FIG. 3.14. PSC WITH PHASOR DIAGRAM

FIG. 3.15. M.C.C. IN I.C.S. MODE.
FFs according to the logic combinations. High output of the FF (Q=1), enables the carrier signal (10 KHz) from the oscillator to reach the DBC. Which in turn controls the switching and conduction period of different power semiconductors in the power switching block. The DBC circuit used here is same as shown in Fig. 3.2.

3.5 APPLICATIONS OF THE DESIGNED MCC

The applications of this circuit for various purposes are discussed below for individual cases separately.

3.5.1. ICS mode

Different load circuits or phases of a supply can be switched at the same or at sequentially different SIs (e.g. θ1, θ2, θ3 etc.) with respect to V. The MCC connections for 3-phase or three load-circuits are shown in Fig 3.15. As discussed earlier the generated voltages V1, V2 and V3 are applied to three PFCs. The control pulse of the first PFC at θ1, when allowed (Fb terminal is set to logic '1' level for burst control), sets the first FF as shown in Fig. 3.16. This part of the circuit is same as that of the "enable circuit" used in digital ICS circuit (Fig. 3.3). Now it enables the second FF to set at θ2 and so on. Thus switching takes place sequentially at required SIs only and continuous conduction of thyristors are maintained through the DBC.

3.5.2. Zero-voltage switching mode

In this case power control in both the modes, burst as well
(a) WAVE FORMS FOR I.C.S.

(b) 3-PHASE SUPPLY

FIG. 3.16. POWER SWITCHING BLOCK
as integral-cycle control, are possible. The connections in MCC are same as in Fig. 3.15 except that the burst or ON/OFF control signal at Fb controls the overall conduction period. When Fb goes to low level it resets all the FFs. Hence all thyristors switch off when their respective currents drop to zero (below holding current level).

3.5.3. Chopper control mode

As in previous cases, two AC signals V2 and V3 are generated by the PSC in MCC at the required frequency as shown in Fig. 3.17. The control pulse at Θ2 and Θ3 from the PFCs sets and resets FF corresponding to the PZIs of these signals (Fig. 3.18). The outputs of the FF, go to the main and auxiliary SCRs through the DBC. The variation of phase-difference |Θ3-Θ2| between them is made in accordance with the desired duty-cycle of the chopper. The phase-difference of 90°, 180° and 270° correspond to 25%, 50%, and 75% of duty-cycle respectively. Therefore,

\[
\text{duty-cycle} = 100 \cdot \frac{|Θ3-Θ2|}{2π} \% \tag{3.2}
\]

The frequency control is achieved by varying the frequency of the reference voltage, V from the sinewave oscillator and time-ratio control is achieved by the phase-difference. The phasor position of V2 and V3 vary in between 0 and π, and π and 2π, by varying R2 and R3 respectively in PSC (Fig. 3.14). Thus the duty-cycle can be continuously controlled from 0 to 100%.

3.5.4. Converter/Inverter control mode

For 1-phase and 3-phase converter/inverter bridges four and
**FIG. 3.17.** M.C.C. IN CHOPPER MODE

**FIG. 3.18.** WAVEFORMS FOR CHOPPER.

**FIG. 3.19.** M.C.C. IN CONVERTER/INVERTER MODE.
six switching pulses respectively are required. Fig. 3.19 shows connections in MCC for 3-phase applications in 120° conduction mode. Here θ1, θ2 and θ3 are set at 0°, 120° and 240° and V1, V2 and V3 are applied to the six PFCs. Three PFCs give positive pulses at PZIs while the remaining PFCs give pulses at negative zero-crossover instants. Now these pulses (at 0°, 120°, 240°, 180°, 300° and 60°) set and reset the FFs for the desired duration as shown in Fig. 3.20. Thus they control the triggering pulses reaching the power semiconductor through DBC. The triggering/switching-angle control is accomplished by the variation of phase-angle 'a' of the reference voltage, V by a pre-PSC.

3.5.5. Realization of distance relay characteristics

In case of a long transmission line, the difference in impedance under heavily loaded condition and fault condition is small. But a considerable difference in phase angle exists [19]. Therefore static phase comparator are most suitable for distance protection. Different authors have reported the realization of directional [20] and quadrilateral characteristics [21,22] by the phase-sequence detector (PSD). However the circuits reported by them contain very large number of discrete components and devices such as mixing transformers, replica impedances in the form of reactor coils and large transistorized network. These circuits, therefore, have the inherent drawbacks of more power drainage, lack of compactness and difficulty in realization of large number of non-linear devices and components. The reliability of the
FIG 3.20 WAVEFORMS AND BRIDGE CONFIGURATION.
circuit, which is very important for protective devices, depends upon the proper functioning of all these components and is obviously adversely affected by their large number.

Here the MCC is used in such a way that it works as a versatile static phase-comparator which can realize all the characteristics of the distance relay viz. directional, general-directional, reactance, angle-impedance and general-angle impedance. It dispenses with the use of actual replica-impedances, mixing transformers and a large transistorized network. The design flexibility and ease of practical realization is obtained by simulating continuously adjustable replica impedances instead of actual ones.

A line impedance, \(Z\), seen by the relay is shown on the impedance plane in Fig. 3.21. If the current signal, \(I\), is taken as reference, then the line voltage signal \(V = IZ\), will represent \(Z\). A directional characteristic is given in Fig. 3.22(a). The sequence of replica-impedance signals \(IZ_1\) and \(IZ_2\), \(V\) at the fault or trip condition will be \(IZ_1, V, IZ_2\). A 3-input PSD can distinguish between the fault and normal condition as it is given in circuit I of Fig. 3.23. Similarly the sequence at the fault condition for reactance relay (Fig. 3.23c) is \(IZ'_1, IZ_3-V, IZ'_2\) and is realized by circuit-II of Fig. 3.23. Several other characteristics i.e. general-directional, angle-impedance and general-angle impedance are also realized by detecting the phase-sequence among these signals.

The connections of MCC to realize different relay characteristics are shown in Fig. 3.23. A combination of characteristics (b) and (e) gives a general quadrilateral characteristic as shown.
Figure 3.21 Line impedance, $Z$ seen by relay on impedance plane.

Figure 3.22 Directinal characteristics and inputs to PSD; (a) directinal, (b) general directinal, (c) reactance, (d) angle-impedance, (e) general angle-impedance and (f) general quadarilateral characteristic.
in Fig. 3.22(f). This can be realized by connecting the outputs of circuit-I and II with an AND gate.

With the help of a replica-impedance a current signal is converted into a voltage signal of required magnitude and phase-shift. Here the function of replica impedance is realized separately for versatile control by PFC. The phase-angle of the generated signal is controlled independently by the PSC and magnitude is controlled by the gain of an amplifier (operational-amplifier, 741 in closed-loop mode). A voltage signal in phase with the current is obtained by taking the voltage across the shunt resistance of the secondary of a current transformer (CT). It is applied to the PSC to generate V1, V2 and V3 or IZ1, IZ2 and IZ3 signals respectively as before. A difference amplifier is used instead of the mixing transformers for generating the IZ3-V signal. The PFCs give positive pulses at the PZIs whose sequence has to determined by PSD. Since the operational amplifier in PFC is connected in open loop mode, the magnitude of signals are not much important for PSD. However, except in case of IZ3, the magnitude of the IZ3 decides the phasor position of IZ3-V signal in circuit-II as shown in Fig. 3.23.

Two AND gates and two FFs are connected to make PSD as shown in Fig. 3.24. The pulse from the PFC of V1 sets the first FF while the pulse corresponding to V3 sets the second one for the sequence V1, V3, V2. The output of the PSD, Q2, remains high as long as the above sequence is maintained otherwise low. The relay is tested successfully with an artificial transmission line consisting of eighteen π-sections, for the normal, fault and
FIG. 3.23. M.C.C. IN RELAY MODE.

Q2 HIGH FOR SEQUENCE V₁, V₃, V₂.

FIG. 3.24. PSD CIRCUIT

FIG. 3.25. ARTIFICIAL TRANSMISSION LINE.
thorough-fault conditions. Each section of the transmission line has a series resistance and inductance of 2.1 ohms and 21 mH and a shunt capacitance of 0.04 μF as shown in Fig. 3.25. The zone of protection was extended up to sixteenth section of the line, leaving the last two sections for simulation of thorough faults. The fault was created by using a variable (fault) resistance, Rf to determine the performance of the relay for different locations on R-X plane (Zf+Rf). All the characteristics of the phase comparator are tested successfully. The maximum operating time of the relay is one cycle during which the phase-sequence measurement completes. However it can be reduced to half cycle if another pair of PFCs, PSD and an OR gate are also used. Here PFCs generate the pulse at negative zero-crossover instants instead of PZIs, as it is used in 3-phase converter/inverter circuit (Fig. 3.19 and 3.20). Thus the phase sequence for the fault condition will be detected within one cycle (maximum) by either PSD. Performance of the relay under dynamic/actual conditions can be improved further, replacing RC branch in PSC by a RL branch, to avoid the effects of power system oscillations.