MANAS: the readout chip

A modular design of the readout electronics was required to read large number of readout channels, around one million, associated with the tracking chambers. The main design issues were low noise, high reliability, low unit cost and ease in manufacturing, installation and repair. The charge induced on the cathode pad by a charged particle crossing the detector is very small \( \sim 10 - 200 \text{ fC} \) and must be amplified. The large size of the cathode planes prohibits the dispatching of low level analog signal to the edge of the chambers and raise the noise level. Hence, digitization should occur close to the cathode pads. It was, therefore, decided to use a chip on board design. This required the use of charge amplifiers and multiplexers in the chip to be mounted on the board. The VLSI chip MANAS has been selected for this function. In the following section, a detailed description of the MANAS chip is presented; its design, validation and production were the responsibility of the Indian Groups, SINP, Kolkata and AMU, Aligarh involved in the ALICE Collaboration.

4.1 The Multiplexed ANAlog Signal processor

4.1.1 Introduction

The readout principle for all the tracking stations with the event rate expected at ALICE is based on an analog multiplexed measurement of the charges induced on the cathode pads of the tracking chambers [1].

In a detector, which is fully devoted to the reconstruction of the tracks of particles hitting the pads, it is required to minimize the electronics noise of every channel. The level of the noise should not be higher than \( \sim 5 \times 10^{-3} \) of the total charge measured in a cluster. This corresponds to a typical value \( \sim 1000 \) electrons.

With such considerations and constraints an Application Specific Integrated Circuit (ASIC) design of Very Large Scale Integration (VLSI) chip named MANAS was
designated at the Saha Institute of Nuclear Physics, Kolkata and fabricated at the Semiconductor Complex Limited (SCL), Chandigarh, India using 1.2 μm CMOS technology [2].

4.1.2 Operating principle and architecture
The MANAS chip is the Front-End readout chip for the tracking stations of the Dimuon Spectrometer. The operating principle of MANAS chip is similar to the operating principle of Gassiplex [3]. It consists of 16 input channels and one output channel. Input signals, after processing, are available at output serially via a multiplexer. The outputs corresponding to each input channel are in the form of voltage levels that are a measure of the amount of input charge to that particular channel. Each channel has a Charge Sensitive Amplifier (CSA), a Deconvolution Filter (DF), a Semi Gaussian Shaper (SGS) and a Track & Hold (T/H) stage. MANAS chip also has an Analog Multiplexer (AM) that converts 16 parallel inputs into one serial output.

The schematic diagram of a single channel with all the essential building blocks is shown in Fig. 4.1.

![Fig. 4.1. Operational schematic of a single channel of MANAS chip.](image)

4.1.2.1 Charge Sensitive Amplifier
The essential building block of CSA is an Operational Transconductance Amplifier
(OTA) built around a folded cascade architecture. The reset mechanism of the CSA is implemented by an active-feedback-resistor \((R_f)\). This resistor together with the feedback capacitor \(C_f\) gives a decay time constant of 20 \(\mu\text{sec}\). The CSA is basically a feedback amplifier that integrates the total input charge \((Q)\) onto its feedback capacitor \(C_f\). The decay time constant is given by \(R_fC_f\), which is usually kept much higher than the width of the input current pulse in order to ensure that complete charge collection occurs. The CSA then sees the input signal as a delta function and the resulting output is a slowly decaying step function with a peak amplitude \(Q/C_f\).

4.1.2.2 Deconvolution Filter

A large fraction of total charge is collected in a very short time. The characteristic time constant for the given chambers is of the order of 1 nsec and the signal continues for a much longer time, typically 50 to 100 \(\mu\text{secs}\). The Deconvolution Filter compensates this long tail and passes the signal to the next stage as a decaying step waveform, where the decay is governed by the pole of CSA.

4.1.2.3 Semi Gaussian Shaper

Signal pulse from the DF has an exponential decaying long tail, typically 20 to 30 \(\mu\text{secs}\). This may cause serious problem in case of pulse pile up that alters the pulse amplitude, which is a measure of the total input charge \(Q\). It is, therefore, mandatory to shape the pulses in a way that eliminates long tails, while keeping the maximum amplitudes unaltered. Incidentally, SGS shapes the pulses in a way that eliminates long tails while keeping the maximum amplitudes unaltered.

4.1.2.4 Track & Hold

Track and Hold (T/H) circuit consists of a hold capacitor \(C_h\), unit gain buffer and a switch \(SW\). \(SW\) is normally in the ON position and the voltage across \(C_h\) tracks the input signal from SGS filter. A properly timed clock opens the \(SW\) at the instant when the peak of the input signal arrives. The capacitor \(C_h\), therefore, holds the peak amplitude of the input signal, which is a measure of the total input charge.
4.1.2.5 Multiplexer (MUX)

The Analog Multiplexer (MUX) consists of sixteen switches, from SW1 to SW16. The output of these switches are connected together and this line forms the output of the chip.

The design specifications of a MANAS chip are listed in Table 4.1.

<table>
<thead>
<tr>
<th>Table 4.1 Design specifications of a MANAS chip.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Silicon Area</td>
</tr>
<tr>
<td>Peaking Time</td>
</tr>
<tr>
<td>Noise at 0 pF</td>
</tr>
<tr>
<td>Noise Slope</td>
</tr>
<tr>
<td>Dynamic Range (+)</td>
</tr>
<tr>
<td>Dynamic Range (-)</td>
</tr>
<tr>
<td>Sensitivity (+)</td>
</tr>
<tr>
<td>Sensitivity (-)</td>
</tr>
<tr>
<td>Readout Speed</td>
</tr>
<tr>
<td>Power Consumption</td>
</tr>
<tr>
<td>Temperature Coefficient</td>
</tr>
</tbody>
</table>

The final layout of MANAS chip, based on the design specifications given in Table 4.1, is shown in Fig. 4.2. The description corresponding to each pin of a MANAS chip is presented in Table 4.2.

Fig. 4.2. Final layout of a MANAS chip.
<table>
<thead>
<tr>
<th>Pin</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 - 14</td>
<td>IN 3 - IN 16</td>
<td>Channel signal inputs 3\textsuperscript{rd} to 16\textsuperscript{th} channel</td>
</tr>
<tr>
<td>15</td>
<td>$V_{SSA}$</td>
<td>$V_{SSA} = -2.5 \text{ V};$ analog -ve supply; connect to PCB -ve supply</td>
</tr>
<tr>
<td>16</td>
<td>$I_{\text{biasCSA}}$</td>
<td>100 $\mu$A current bias for CSA module; connect to PCB $V_{DD}$ via $R_{CSA}$</td>
</tr>
<tr>
<td>17</td>
<td>NC</td>
<td>No connection</td>
</tr>
<tr>
<td>18</td>
<td>GND</td>
<td>Floating Pin; connected to PCB ground</td>
</tr>
<tr>
<td>19 - 22</td>
<td>NC</td>
<td>No connection</td>
</tr>
<tr>
<td>23</td>
<td>$I_{\text{biasTHB}}$</td>
<td>20 $\mu$A current bias for TH buffer module; connect to PCB $V_{DD}$ via $R_{THB}$</td>
</tr>
<tr>
<td>24</td>
<td>$V_{DDA}$</td>
<td>$V_{DDA} = +2.5 \text{ V};$ analog +ve supply; connect to PCB $V_{DD}$</td>
</tr>
<tr>
<td>25</td>
<td>$V_{SS}$</td>
<td>$V_{SS} = -2.5 \text{ V};$ connected to the substrate</td>
</tr>
<tr>
<td>26</td>
<td>CLK.OUT</td>
<td>Low = 0 V, High = +2.5 V, Active High; output clock for daisy chaining</td>
</tr>
<tr>
<td>27</td>
<td>CLK.IN</td>
<td>Low = 0 V, High = +2.5 V, Active High, input clock for output multiplexing</td>
</tr>
<tr>
<td>28</td>
<td>CLEAR</td>
<td>Low = 0 V, High = +2.5 V, Active High, clear for output multiplexer and T/H capacitors</td>
</tr>
<tr>
<td>29</td>
<td>GNDD</td>
<td>GNDD = 0 V; digital ground; connect to PCB ground</td>
</tr>
<tr>
<td>30</td>
<td>$V_{SSD}$</td>
<td>$V_{SSD} = -2.5 \text{ V};$ digital -ve supply, connect to PCB -ve supply</td>
</tr>
<tr>
<td>31</td>
<td>$V_{DDD}$</td>
<td>$V_{DDD} = +2.5 \text{ V};$ digital +ve supply; connect to PCB +ve supply</td>
</tr>
<tr>
<td>32</td>
<td>SWAN.OUT</td>
<td>Multiplexed Analog Output</td>
</tr>
<tr>
<td>33</td>
<td>$I_{\text{biasOB}}$</td>
<td>50 $\mu$A current bias for output buffer; connect to PCB $V_{DD}$ via $R_{OB}$</td>
</tr>
<tr>
<td>34</td>
<td>GNDA</td>
<td>Analog ground; connect to PCB ground</td>
</tr>
<tr>
<td>35</td>
<td>$V_{SSA}$</td>
<td>$V_{SSA} = -2.5 \text{ V};$ analog -ve supply; connect to PCB -ve supply</td>
</tr>
<tr>
<td>36</td>
<td>$V_{SS}$</td>
<td>$V_{SS} = -2.5 \text{ V};$ connected to the substrate</td>
</tr>
<tr>
<td>37</td>
<td>NC</td>
<td>No connection</td>
</tr>
<tr>
<td>38</td>
<td>TH.IN</td>
<td>Low = 0 V, High = +2.5 V, High Hold, input for Track &amp; Hold</td>
</tr>
<tr>
<td>39</td>
<td>GND</td>
<td>Floating Pin; connected to PCB ground</td>
</tr>
<tr>
<td>40</td>
<td>$V_{\text{outOFF}}$</td>
<td>$V_{\text{outOFF}} = 0 \text{ V};$ adjustment of pedestal mean level offset</td>
</tr>
<tr>
<td>41</td>
<td>$I_{\text{biasRDS}}$</td>
<td>45 $\mu$A current bias for Resistor, Filter &amp; Shaper; connect to PCB $V_{DD}$ via $R_{RDS}$</td>
</tr>
<tr>
<td>42</td>
<td>$V_{\text{ROFF}}$</td>
<td>$V_{\text{ROFF}} = +0.6 \text{ V};$ to adjust DC level of SWAN.OUT</td>
</tr>
<tr>
<td>43</td>
<td>NC</td>
<td>No connection</td>
</tr>
<tr>
<td>44</td>
<td>CAL.IN</td>
<td>Common calibration input; connected to all the channels via a small series capacitance of 0.2 pF (design value)</td>
</tr>
<tr>
<td>45</td>
<td>GNDA</td>
<td>Analog ground; connect to PCB ground</td>
</tr>
<tr>
<td>46</td>
<td>$V_{DDA}$</td>
<td>$V_{DDA} = +2.5 \text{ V};$ analog +ve supply; connect to PCB +ve supply</td>
</tr>
<tr>
<td>47 - 48</td>
<td>IN 1 - IN 2</td>
<td>Channel signal inputs (1\textsuperscript{st} and 2\textsuperscript{nd} channel)</td>
</tr>
</tbody>
</table>
MANAS is a collaborative effort of SINP - AMU - SCL - UTAC. The job description of each organization is mentioned in Table 4.3.

Table 4.3 Job description of various organizations for fabricating and testing of MANAS.

<table>
<thead>
<tr>
<th>Organization</th>
<th>Job Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>SINP, Kolkata</td>
<td>Front-end design, Circuit simulation, MANAS bias conditions, Automatic Test Board validation, MANAS testing and validation of production batches</td>
</tr>
<tr>
<td>AMU, Aligarh</td>
<td>MANAS testing and validation</td>
</tr>
<tr>
<td>SCL, Chandigarh</td>
<td>Back-end design, Setting-up of Automatic TestBench Wafer Fabrication</td>
</tr>
<tr>
<td>UTAC, Singapore</td>
<td>Wafer testing, packaging and device testing</td>
</tr>
</tbody>
</table>

4.2 MANAS testing

In-house (manual) testing was done on a VME - DAQ based on DATE 3.7 to perform the pedestal and gain measurements of each channel of every device. The main aim of testing of MANAS chips at SINP was to deliver the devices with gain spread $\leq 2.5\%$ [4]. The set up is shown in Fig. 4.3.

Fig. 4.3. Test board set up for testing MANAS chips.
A common input voltage pulse was given to all 16 independent capacitors on test board from pulse generator to generate an input charge for each channel of MANAS.

Four pulse signals were necessary for testing a MANAS chip. One pulse signal was for the input, and three more were necessary for the control signals. These were CLK, T/H and CLEAR. All pulse generators were synchronised by a common trigger from the input pulse generator. A triple output power supply was used for providing ± 2.5 V for MANAS biasing.

The operating points for testing are listed in Table 4.4.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Pin</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{bias\text{CSA}}$</td>
<td>100 µA</td>
<td>#16</td>
</tr>
<tr>
<td>$I_{bias\text{T/H}}$</td>
<td>22 µA</td>
<td>#23</td>
</tr>
<tr>
<td>$I_{bias\text{OB}}$</td>
<td>20 µA</td>
<td>#33</td>
</tr>
<tr>
<td>$I_{bias\text{RDS}}$</td>
<td>39 µA</td>
<td>#41</td>
</tr>
<tr>
<td>$V_{ROFF}$</td>
<td>0.66 V</td>
<td>#42</td>
</tr>
<tr>
<td>$V_{\text{outOFF}}$</td>
<td>100 mV</td>
<td>#40</td>
</tr>
</tbody>
</table>

Operating point is set by varying $I_{bias\text{RDS}}$ and $V_{ROFF}$ as both of these values are expected to affect the gain dispersion. The details of the measurements are given in Table 4.5. It is clear from Table 4.5 that for $I_{bias\text{RDS}} = 39$ µA and $V_{ROFF} = 0.66$ V, RMS/Mean = 2.2 is the minimum achieved value.

**Note:** RMS/Mean is the ratio of the RMS value of the gaussian distribution of the gain of all the channels of a MANAS chip to the mean value of the distribution.

### 4.2.1 Testing of validation batch

In the fourth week of May, 2005 seven thousand MANAS devices, fabricated during 20th to 27th week of 2004 at SCL, were tested and packaged at UTAC, Singapore. A total of four thousand devices were sent to IPN, Orsay for fabrication of MANU cards and the rest were made available to SINP.
Table 4.5 Measurement of RMS/Mean at different $V_{ROFF}$ and $I_{biasRDS}$.

<table>
<thead>
<tr>
<th>$I_{biasRDS}$ ($\mu$A)</th>
<th>RMS/Mean at 100 fC</th>
<th>RMS/Mean at 200 fC</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$V_{ROFF} = 0.6$ V</td>
<td></td>
</tr>
<tr>
<td>39</td>
<td>2.1</td>
<td>2.8</td>
</tr>
<tr>
<td>44</td>
<td>3.0</td>
<td>4.1</td>
</tr>
<tr>
<td>48</td>
<td>4.0</td>
<td>5.1</td>
</tr>
<tr>
<td></td>
<td>$V_{ROFF} = 0.66$ V</td>
<td></td>
</tr>
<tr>
<td>39</td>
<td>1.8</td>
<td>2.2</td>
</tr>
<tr>
<td>44</td>
<td>2.6</td>
<td>3.2</td>
</tr>
<tr>
<td>48</td>
<td>3.6</td>
<td>4.5</td>
</tr>
</tbody>
</table>

These devices were tested at room temperature both at SINP and Orsay in the gain and pedestal windows: (3.8 - 4.4) mV/fC and (60 - 220) mV respectively. It was found at both the places ~ 50 % of the devices had one or two (in few cases even more than two) channels outside the specified gain window (4.1 ± 0.3) mV/fC. This finding was first reported by Jean Peyre from his initial tests [5].

Figs. 4.4 and 4.5 exhibit the results obtained at SINP. It is evident from Fig. 4.4 that there were channels with high and low gains with respect to the gain window.

![Fig. 4.4. Gain distribution of 294 channels observed at SINP.](image)
The pedestal distribution in Fig. 4.5 shows that a few channels were outside the pedestal window.

Fig. 4.5. Pedestal distribution observed at SINP.

This result is quite surprising as these chips qualified in this window on the Automatic Tester whose performance was independently validated in April, 2005.

During validation of Automatic Test Bench (ATB) at UTAC, gain window was selected by testing 50 devices. In this testing, nine devices failed in the DC test. The gain distribution of the remaining 41 devices is exhibited in Fig. 4.6.

Fig. 4.6. Gain distribution observed at ATB, UTAC.
Hence, the good gain distribution observed at ATB was an artifact. This measurement differed from the measurement done at SINP in the following two aspects:

- Pedestal and gain measurements on the ATB were done within 1 msec, which takes about a minute at the SINP lab. Thus, any property which changes over time scale of seconds will not be detected at the ATB.

- Temperature at UTAC was around 22° C - 24° C, while at the SINP lab it was around 28° C. So, any temperature dependant effect will be very substantial in the lab at SINP.

In order to examine the above effects, these devices were tested at high temperature around 50° C. Figs. 4.7 and 4.8 show the swan out of a device at room temperature and high temperature (~ 50° C), respectively.

**Fig. 4.7.** Swan out at 0 pF and 200 pF for a device at room temperature.

**Fig. 4.8.** Swan out at 0 pF and 200 pF for a device at high temperature.
It is clear from Fig. 4.7 that in this device 2nd channel shows low gain at room temperature, whereas Fig. 4.8 reveals that swan out for this channel is absent for 200 fC at high temperatures. Although channel remains functional as it shows the pedestal at high temperature. The swan out of pedestal and gain for another device at room temperature is displayed in Fig. 4.9 and Fig. 4.10 shows the swan out at high temperature. At high temperature three channels do not give any output, whereas the behaviour of these three channels at room temperature is quite satisfactory.

![Pedestal Swan out](image1.png) ![Swan out at 200 fC](image2.png)

**Fig. 4.9.** Swan out at 0 pF and 200 pF for a device at room temperature.

![Pedestal Swan out](image3.png) ![Swan out at 200 fC](image4.png)

**Fig. 4.10.** Swan out at 0 pF and 200 pF for a device at high temperature.

On the other hand, almost 50% of the devices do not exhibit this behaviour at high temperature. The swan out for all the channels of every device was observed and no variation with time was observed. In the case of bad channels, the swan out decreases with time in many cases at room temperature. For example, at the instant
when power was switched on, some bad channels were found to be good ones when observed on oscilloscope. However, this behaviour was not seen at high temperature, where the ambient temperature of the chip was anyway higher. This shows that the observed behaviour was strongly dependent on temperature. The pedestal and gain distributions of good devices at room temperature, i.e., the swan out of all the 16 channels of the chips are present at high temperature and are shown in Fig. 4.11.

![Pedestal and gain distributions of good devices at room temperature.](image)

In order to identify the problem, we investigated the shaper output of the good and bad channels. The outputs are shown in Figs. 4.12 and 4.13.

![Shaper output for a good channel.](image)
From this observation it can be stated that:

- For a good channel the shaper output is higher for higher biasing, which is the expected behaviour. However, for a bad channel the shaper output is lower for higher biasing. This unexpected behaviour seems to indicate a current leakage as it is expected to increase with higher bias voltage. This conclusion is also consistent with the previous observation that outputs of bad channels show a tendency of strong temperature dependence.

In a MANAS, current leakage will affect the Charge Sensitive Amplifier (CSA) stage as this will change the operating point of the amplifier. One probable source of the leakage may be the ESD protection circuit, which is implemented by two back-to-back reversed biased diodes. This circuit is shown in Fig. 4.14.

The circuit simulations showed that DC level of the input to CMOS gate of CSA is maintained around - 1.0 V. Thus, both the diodes are reverse biased with $V_{DD} = + 2.5$ V and $V_{SS} = - 2.5$ V in the ESD protection circuit. We also measured I - V characteristics of the diodes at reverse bias under the following two different conditions:

1. $V_{DD} = + 2.5$ V, $V_{SS}$ open and $V_{in} = 0.0$ V to $+ 3.5$ V
2. $V_{DD}$ open, $V_{SS} = -2.5 \text{ V}$ and $V_{in} = -3.1 \text{ V}$ to 0.0 V

Measurements were done at $25 \pm 1 \degree C$ by using a Picoampere Meter and it was difficult to measure the reverse currents below 50 picoamp. For every set of measurements, $V_{in}$ varied from 0.0 V to $\pm 3.0 \text{ V}$ and then came back to zero. In addition, every current value was measured five times for a given voltage and the mean value is exhibited in Fig. 4.15.

![Fig. 4.14. Schematic of the ESD protection circuit.](image)

![Fig. 4.15. I - V characteristic plots of diodes in ESD protection circuit.](image)

In the plots the red dots show the data points for good channels and the black ones are the data points for the bad channels. The data in the left plot were taken for
condition 1 when the diode P+/N-well became forward biased at + 3.0 V. Similarly, the data in the right plot were taken under condition 2 when the diode N+/P-sub became forward biased at - 3.0 V. From Fig. 4.15 the following conclusions can be drawn:

- Leakage current in the ESD protection circuit is negligibly small (less than 50 pA) for a good channel, whereas in a bad channel this current is at least 2 orders of magnitude higher;

- Leakage current increases with increasing reverse bias voltage;

- Reverse current is always of the same sign. In our measurements it was positive. This can be understood from the fact that one diode has N+ doping and the other has P+ doping. So, the minority carriers also reverse the sign for the back - to - back diodes.

The variation of leakage current with temperature was plotted for condition 2 and \( V_{\text{in}} = - 1.0 \text{ V} \). Fig. 4.16 shows that leakage current increases linearly with temperature and becomes around 50 nA at 50 °C.

![Fig. 4.16. Leakage current variation with temperature for a bad channel.](image)
Circuit simulation of MANAS using spice file extracted from full chip layout provided by the SCL, Chandigarh was carried out and the simulated shaper output for an input charge of 300 fC is shown in Fig. 4.17. It is clear from this figure that the shaper output does not deteriorate up to a temperature of 100 °C. In order to observe the effect of leakage current at CSA stage, we ensured leakage currents of 10, 20, 30 and 50 nA at the CSA stage. Results of these calculations for 20 and 50 nA leakage currents are given in Fig. 4.18 and it is noticed that there is no appreciable effect at 20 nA but the output seems to be affected substantially at 50 nA.

Fig. 4.17. Simulated shaper output for an input charge of 300 fC.

Fig. 4.18. Shaper output at 20 nA (left) and 50 nA (right).
In order to quantify these results, the shaper output as a function of leakage current at high temperature (~ 50°C) is plotted in Fig. 4.19. The figure shows that for a 'leaky' channel the gain may change by more than a factor of five at a high temperature as compared to those at room temperature, where it may have very low leakage current.

![Plot of shaper output vs. leakage current](image)

**Fig. 4.19.** Variation of shaper output with leakage current.

We call a chip as 'good' chip whose swan out exists for all 16 channels at high temperature, while a 'bad' chip has atleast one channel dead at high temperature (refer to Figs 4.8 and 4.10). Absence of swan out at high temperature is because the channels outside the gain window at room temperature has some leakage current, which increases rapidly at high temperature. This leads to the failure of that channel at high temperature.

In order to substantiate the simulation results, leakage currents were measured for randomly selected 50 chips from the faulty 2004 batch. The following measurements were done:

- channelwise gains at room and high temperatures;
- channelwise leakage currents at room and high temperatures.
From the tests of 50 chips at room and high temperatures only 23 good devices were found, i.e., almost 46% devices of this lot were found to work at both room and high temperatures. The gain distributions for all the 50 chips and 27 bad chips are displayed in Fig. 4.20 and Fig. 4.21 shows the gain distribution for 23 good chips.

It may be noticed from Fig. 4.21 that the gain distribution at room temperature for good chips is quite acceptable with RMS/Mean \( \approx 2.5 \% \) and there is not a single channel with gain value outside the gain window. These chips were also tested at high temperature (\( \sim 50 \, ^{\circ}\text{C} \)) and the RMS/Mean ratio was found to be around 3.0 %.
Leakage currents for all 50 chips were measured at high temperature and the result is exhibited in Fig. 4.22 (left). In this figure single grid corresponds to all 16 channels of a MANAS. All the 27 bad chips show substantial leakage currents (~ 20 nA) at the dead channel. Furthermore, the correlation of the leakage current at room and high temperatures for 10 bad chips is shown in Fig. 4.22. At a later point of time this correlation was checked for all the 50 chips. We observed leakage currents lying in the interval: 4 nA - 5 nA at room temperature in the channels whose gains were outside the gain window. However, the leakage currents increase to 25 - 30 nA at high temperatures.

**Fig. 4.22.** Measured leakage currents of 50 MANAS chips at high temperature (left). Correlation of leakage currents at room and high temperatures (right).

Amplification observed in Fig. 4.22 (right) is about 5 times. The correlation of channel gain with leakage current is also plotted in Fig. 4.23. Fig. 4.23 (a) shows the second and third chips. It is evident from the figure that the second chip is a 'good' chip, the gains remain good at room and high temperatures and correspondingly there is no leakage current. The second channel for the third chip is bad as this shows a leakage current of ~ 4 nA at room temperature (in red) and the gain of the channel at room temperature (in green) is surely lower than the others (outside the gain window). At higher temperature the leakage current increases to ~ 30 nA (in blue) and the channel is dead.
In Fig. 4.23 (b), the observations of 14\textsuperscript{th} and 15\textsuperscript{th} chips are presented. The channel gain of the 14\textsuperscript{th} chip is good both at room and high temperatures. Thus, this is a 'good' chip. However, in 7\textsuperscript{th} channel of this chip a small leakage current (≤ 3 nA) at room temperature was found, which increases to 5 nA at a high temperature but this does not have any appreciable effect on gain. This behaviour is consistent with our simulation studies, which has shown that the circuit is robust to leakage currents of 5 nA (Fig 4.19).

![Figure 4.23](image)

**Fig. 4.23.** Correlation of channel gain at room temperature (green) and high temperature (pink) with leakage currents at room temperature (red) and high temperature (blue).

Correlations of the channel gain with leakage current for 25\textsuperscript{th}, 26\textsuperscript{th} and 27\textsuperscript{th} chips are shown in Fig. 4.23 (c). It is noticed that 25\textsuperscript{th} chip is 'bad' in usual sense with
11\textsuperscript{th} and 13\textsuperscript{th} channels showing lower gain at room temperature and these channels die at a high temperature. 6\textsuperscript{th} channel in 27\textsuperscript{th} chip has a low leakage current at room temperature and this channel remains within the gain window at room temperature but at high temperature the leakage current increases to \sim 10 \text{nA} and the channel gain drops.

From Fig. 4.23 it can be concluded that if the leakage current (both at room and high temperatures) is below 5 \text{nA} then the channel gain is not affected and there is an excellent correlation between the channel leakage current and channel gain. Thus, this production batch of SCL was rejected and it was suggested to UTAC to test the next batch of MANAS chips at high temperature as the leakage currents were found appreciable at high temperatures (\sim 50\textdegree C) and in this way the bad chips were easily identified.

4.2.2 Testing of pre-production batch

The MANAS devices from U5284382.1 batch were tested in July, 2005 at ATB, UTAC at high temperature (50\textdegree C). This batch was a batch from the older FAB (batch from 2004 FAB). The chips of this batch were tested because of the following reasons:

- wafers for this batch were selected carefully to have low particle count, unlike those supplied in May, 2005;
- datalog file helped us choose the gain and pedestal windows at 50\textdegree C;
- to ascertain that all the bad chips from the lot could be removed by testing at 50\textdegree C;
- analysis of the datalog file were carried out to find whether we had gain-failures with zero gain at 50\textdegree C. This led to identify the chips with leakage currents.

The datalog file of all the 2174 chips from U5284382.1 batch tested on ATB, UTAC was available. Out of these 2174 chips, 1477 chips qualified in both the gain & pedestal windows. A total of 67 chips were outside the gain window and 608 chips were outside the pedestal window. In the second week of August, 2005, 1000 tested
devices were delivered to SINP from UTAC.

The gain and pedestal distributions of 1477 MANAS chips passed by ATB is shown in Fig. 4.24. These histograms are plotted by analyzing the datalog files of UTAC.

**Fig. 4.24.** Gain distribution (left) and pedestal distribution (right) of 1477 chips from the datalog file of UTAC.

From these figures the following conclusions may be drawn:

- both pedestal and gain windows are respected by UTAC tests;

- pedestal distribution peaks slightly to the right, i.e., instead of having a mean of 140 mV, the distribution has a mean of 148 mV;

- mean gain is 3.9 mV/fC, shifted slightly down (before 4.05 mV/fC at room temp). This effect was also observed on SINP test bench with chips delivered in May, 2005;

- gain dispersion at 200 fC is 3.6 %, which is unexpectedly high for a single batch although the window used is quite broad. It was known from our previous experience that the gain dispersion slightly deteriorates at high temp., but this should not have induced such a large gain dispersion.
In order to ascertain that high temperature tests at ATB, UTAC were good, 50 chips were tested at 50° C. The main concern was to check that none of the chips fail at SINP test bench, otherwise we would conclude that the soaking-time (time for which the chips are kept at 50° C before testing) at UTAC was not enough.

Data at SINP was taken under the same conditions as at ATB. The devices were kept at 50° C for almost 4 hours before starting the measurements at 50° C. The measurements at SINP were done through signal input with sixteen 2.2 pF capacitors and with 100 mV input signal. So, the SINP data was collected for 220 fC input. The gain and pedestal distributions are displayed in Fig. 4.25.

The most important conclusion which can be drawn from Fig. 4.25 is that none of these chips had even one channel with abnormally low gain. Thus, the high temperature tests at UTAC were acceptable. The mean gain was found to match reasonably well with those of the ATB. However, the gain dispersion without capacitor calibration was found to be 3.1 %, Fig. 4.25 (left), which was already less than what was found at ATB. In the pedestal distribution we observed only 2 channels marginally outside the pedestal window. However, it should be noted that the noise level at SINP test bench was around 3 mV. The mean pedestal observed at SINP matched quite well with those measured at ATB, UTAC.
We measured the channel-wise average gain of these 50 chips at 50° C and observed large fluctuations because of the capacitance values for which the data was not corrected. Similar measurement was done at the room temperature (∼ 27° C) as the capacitance values were not expected to change for a temp rise of 23 degrees. The relative capacitance values were measured by inserting all 16 of them in a given signal input for 220 fC and by taking the ratio of the measured outputs. The measurement was repeated for every capacitor by removing and placing it in the slot at least for 5 times. This was cross-checked by plotting the channel-wise mean gain at room temperature. This led to believe that the capacitor calibration remained the same for both the room and high temperatures. The channel-wise average gain for 16 channels for 50 chips measured at 50° C and 27° C are exhibited in Fig. 4.26.

Fig. 4.26. Channel-wise average gain for 16 channels for 50 chips at 50° C (left) and 27° C (right).

Channel-wise mean gain at 50° C after the capacitor calibration is shown in Fig. 4.27 (left). We notice a marked improvement and the values could be corrected within 1.2 %. This order of correction is quite appropriate as the expected gain dispersion is around 2.5 %.

In order to test our capacitor calibration, data were taken for 20 chips at room temperature with calibration input. This means that this data utilized the internal capacitors of MANAS chips. However, it should be noted that data for the first three
channels with our test board could not be utilized on using the CALIB-IN due to stray capacitors. But the channel-wise average gains for the remaining 13 channels were investigated. Fig. 4.27 (right) shows this plot and we find that our capacitor calibration is not up to the level of the accuracy of the internal capacitors. Thus, it is expected that the observed gain distribution would be better with CAL-IN. This observation leads to believe that the capacitor calibration of the external capacitors do not induce any over compensation leading to a fictitious narrow gain spread.

The gain distribution of 50 chips at 50° C after the capacitor calibration is shown in Fig. 4.28. It is observed that the gain dispersion improves to 2.6 % at 50° C.

![Fig. 4.27. Channel-wise average gain after the capacitor calibration at 50° C (left). The channel-wise average gain with CAL-IN at 27° C (right).](image)

![Fig. 4.28. Gain distribution of 50 chips at 50° C after the capacitor calibration.](image)
It was decided to test 500 chips at room temperature after the observation that these chips worked very well at 50°C. In May, 2005 batch of the chips, it was found that 50% of the chips were outside the gain window even at room temperature, which was attributed to leakage at ESD protection circuit. These 500 chips were chosen randomly but due to handling problem 3 chips got damaged because some pins bent. All these chips were marked and the datalog file (collected at SINP) were saved. Fig. 4.29 shows the gain and pedestal distributions of the remaining 497 MANAS chips.

![Gain and pedestal distributions of 497 MANAS chips.](image)

**Fig. 4.29.** Gain distribution (left) and pedestal distribution (right) of 497 MANAS chips at room temperature tested at SINP.

A few pedestal channels were found to be outside the window of 60 to 220 mV. The gain of all the 497 chips were found to be within a narrow range of 3.65 to 4.35 and RMS/MEAN = 2.4 %. These chips were chosen with a large gain window of 3.4 to 4.6! Thus, this generally showed that MANAS gain spread had really gone down to 2.5 %.

Hence, result of the testing of the pre-production batch devices can be stated as:

- test at 50°C was done properly at UTAC and this allowed to identify the bad chips from the lot and accept only the good ones;
- scheme of testing the devices at 50°C at SINP worked very well;
Chapter 4

- measurement of 497 devices (from the validated lot from ATB) at SINP test bench through signal input showed good pedestal and gain windows for all the devices;

- analysis of the datalog file for this lot showed that 1.7% devices have abnormally low gain at 50°C. These were the bad chips in this lot;

- we rejected this lot as 1.7% of the devices exhibited the effect of leakage current at 50°C.

4.2.3 Testing of production batch

The devices of U5284384.1 batch (43rd week batch of 2004 of the SCL) were tested at UTAC and it was found that none of the devices showed low gain at 50°C. This indicates that leakage current effect is absent in this batch of chips. Fig. 4.30 shows gain and pedestal distributions of 589 MANAS devices passed by ATB, UTAC within the usual pedestal window of 60 to 200 mV and a gain window of 3.4 to 4.6 mV/fC. This was the largest datalog file of this batch.

![Pedestal distribution (left) and gain distribution (right) of 589 MANAS devices at 50°C from datalog file of UTAC.](image)

Fig. 4.30. Pedestal distribution (left) and gain distribution (right) of 589 MANAS devices at 50°C from datalog file of UTAC.

Following conclusions can be drawn from the figure:

- pedestal and gain windows had been respected by UTAC;
• peak of the pedestal distribution was slightly to the left side of the mean value (140 mV) and has a mean value of 135 mV;

• mean gain is 3.67 mV/fC, which is consistent with the designed value of 3.5 mV/fC;

• gain dispersion at 200 fC is quite large, around 3.3%.

Following tests were performed on the SINP test bench on the devices of U5284384.1 batch:

• pedestal and gain distributions of 50 randomly selected chips at 50° C under the same conditions as the Automatic Test Bench;

• all the 775 chips, received from this batch, were tested at room temperature with $I_{biasRDS} = 39 \, \mu A$ and VROFF = 0.66 V;

• linearity plot for the same 50 chips at room temperature with $I_{biasRDS} = 39 \, \mu A$ and VROFF = 0.66 V. The data were taken at 100, 200 and 300 fC because most of the pad charges were found below 300 fC in the test-beam results. The gain distribution was also extracted at 300 fC.

We tested 50 chips at 50° C in order to ascertain whether the high temperature tests at ATB, UTAC was right. Data was taken under the same conditions as at ATB except that $V_{outOFF}$ was kept equal to 85 mV instead of 100 mV. This discrepancy was realized after the data was taken and was confirmed by measuring $V_{outOFF}$ on the test board. All the measurements were not repeated as this error led to only a DC shift for all the values and did not affect other measurements. However, we had used the input voltage of 90.9 mV, so the input charge was 200 fC with 2.2 pF capacitor.

Fig. 4.31 shows the pedestal and gain distributions of the 50 devices tested at 50° C at SINP. The pedestal window was 45 to 205 mV with $V_{outOFF} = 85$ mV. We had observed only 3 channels out of 800 marginally outside (by 3 mV) the pedestal window. There was no gain failure at 50° C and the mean gain was comparable with
those of the ATB. The gain dispersion without capacitor calibration was found to be 2.9%.

Fig. 4.31. Pedestal distribution (left) and gain distribution without capacitor calibration (right) of 50 MANAS chips at 50$^0$ C tested at SINP.

Gain distribution of 50 chips at 50$^0$ C after capacitor calibration is displayed in Fig. 4.32. It is found that gain dispersion improved to 2.2% at 50$^0$ C. Thus, this batch showed significant improvement in gain dispersion as compared to that observed in the previous batch, where it was 2.6% (Fig. 4.28).

Fig. 4.32. Gain distribution of 50 MANAS devices at 50$^0$ C after capacitor calibration.
The good gain and pedestal values obtained for the 50 chips at high temperature led to the testing of all the 775 devices from this batch at room temperature.

Fig 4.33 (left) shows the gain distribution without capacitor calibration at room temperature. A gain dispersion of 2.7% is observed.

Fig 4.33 (right) shows the true gain distribution of this batch of MANAS, i.e., with capacitor calibration. This lot gave RMS/Mean = 1.9%. This is an extremely satisfactory result obtained at the SINP test board.

**Fig. 4.33.** Gain distribution without capacitor calibration (left), gain distribution after capacitor calibration (right) of 775 MANAS devices at room temperature tested at SINP.

Before declaring this batch to be valid, a representative study of linearity of these devices was carried out. The gain data was taken at 100, 200 and 300 fC for 50 devices and the calibration data was fitted with a second order polynomial. It is to be noted that a quadratic term is the measure of the nonlinearity.

The gain linearity of all the 16 channels of a single chip is exhibited in Fig. 4.34. The quadratic term is found to be very small (\(\sim 10^{-4}\)), thus indicating that nonlinearity up to 300 fC is negligible.

**Fig. 4.35 (left).** Shows the delay plot for all 16 channels of a MANAS from two different lots, namely, S0440 and S0443. It is concluded that the gains in all the channels remain linear for a delay between I/P and T/H ranging between 1.2 and 1.3 \(\mu\)sec.
Fig. 4.35 (right) shows the gain dispersion at 300 fC. The conclusion made from this figure is that the 50 chips from this batch showed a gain spread of 2.7% at 300 fC. This is also within an acceptable limit.

Fig. 4.34. Left: Gain linearity up to 300 fC for 16 channels of a MANAS chip. Right: Linear and quadratic coefficients with respect to biasing voltages.

Fig. 4.35. Left: Delay plot for all 16 channels of a single MANAS device from two different lots. Right: Gain distribution of 50 devices at 300 fC at room temperature.

Some of these devices were tested on MANU cards. A gain spread around 2.25% was found.
The various tests of the devices from U5284384.1 batch led to the following conclusions:

- gain spread at the room temp. is 1.9 % for the 775 chips, whereas at 50°C the gain spread is 2.2 %;
- none of the devices were found to be outside the narrow gain window both at room temperature and at 50°C. This indicates that the leakage current problem is absent in this batch of chips;
- linearity upto 300 fC is within a reasonable limit and the gain spread at 300 fC is 2.7 %.

4.2.4 Testing of the first production batch

The devices from first production batch were tested at ATB, UTAC at 50°C in the following three gain windows:

3.35 - 3.95 with mean gain around 3.65 mV/fC
3.25 - 3.85 with mean gain around 3.55 mV/fC
3.15 - 3.75 with mean gain around 3.45 mV/fC

Results of the analysis of datalog files are displayed in Figs. 4.36 and 4.37.

![Fig. 4.36. Left: Gain distribution of devices in gain window 3.35 - 3.95 mV/fC. Right: Gain distribution of devices in gain window 3.25 - 3.85 mV/fC.](image)
These devices are also having different mean values of gain for different production lots and there is a slight tale on the left side of the distribution as evident from Fig. 4.38.

**Fig. 4.37.** Gain distribution of devices in gain window 3.15 - 3.75 mV/fC.

**Fig. 4.38.** Gain distribution of the devices, analysed from UTAC datalog file, showing different mean values for different lots.

With such a consideration, all the devices of the first production batch were tested at SINP in January, 2006. They were tested in three different gain windows and ensured a gain spread (RMS/Mean) of the order of or less than 2.5 %. The chosen gain windows over a gain range from 3.3 to 3.9 mV/fC are:
Testing of the chips from various lots of the first production batch led to conclude that the devices were in the acceptable windows of gain and pedestal and provided a gain spread of 2.5%. Hence, the devices from this batch were delivered to the ALICE Collaboration; delivery status is discussed in Section 4.2.4.

4.3 MANAS delivery

A total of 88,000 and 20,000 MANAS devices were respectively delivered to ALICE-MUON and ALICE-PMD Collaborations. The only devices with gain spread, RMS/Mean \( \leq 2.5 \% \), were delivered to ALICE-MUON Collaboration. The ALICE-PMD Collaboration was not constrained to such gain spread. The devices mainly with lower mean gain values were delivered to the ALICE-PMD Collaboration.

The delivery of all the devices in a single gain window with a fixed gain spread was not practically possible. So, it was decided to deliver the devices in various gain windows. As mentioned in Section 4.2.4, three gain windows with mean gain values: \( \sim 3.7, 3.6 \) and \( 3.5 \) mV/fC were chosen to test and deliver the devices but during testing a large number of devices with mean gain values around 3.3 and 3.85 mV/fC were found. It was, therefore, decided to test and deliver those devices in the following five gain windows:

- **Bin 0**: 3.60 to 4.10 with mean gain \( \sim 3.85 \) mV/fC
- **Bin 1**: 3.45 to 3.95 with mean gain \( \sim 3.70 \) mV/fC
- **Bin 2**: 3.35 to 3.85 with mean gain \( \sim 3.60 \) mV/fC
- **Bin 3**: 3.25 to 3.75 with mean gain \( \sim 3.50 \) mV/fC
- **Bin 4**: 3.05 to 3.55 with mean gain \( \sim 3.30 \) mV/fC

Delivery of MANAS devices started in August, 2005 and got over by January, 2007. The total number of devices delivered in each Bin is mentioned in Table 4.6. A complete delivery status of MANAS devices is displayed [6] in Fig. 4.39. The delivery
Table 4.6 Number of MANAS devices delivered to ALICE MUON Collaboration.

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Grand Total = 88000

**MANAS Delivery Status**

(Delivered to MUON Collaboration)

(Delivered to PMD Collaboration)

Fig. 4.39. Delivery status of MANAS devices.
of MANAS chips to ALICE-PMD Collaboration is also given in the same figure.

Gain distributions of the devices delivered in various bins are shown in Figs. 4.40 - 4.44:

Fig. 4.40. Gain distribution of 1000 MANAS devices delivered in Bin 0.

Fig. 4.41. Gain distribution of 4000 MANAS devices delivered in Bin 1.
Fig. 4.42. Gain distribution of 4000 MANAS devices delivered in Bin 2.

Fig. 4.43. Gain distribution of 4000 MANAS devices delivered in Bin 3.
Fig. 4.44. Gain distribution of 4000 MANAS devices delivered in Bin 4.
References:


