CHAPTER 8

DESIGN OF HIGH PERFORMANCE VOLTAGE CONTROLLED OSCILLATOR (VCO) USING 45 NM VLSI TECHNOLOGY

A key circuit use in modern communication is voltage control oscillator (VCO). VCO’s output is an AC waveform whose frequency is dependent upon the input voltages. In today’s wireless communication system, greater maximum frequency required by the VCO with respect to the digital phones that use this circuit, low power consumption, small size & low fabrication cost are important design factor. The layout of VCO which is develop by us is a modified design of high performance VCO. This is a optimum design for use in industries at 45 nm VLSI technology. In the estimated design more emphases is given on power consumption, layout design and many more. This report is a brief study of high performance VCO on 45 nm VLSI technology to achieve some objectives as mention above.

The role of oscillators is to create a periodic logic or analog signal with a stable and predictable frequency. Oscillators are required to generate the carrying signals for radio frequency transmission, but also for the main clocks of processors. The high performance VCO provides very good linearity as compared to previous one.

The main problem of this type of oscillators is the very strong dependence of the output frequency on virtually all process parameters and operating conditions. As an example, the power supply voltage VDD has a very significant importance on the oscillating frequency.
The oscillation frequency of the ring oscillator is neither stable, nor controllable, and even not precisely predictable, as it is based on the switching characteristics of logic gates which may fluctuate +/-20%.

In Microwind, the threshold and mobility parameters are varying with a Normal distribution <Gloss>, with a typical variation of 10%. The normal distribution of the threshold voltage $V_t$ corresponds to a density of probability following the equation.

$$f_{Vt} = \frac{1}{\sqrt{2\pi}\sigma} e^{\frac{(Vt-Vt_0)^2}{2\sigma^2}}$$

Where

$f$ is the density of probability $= 0.1$(Equivalent to 10% typical fluctuation of the parameter)

$Vt_0 = \text{typical threshold voltage (0.4V)}$

$Vt = \text{threshold value (V)}$

The aspect of $f$ versus $Vt$ is given in fig 8.1

The high performance VCO shown in fig 8.2, provides very good linearity. The principle of this VCO is a delay cell with linear delay dependence on the control voltage. The delay cell consists of a p-channel MOS in series, controlled by $V_{\text{control}}$, and a pull-down n-channel MOS, controlled by $V_{\text{plage}}$. The delay dependence on $V_{\text{control}}$ is almost linear for the fall edge. The key point is to design an inverter just after the delay-cell with a very low commutation point $Vc$. The rise edge is almost
unchanged.

\[ f_{v_t} \]

High probability of obtain 0.4 V

Low probability to be higher than obtain 0.5V

Very low probability to be higher than obtain 0.6V

Fig 8.1 The normal distribution of Vt, with a typical variation of 10%

The delay cells are connected, to delay both rise and fall edge of the oscillator as shown in following fig 8.2.
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Fig 8.2 High performance VCO

The layout of the above VCO using 45 nm VLSI technology is shown in fig 8.3 below.
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Fig 8.3 The layout of the high performance VCO using 45 nm VLSI technology
Fig 8.4 The voltage verses time response of high performance VCO using 45 nm VLSI technology
Fig 8.5 The voltage, current verses time response of high performance VCO using 45 nm VLSI technology
Fig 8.6 The Frequency verses time response of high performance VCO using 45 nm VLSI technology
Table 8.1 Voltage variation of VDD versus frequency of node Vosillator

Fig 8.7 Voltage variation of VDD versus frequency of node Vosillator
The supply used Vdd is a DC supply of 1V. The technology used in 45 nm technology, Vcontrol is a clock of 0.5 V as a level 1 and 0.0V as level 0 with time low \( t_l = 0.450 \text{ ns} \), Rise time \( (t_r) = 10.000 \text{ ns} \), high time \( t_h = 0.45 \text{ ns} \) and fall time \( (t_f) = 10.00\text{ns} \).

Vplage is DC supply having DC voltage level equal to 0.667V. N1, N2, N5 NMOS transistor are having width \( W = 0.240 \mu \text{m} \) and length \( L = 0.040\mu\text{m} \).

N3, N7 n mos width = 0.080\mu m and length \( L = 0.200\mu\text{m} \). Other NMOS N4 and N6 are having dimensions as \( W = 1.44 \mu \text{m} \) & \( L = 0.040\mu \text{m} \).

The PMOS transistors are having dimensions as follows:

- P1, P4, P5 \( W = 0.640 \mu \text{m} \) & \( L = 0.040 \mu \text{m} \)
- P2, P6 \( W = 0.240 \mu \text{m} \) & \( L = 0.040 \mu \text{m} \)
- P3, P7 \( W = 0.320 \mu \text{m} \) & \( L = 0.040 \mu \text{m} \).

Fig 8.4 shows the voltage response with respect to time. Fig 8.5 shows voltage and currents response with respect to time. Fig 8.6 shows frequency verses time response of high performance VCO. At a time 30 nanosecond for controlled voltage \( V_c = 0.42 \text{ volt} \) frequency is found as 2.44 Giga Hz. It is also proved that Frequency of

<table>
<thead>
<tr>
<th>Sr. No.</th>
<th>Vdd (volt)</th>
<th>Frequency(GHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0.800</td>
<td>4.000</td>
</tr>
<tr>
<td>2</td>
<td>1.00</td>
<td>4.000</td>
</tr>
<tr>
<td>3</td>
<td>1.20</td>
<td>3.766</td>
</tr>
<tr>
<td>4</td>
<td>1.40</td>
<td>3.054</td>
</tr>
</tbody>
</table>
oscillation of this VCO is inversely proportional to control voltage.

The total power consumption is \( P = 45.749 \mu\text{w} \).

The dependence of voltage of node \( V_{DD} \) on frequency of node V-oscillator is observed by taking variations of VDD from 0.8 V to 1.6 V in step of 0.20V as shown in fig 8.7.

It is concluded that high performance voltage controlled oscillator gives more linear response than the previous one. It is also found that for change in supply voltage 0.8 to 1.00v freq of oscillator is nearly constant.

Following program shows the spice netlist of this VCO. This netlist shows complete component list along with parameter specifications.

\[
\text{n+CGBO} = 60.0p \\
* \\
* \text{p-MOS BSIM4:} \\
* \text{low leakage} \\
\.MODEL P1 PMOS LEVEL=14 VTHO=-0.15 U0=0.018 TOXE=3.5E-9 LINT=0.000U \\
+K1 =0.650 K2=0.100 DVT0=2.300 \\
+DVT1=0.540 LPE0CIRCUIT C:\Program Files\MICROWIND3.1\Client\Ph.d work 30-4-10high performance \\
vco45.MSK \\
* \\
* \text{IC Technology: CMOS 45nm - HighK/Metal/Strain - 8 Metal copper} \\
* \\
\text{VDD 1 0 DC 1.00} \\
\text{VVcontrol 11 0 DC 0 PULSE(0.00 0.50 0.45N 10.00N 10.00N 0.45N 20.90N)} \\
\text{V12_Vplage 12 0 DC 0.67V} \\
* \\
\]

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* List of nodes
* “V-oscillator” corresponds to n°3
* “s1” corresponds to n°4
* “N6” corresponds to n°6
* “N7” corresponds to n°7
* “N8” corresponds to n°8
* “N9” corresponds to n°9
* “Vcontrol” corresponds to n°11
* “Vplane” corresponds to n°12

* MOS devices

MN1 0 9 8 0 N1 W= 0.24U L= 0.04U
MN2 0 8 7 0 N1 W= 0.24U L= 0.04U
MN3 6 12 0 0 N1 W= 0.08U L= 0.20U
MN4 4 6 0 0 N1 W= 1.44U L= 0.04U
MN5 0 4 3 0 N1 W= 0.24U L= 0.04U
MN6 0 10 9 0 N1 W= 1.44U L= 0.04U
MN7 10 12 0 0 N1 W= 0.08U L= 0.20U
MP1 1 4 3 1 P1 W= 0.64U L= 0.04U
MP2 1 6 4 1 P1 W= 0.24U L= 0.04U
MP3 7 11 6 1 P1 W= 0.32U L= 0.04U
MP4 1 8 7 1 P1 W= 0.64U L= 0.04U
MP5 1 9 8 1 P1 W= 0.64U L= 0.04U
MP6 1 10 9 1 P1 W= 0.24U L= 0.04U
MP7 3 11 10 1 P1 W= 0.32U L= 0.04U

* C2 1 0  6.481fF
C3 3 0  0.687fF
C4 4 0  0.621fF
C6 6 0  0.335fF
C7 7 0  0.404fF
C8 8 0  0.326fF
C9 9 0  0.621fF
C10 10 0 0.335fF
C11 11 0 0.308fF
C12 12 0 0.292fF

* Transient analysis

* (Pspice)

.PROBE

.END