Annexure – B

PIN MAPPING FOR FPGA

#PACE: Start of Constraints generated by PACE

#PACE: Start of PACE I/O Pin Assignments

NET "ADC_Addrs_in<0>" LOC = "p29" | IOSTANDARD = LVTTL ;
NET "ADC_Addrs_in<1>" LOC = "p27" | IOSTANDARD = LVTTL ;
NET "ADC_Addrs_in<2>" LOC = "p21" | IOSTANDARD = LVTTL ;
NET "ADC_Clk_in" LOC = "p79" | IOSTANDARD = LVTTL ;
NET "ADC_data_in<0>" LOC = "p196" | IOSTANDARD = LVTTL ;
NET "ADC_data_in<1>" LOC = "p197" | IOSTANDARD = LVTTL ;
NET "ADC_data_in<2>" LOC = "p191" | IOSTANDARD = LVTTL ;
NET "ADC_data_in<3>" LOC = "p194" | IOSTANDARD = LVTTL ;
NET "ADC_data_in<4>" LOC = "p189" | IOSTANDARD = LVTTL ;
NET "ADC_data_in<5>" LOC = "p190" | IOSTANDARD = LVTTL ;
NET "ADC_data_in<6>" LOC = "p185" | IOSTANDARD = LVTTL ;
NET "ADC_data_in<7>" LOC = "p187" | IOSTANDARD = LVTTL ;
NET "Address_out<0>" LOC = "p171" | IOSTANDARD = LVTTL ;
NET "Address_out<1>" LOC = "p172" | IOSTANDARD = LVTTL ;
NET "Address_out<2>" LOC = "p168" | IOSTANDARD = LVTTL ;
NET "Capture_ctrl_in" LOC = "p165" | IOSTANDARD = LVTTL ;
NET "LED_out" LOC = "p132" | IOSTANDARD = LVTTL ;
NET "OE1_Disp" LOC = "p2" | IOSTANDARD = LVTTL ;
NET "OE2_Disp" LOC = "p3" | IOSTANDARD = LVTTL ;
NET "OE3_Disp" LOC = "p7" | IOSTANDARD = LVTTL ;
NET "OE4_Disp" LOC = "p9" | IOSTANDARD = LVTTL ;
NET "OE_out" LOC = "p198" | IOSTANDARD = LVTTL ;
NET "PID_Data_out<0>" LOC = "p183" | IOSTANDARD = LVTTL ;
NET "PID_Data_out<1>" LOC = "p184" | IOSTANDARD = LVTTL ;
NET "PID_Data_out<2>" LOC = "p181" | IOSTANDARD = LVTTL ;
NET "PID_Data_out<3>" LOC = "p182" | IOSTANDARD = LVTTL ;
NET "PID_Data_out<4>" LOC = "p178" | IOSTANDARD = LVTTL ;
NET "PID_Data_out<5>" LOC = "p180" | IOSTANDARD = LVTTL ;
NET "PID_Data_out<6>" LOC = "p175" | IOSTANDARD = LVTTL ;
NET "PID_Data_out<7>" LOC = "p176" | IOSTANDARD = LVTTL ;
NET "Reset_in" LOC = "p165" | IOSTANDARD = LVTTL ;
PIN MAPPING FOR FPGA (cont...)

NET "Seven_seg_out<0>" LOC = "p10" | IOSTANDARD = LVTTL ;
NET "Seven_seg_out<1>" LOC = "p11" | IOSTANDARD = LVTTL ;
NET "Seven_seg_out<2>" LOC = "p12" | IOSTANDARD = LVTTL ;
NET "Seven_seg_out<3>" LOC = "p13" | IOSTANDARD = LVTTL ;
NET "Seven_seg_out<4>" LOC = "p15" | IOSTANDARD = LVTTL ;
NET "Seven_seg_out<5>" LOC = "p16" | IOSTANDARD = LVTTL ;
NET "Seven_seg_out<6>" LOC = "p18" | IOSTANDARD = LVTTL ;
NET "Seven_seg_out<7>" LOC = "p19" | IOSTANDARD = LVTTL ;

NET "SOC_out" LOC = "p199" | IOSTANDARD = LVTTL ;

NET "Speed_select_in<0>" LOC = "p133" | IOSTANDARD = LVTTL ;
NET "Speed_select_in<1>" LOC = "p131" | IOSTANDARD = LVTTL ;
NET "Speed_select_in<2>" LOC = "p125" | IOSTANDARD = LVTTL ;

#PACE: Start of PACE Area Constraints

#PACE: Start of PACE Prohibit Constraints

#PACE: End of Constraints generated by PACE