CHAPTER 4
ELECTRONICALLY TUNABLE INTEGRABLE
CCCII-BASED ASP CIRCUITS

4.1 Introduction

As already studied in the previous Chapter, current conveyor (CCII) based realizations have gained significant popularity in analog signal processing applications as they provide simple and attractive CCII–RC circuits for voltage mode and current mode operations. These circuits also exhibit reliable high frequency performance. However, the requirement of precise R and C components and the non availability of electronic tunability make their implementation unsuitable in the complementary monolithic technologies. To overcome this problem, Current Controlled Conveyor (CCCII), implemented using the mixed translinear loop, has been introduced [19]. The intrinsic resistance, $R_x = \frac{V_T}{2I_o}$, in Bipolar [19] and $R_x = \frac{14.96}{\sqrt{I_o}}$ in MOS/CMOS [75] of the CCCII is used to minimize the conversion error and provide tunability and parameter adjustability through bias control current ($I_o$) [18-22]. Also, the non-ideality ($R_x$) of the device can be utilized to advantage in the design by eliminating/reducing the requirement of physical R’s, and in many cases, making the realization completely active-C. Such circuits may be fabricated in monolithic CMOS form with electronic tunability.

This Chapter presents some novel analog signal processing circuits based on current controlled conveyor. In Sec. 4.2, the realization of a novel electronically tunable temperature insensitive current mode analog multiplier/divider circuit is given, which uses only active devices. The proposed all active circuit employs only two CCCIIs without requiring matching constraints. Section 4.3 is devoted to the realization of novel CCCII-

* Authors’ paper [P5] [P6] [P7] are based on the material presented in this chapter
based ideal grounded inductance simulator (GIS). The proposed GIS uses two CCCIIIs, alongwith, a grounded capacitor and also without matching constraints. This makes it attractive for IC implementation. Section 4.4 presents a new circuit realization of component multiplier employing CCII and CCCII. It is then extended to realize low component CCCII-based ideal grounded R-multiplier. The proposed circuits provide convenient tuning of the R and C values with the bias control current \( I_o \). In Sec. 4.5, the realized inductance simulator of Sec. 4.3 is used in the realization of an MBF, without the requirement of component matching. In the next Section, a novel canonical VM universal translinear-C biquadratic filter (UBF) is given. The realized filter gives all standard biquadratic responses through appropriate selection of inputs. In an IC version, this may be done through a simple electronic switching arrangement. Section 4.7 gives the realization and study of electronically tunable higher order current mode Butterworth low pass ladder filter, based on inductance simulation approach. PSpice simulation results are included in support of the theory. Finally, conclusion is given in Section 4.8.

### 4.2 Temperature Insensitive CM Analog Multiplier/Divider

Analog multipliers and dividers are important nonlinear building blocks and are widely used in control, instrumentation, signal processing and telecommunication systems. As discussed earlier the CM circuits have been receiving growing interest due to their well known advantages. In the literature [82-88], different methods and techniques have been used for the realization of analog multiplier/divider circuits. Realization of analog multiplier/divider, implemented through CMOS structures is used in Refs [83, 84]. Another technique for designing such circuits is based on the use of various active devices [82, 85, 86, 87, 88]. In [82, 87], VM CCII-based and CFA-based analog multipliers/dividers are realized using large number of active and passive elements. In Ref [86], OTA-based circuit is given, which suffers from
limited output voltage swing. The CCCII-based circuits are given in [85, 88]. Ref [85] gives the realization of multiplier/divider circuit. It requires four inputs for the two quadrant multiplier along with a matching condition. In [88], only an analog multiplier realization is given, which employ a single CCCII and passive resistor in its realization.

It may be seen that although a wide variety of multipliers/dividers exist, they suffer from specific drawbacks and scope is present for finding more attractive circuits. An all-CCCII multiplier/divider is considered in this Section.

### 4.2.1 Circuit description

The circuit of a novel temperature insensitive current mode analog multiplier/divider is shown in Fig. 4.1. It consists of only two CCCII's and does not require any passive components in its realization. For the CCCII+, the \( v-i \) relations are defined by:

\[
i_y = 0, \quad v_x = v_y + i_x R_x, \quad i_z = \pm i_x
\]  

where \( R_x (-14.96/\sqrt{I_o}) \), is the intrinsic resistance for CMOS implementation of CCCII of Ref [75]. Routine analysis of the circuit yields the output current:

\[
I_{out} = \pm \frac{I_m I_{o2}}{I_{o1}} = \pm K_I m
\]  

For the multiplier, its multiplication factor \( (K_m) \) is given by:

\[
K_m = \frac{I_{o2}}{I_{o1}}
\]  

For the divider, the division factor \( (K_d) \) is given as:

\[
K_d = \frac{I_{o1}}{I_{o2}}
\]
It may be noted that the non-inverting analog multiplier/divider circuit is realized, if the input of first CCCII is connected to negative output terminal ($Z_1^-$), as shown in Fig. 4.1. The inverting analog multiplier/divider can also be obtained, by connecting the input of first CCCII to positive output terminal ($Z_1^+$).

It is evident from eqns. (4.2), (4.3) and (4.4) that the circuit can perform multiplication of $I_m$ by varying $K_m$ with $I_n$, while keeping the current $I_n$ constant. Also, it realizes divider by varying $K_d$ with $I_n$, keeping the current $I_n$ constant. The important feature of this circuit is that it is an all-CCCII realization, without using passive components. It is also to be noted that since $K$ is in the form of bias current ratio, the thermal voltages of the CCCIIIs get cancelled and the output current becomes insensitive to temperature variations.

4.2.2 Non-ideal analysis

Here we consider the frequency effects and parasitic effects of analog multiplier/divider circuit.

(a) Frequency effect

Taking the frequency dependent $\alpha(s)$ and $\beta(s)$ into consideration, as discussed in Sect. 2.3.2, the analysis of the circuit of Fig. 4.1 yields
It is clear from eqn. (4.5), the output current has two extra poles and two zeros due to single pole roll off model of the CCCII. It is evident, that in integrated CCCIIIs, inherently matched device characteristics are obtained, i.e., \( \omega_{a1} = \omega_{a2} \), \( \omega_{p1} = \omega_{p2} \), and also \( \alpha_1 = \alpha_2 \), \( \beta_1 = \beta_2 \). Hence, pole/zero cancellation take place and the output current has negligible affect of the non-idealities at higher frequencies.

(b) Parasitics effects

Taking the non-idealities, due to parasitics and frequency independent current ratio and voltage ratio of the CCCII into consideration, the analysis of the circuit of Fig. 4.1 yields the output current:

\[
I_{out} = \pm \frac{I_m \alpha_2 \beta_2 R_{X1} I_m}{I_\alpha} \alpha_1 \beta_1 R_{X2} + R_{X1} R_{X2} \left( \frac{1}{R_p} + sC_p \right) \quad 4.6(a)
\]

where \( R_p = R_{y1} \parallel R_{y2} \parallel R_{z1} \) and \( C_p = C_{y1} + C_{y2} + C_{z1} \).

It is seen that at very high frequency a single pole (low pass) characteristics is exhibited. However, taking into consideration, the approximate range of the parasitic values involved in eqn. 4.6 (a), at low to medium frequencies (around 10MHz), eqn. 4.6 (a) modifies to:

\[
I_{out} = \pm \frac{\alpha_2 \beta_2 R_{X1} I_m}{\alpha_1 \beta_1 R_{X2}} \quad 4.6(b)
\]

This for either \( \alpha, s \) and \( \beta, s \) reduces to the ideal expression given in eqn. (4.2).

4.2.3 Sensitivity study

The active and passive sensitivities of the output current \( I_{out} \) of Fig.4.1 are evaluated and are summarized below:
All the sensitivities are found to be reasonable and unity in magnitude.

4.2.4 Design and simulation

The performance study of the circuits presented in this Chapter were carried out through PSpice simulation using MO-CCCII [75], in 0.5 μm CMOS process with $V_{DD} = V_{SS} = 1$ volt, as discussed in Sec. 1.5.2.

A. The multiplier:

The inverting and non-inverting multipliers were simulated. Their output current ($I_{out}$) were plotted against the input current ($I_{in}$) swept in the range of ±100 μA keeping $I_{o_1} (= 10 \mu A)$ constant. A family of curves are obtained for the inverting and non-inverting multipliers shown in Figs. 4.2 (a) and 4.2 (b), respectively at various multiplication factor $K_m (= I_{o_2}/I_{o_1})$ of 2 ($= 20 \mu A/10 \mu A$), 4 ($= 40 \mu A/10 \mu A$) and 6 ($= 60 \mu A/10 \mu A$).

$$S_{1,\alpha_2,\beta_2} = 1, \quad S_{\alpha_1,\alpha_1} = 1, \quad S_{\beta_1,\alpha_1,\beta_1} = -1 \quad (4.7)$$
As expected, straight lines of desired slopes are obtained with the common intersection at point P corresponding to $I_{in} = I_{out} = 0 \mu A$. It is evident that as the numerator current $I_{in}$ increases the output current $I_{out}$ also increases. The output current is multiple of input current with the variation of $I_{in}$ at constant $I_{out}$.

In another simulation, the multiplier was tested by multiplying a triangular waveform of peak values of $\pm 100 \mu A$ by a factor of 2 and 4 by keeping the current $I_{in}$ constant at $10 \mu A$. Figs. 4.3 (a) and 4.3 (b), respectively, show inverting and non-inverting responses, i.e., the output current $I_{out}$ is seen as a product of input current multiplied by a factor of 2, and 4, corresponding to the bias control current $I_{in} (= 20 \mu A$, and $40 \mu A$).
Fig 4.3 (a) transient response of inverting multiplier circuit at $I_{o1} = 20 \, \mu A$, $40 \, \mu A$ for $I_{i} = 10 \, \mu A$ and $I_{in} = 100 \, \mu A$ (pk)

Fig 4.3 (b) transient response of non-inverting multiplier circuit at $I_{o1} = 20 \, \mu A$, $40 \, \mu A$ for $I_{i} = 10 \, \mu A$ and $I_{in} = 100 \, \mu A$ (pk)

**B. The divider:**

The DC transfer characteristics for the inverting and non-inverting divider, shown in Fig. 4.4 (a) and 4.4 (b) respectively were plotted. These give
the variation of the output current \( I_{\text{out}} \) against the input sweep current \( (I_m) \) at different dividing factors \( K_d (= I_{o1}/I_{o2}) \) of 0.1 \((10 \mu A/100 \mu A)\) and 0.2 \((20 \mu A/100 \mu A)\) with \( I_{o2} \) held constant at 100 \( \mu A \). The results show linear variation, as expected.

![Fig. 4.4 (a) DC transfer characteristics for inverting divider function](image)

![Fig. 4.4 (b) DC transfer characteristics for non-inverting divider function](image)
For the divider circuit, the divider operation was performed by dividing the triangular waveform at \( I_{V_1} = 100 \mu A \) by a factor of 2, and 4 shown in Figs. 4.5 (a) and 4.5 (b), respectively.

**Fig 4.5 (a) transient response of inverting divider circuit at**  
\[ I_{V_1} = 40 \mu A, 80 \mu A \text{ for constant } I_{V_2} (= 20 \mu A) \text{ and } I_{in} \text{ of (pk) } = 100 \mu A \]

**Fig 4.5 (b) transient response of non inverting divider circuit at**  
\[ I_{V_1} = 40 \mu A, 80 \mu A \text{ for constant } I_{V_2} (= 20 \mu A) \text{ and } I_{in} = 100 \mu A \text{ (pk)} \]
The high frequency performance of multiplier/divider circuit was verified by frequency response of the output current $I_{out}$ at $K_m = 1$ and 2 (by changing $I_{o1}$) and keeping the input current $I_{in} = 100 \ \mu A$ (constant). The frequency response for non-inverting multipliers is plotted in Fig. 4.6.

![Simulated results at $I_{o1} = 10 \ \mu A$](image)

<table>
<thead>
<tr>
<th>$I_{o2}$ ($\mu A$)</th>
<th>$I_{out}$ ($\mu A$)</th>
<th>Frequency</th>
</tr>
</thead>
<tbody>
<tr>
<td>10 $\mu A$</td>
<td>100.02</td>
<td>30.9 MHz</td>
</tr>
<tr>
<td>20 $\mu A$</td>
<td>200.01</td>
<td>29.8 MHz</td>
</tr>
</tbody>
</table>

Fig 4.6 Frequency response of non-inverting multiplier circuit at constant $I_{o1} = 10 \ \mu A$ and $I_{in} = 100 \ \mu A$ for $I_{o2} = 10 \ \mu A, 20 \ \mu A$

It is evident that the output current $I_{out}$ is found to be constant up to the frequency range of 30.9 MHz and 29.8 MHz, corresponding to $I_{out}$ is equal to 100.02 $\mu A$ and 200.01 $\mu A$, respectively. The non-idealities have negligible effects over a wider frequency range. At higher frequencies low pass response is obtained, as discussed in Section 4.2.2.

A simple active only, current mode temperature insensitive electronically tunable analog multipliers / divider circuit has been given and studied. The proposed circuit can perform ideal multiplication and division, without requiring any matching constraints. The performance of the analog multiplier and divider circuit was verified through PSpice simulation with convincing results. The circuit is found to have excellent high frequency performance. It also has the advantages of low component count, low
sensitivity and low supply voltage operation, as compared to available references in the literature [82-88].

### 4.3 Realization of Ideal Grounded Inductance Simulator (GIS)

Inductance simulation based on CCCII, has been a topic of keen interest for analog designers. In reference [21], CCCII-based non-ideal grounded inductance is reported, which is used in the realization of band pass filter from an RLC-prototype through L-replacement scheme. In 2004, Gift [74] proposed a circuit to realize non-ideal simulated inductor using operational conveyors, however it has the disadvantage of large component count and lack of electronic tunability.

#### 4.3.1 Circuit description

Fig. 4.7 shows the circuit of a novel tunable ideal grounded inductance simulator (GIS) [P5] using two current controlled conveyors (CCCIIs) and a grounded capacitor. It is obtained from the scheme of Reference [71]. Using the v-i relations defined by eqn. (4.1) for the CCCII+, routine analysis of the circuit yields input impedance:

\[
Z_{in}(s) = sC/R_x \quad 4.8(a)
\]

\[
Z_{m}(s) \triangleq s Leq \quad 4.8(b)
\]

where \( Leq \) is the equivalent inductance given by:

\[
Leq = CR_{x1} R_{x2} \quad 4.9
\]

For \( R_{x1} = R_{x2} = R_x \),

\[
Leq = CR_x^2 = \frac{(14.96)^2}{I_o} C \quad 4.10
\]

Eqns. (4.9) and (4.10) show that an ideal grounded inductance is realized, which can be tuned through bias control current (\( I_o \)).
4.3.2 *Non-ideal analysis*

Taking into consideration the non-idealities of CCCII mentioned in Sec. 2.3.2, for low to medium frequencies, eqn. (4.1) can be expressed as:

\[ i_y = 0, v_y = \beta v_y + i_x R_x, i_y = \alpha i_x \quad (4.11) \]

Analysis of the GIS using eqn. (4.11) yields the input impedance as:

\[ Z_m(s) = \frac{sCR_x R_{22}}{\alpha_1 \alpha_2 \beta_1 \beta_2} = s L_{eq} \quad (4.12) \]

For \( R_{x_1} = R_{x_2} = R \),

\[ L_{eq} = \frac{CR^3}{\alpha_1 \alpha_2 \beta_1 \beta_2} = C \frac{(14.96)^2}{1_C \alpha_1 \alpha_2 \beta_1 \beta_2} \quad (4.13) \]

where the eqn. (4.13), clearly shows L- enhancement due to frequency independent non-idealities.
4.3.3 Sensitivity study

The passive and active sensitivities of the inductor are evaluated and are found to be reasonably small. These are summarized below:

\[ S_{C,R_n,R_2}^{Leq} = 1, \quad S_{a_1,a_2,a_3,a_4}^{Leq} = -1 \]  \hspace{1cm} (4.14)

From eqn. (4.14) it is clear that all the active and passive sensitivity figures are reasonable being equal to unity in magnitude.

4.3.4 Design and simulation

The performance of the grounded inductance simulator (GIS) was verified through PSpice simulation. The high frequency performance of CCCII-based ideal grounded inductor of Fig.4.7 was verified by designing it for \( I_{o_1}, I_{o_2} = 0.65 \mu A \), corresponding to \( R_{n_1} = R_{x_1} = R_{x_2} = 18.5 \, K\Omega \) and \( C = 12 \, pF \).

The theoretical value of \( L_{eq} \) obtained from eqn. (4.10) is 4.8 mH. The resulting frequency response is shown in Fig.4.8. It gives the simulated value of \( L_{eq} = 4.81 \, mH \), which remains constant over a frequency range of about 2.8 MHz. The value of \( L_{eq} \) depicts a LP characteristic. It may be noted that in Ref [74], the frequency range is only 30 KHz, which show reliable high frequency operation of the proposed circuit.

![Fig.4.8 Frequency response of CCCII-based simulated inductor](image-url)
The proposed inductance simulator is realized using low component circuit with Current Controlled Conveyor (CCCII), alongwith, a single grounded capacitor. The circuit is free from matching constraints and enjoys attractive features of electronic tunability, low active and passive component count, low sensitivity performance, wide frequency range of operation and use of low supply voltage. The use of only CCCII and grounded passive capacitors is attractive for monolithic CMOS implementation.

4.4 Realization of Component Multipliers

Component multipliers find wide applications in the realization of large R- and C-values in ICs, as well as, for convenient wide range tuning of filters and oscillators [78-80]. Multiplier circuits using Operational Transconductance Amplifiers (OTAs) [78-80] enjoy electronic tunability, but suffer from limited output voltage swing and operating range. Second generation Current Conveyors (CCII’s) can provide wider bandwidth and better accuracy than OTA-based circuits, but lack electronic tunability. In this Section, a new circuit configuration of an ideal grounded R and C multipliers is proposed, which consists of a CCII, a CCCII, alongwith, two grounded passive components. This generalized circuit can be used to obtain R and C multipliers which have convenient tuning of multiplication factor with bias control current ($I_0$). It is easily extended to realize low component CCCII-based ideal grounded R-multiplier.

4.4.1 Realization of R/C Multipliers

The proposed generalized circuit for R/C- multiplier [P6], shown in Fig. 4.9, is realized using the basic scheme for grounded immittance simulation [71]. It requires one CCII and a CCCII, alongwith, two grounded passive components. Its analysis gives the driving point impedance function as:
Fig. 4.9 Ideal grounded R/C- component multiplier

**A. R-Multiplier:** If $Z_1 = R_1$ and $Z_2 = R_2$, then an R-multiplier is realized having,

$$Z_1(s) = \frac{Z_1 R_1}{Z_2}$$

(4.15)

or

$$R_{eq} = K R_1$$

(4.17)

where the multiplication factor ($K_1$) is:

$$K_1 = \frac{R_1}{R_2} = \frac{14.96}{\sqrt{I_0} R_2}$$

(4.18)

It is to be noted that the multiplication factor $K_1$ is inversely proportional to $\sqrt{I_0}$. 

108
**B. C-Multiplier:** If \( Z_1 = 1/sC_1 \) and \( Z_2 = R_2 \), then C-multiplier is realized having,

\[
Z_i(s) = \frac{1}{sC_{eq}} = \frac{R_\eta}{sC_1R_2}
\]

(4.19)

where

\[
C_{eq} = \frac{C_1R_2}{R_\eta}
\]

(4.20)

Its multiplication factor is

\[
K_C = \frac{R_2}{R_\eta} = \frac{\sqrt{I_o}R_2}{14.96}
\]

(4.21)

where \( K_C \) is directly proportional to \( \sqrt{I_o} \). It can be seen that ideal grounded R- and C-multipliers are realized having their multiplication factors electronically tunable with bias control current \( I_o \).

**C. CCCII-Based R-Multiplier:** The multiplier circuit of Fig. 4.9 can easily be converted to CCCII-based R-multiplier by replacing CCII and \( Z_1 (= R_1) \) by a CCCII. This eliminates the physical requirement of \( R_1 \). The resulting circuit consists of only two CCCIIs, along with, a grounded resistor, as shown in Fig. 4.10. Its analysis yields:

\[
Z_i(s) = R_{eq} = \frac{R_\eta R_{x_1}}{R}
\]

(4.22)

or

\[
Z_i(s) = \frac{K_r}{R}
\]

(4.23)

where the multiplication factor is

\[
K_r = R_\eta R_{x_1} = \frac{(14.96)^2}{\sqrt{I_o}I_{o_2}}
\]

(4.24)

For \( R_{x_1} = R_{x_2} = R_x \),

\[
K_r = (R_x)^2 = \frac{(14.96)^2}{I_o}
\]

(4.25)
Here the physical resistor $R$ is preselected of convenient value suitable for fabrication in IC technology and the control currents $I_{o_1}$ and $I_{o_2}$ are set to obtain the multiplication factor for realizing the desired $R_{eq}$ value.

### 4.4.2 Non-ideal analysis

Considering the non-idealities of CCCII, analysis of the circuit of Fig.4.9 yields the input impedance as:

$$Z_i(s) = \frac{\alpha_2Z_1R_i}{\alpha_1\beta_1\beta_2Z_2}$$  \hspace{1cm} (4.26)

The modified $R_{eq}$ and $C_{eq}$ are respectively given by:

$$R_{eq} = \frac{\alpha_2R_1R_i}{\alpha_1\beta_1\beta_2R_2}$$  \hspace{1cm} (4.27)
which show R-enhancement and C-reduction.

The non-ideal $R^q$ for CCCII-based R-multiplier is given by:

$$R^q = \frac{R_i^q}{R_2}$$

(4.29)

which depicts R-enhancement.

\subsection*{4.4.3 Sensitivity study}

The active and passive sensitivities of the $R^q$ and $C_{eq}$ of Fig.4.9 are evaluated and are summarized below:

$$S_{R_{1},R_{2}} = 1, \quad S_{R_{1},R_{2}} = -1, \quad S_{C_{max},R_{1},R_{2}} = 1, \quad S_{C_{max},R_{1},R_{2}} = -1,$$

$$S_{C_{max},R_{1},R_{2}} = -1, \quad S_{C_{max},R_{1},R_{2}} = 1, \quad S_{C_{max},R_{1},R_{2}} = -1$$

(4.30)

Similarly, the active and passive sensitivities of the $R^q$ of Fig.4.10 are evaluated and are given as:

$$S_{R_{1},R_{2}} = 1, \quad S_{R} = -1, \quad S_{C_{max},R_{1},R_{2}} = 1, \quad S_{C_{max},R_{1},R_{2}} = -1$$

(4.31)

All the sensitivities are seen to be reasonable and being unity in magnitude.

\subsection*{4.4.4 Design and simulation}

The performance of the basic R/C-multiplier was verified through PSpice simulation using multiple output-CCCII model of [75] and CCII model of [11]. The basic R-multiplier of Fig.4.9 was designed at $R_1 = 10 \, \text{K}\Omega$ and $R_2 = 1 \, \text{K}\Omega$. The multiplication factor $K_r$ of eqn. (4.18) was varied with the control current ($I_\alpha$)
from 0.022 μA to 223.8 μA (R₁: 1 kΩ to 100 kΩ). This gives the variation of R<sub>eq</sub> from 10 kΩ to 1 MΩ. The theoretical and simulated variation of effective resistance with the multiplication factor (K<sub>e</sub>) is shown in Fig. 4.11. This exhibits convenient wide range tunability of effective resistance with the multiplication factor.

![Graph showing variation of effective resistance R<sub>eq</sub> with K<sub>e</sub> (1/√I<sub>c</sub>)](image)

Fig. 4.11 Variation of effective resistance R<sub>eq</sub> with K<sub>e</sub> (1/√I<sub>c</sub>)

Similarly, the C-multiplier of Fig. 4.9 was designed with C₁ = 10 pF and R₂ = 100 kΩ. The multiplication factor (K<sub>c</sub>), given by eqn. (4.21) was varied with the control current (I<sub>c</sub>) from 0.022 μA to 223.8 μA, (R₂: 1 kΩ to 100 kΩ). The theoretical and simulated variation of effective capacitance with K<sub>c</sub> is shown in Fig. 4.12. Linear tunability is exhibited over a wide range.
Next, the CCCII-based R-multiplier of Fig.4.10 was designed with \( R = 1 \) KΩ and \( R_x = 10 \) KΩ by setting \( I_{o_1} = 2.23 \) μA. The multiplication factor (\( K_r \)) given in eqn. (4.24), was varied with the control current \( I_{o_2} \) from 0.022μA to 223.8 μA (\( R_x : 1 \) KΩ to 100 KΩ). This gives the corresponding range of \( R_{eq} \) from 10 KΩ to 1 MΩ. The theoretical and simulated results are shown in Fig.4.13. These again exhibit convenient tunability of effective resistance with its multiplication factor.

The range of \( R_{eq} \) was increased by setting \( R_{x_1} = R_{x_2} = R_x \), corresponding to \( I_{o_1} = I_{o_2} = I_{o} \). The theoretical and simulated variation of effective resistance with multiplication factor \( K_r \) is shown in Fig.4.14.
\( I_{o_1} = 2.23 \mu A \)

Fig. 4.13 Variation of effective resistance \( R_{eq} \) with \( K_r (1/\sqrt{I_{o_1} I_{o_2}}) \)

Fig. 4.14 Variation of effective resistance \( R_{eq} \) with \( K_r (1/I_{o}) \)
To verify the frequency performance of CCCII-based R-multiplier of Fig.4.10, it was designed at $R = 1 \, \text{K} \Omega$ and $I_{\alpha} = 2.23 \, \mu\text{A}$ ($R_{\alpha} = 10 \, \text{K} \Omega$). The value of effective resistance $R_{eq}$ at $I_{\alpha} = 0.139 \, \mu\text{A}$ ($R_{\alpha} = 40 \, \text{K} \Omega$) is found to be $400.05 \, \text{K} \Omega$. It is evident from Fig.4.15 that the effective resistance $R_{eq}$ remains constant up to frequency of $1.5 \, \text{MHz}$, after which it decreases due to non-idealness of CCCII described earlier.

![Variation of effective resistance $R_{eq}$ with frequency](image)

Fig.4.15 Variation of effective resistance $R_{eq}$ with frequency

The proposed ideal grounded R and C-multipliers provide convenient, electronic tunability of their multiplication factors with control current ($I_{\alpha}$). The design of multipliers is free from matching constraints. These circuits enjoy very low sensitivities with respect to the circuit elements. The multipliers are ideally suited for providing large R and C-values in IC-fabrication. Also, they have attractive use in wide range electronically tunable filters and oscillators.
4.5 Realization of Multifunctional Biquadratic Filter Using GIS

In this Section, the realization of second order multifunctional filter [P5] has been obtained through the inductance simulation approach applied on a passive RLC prototype band pass filter of Fig. 4.16 (a). On replacing the inductor (L) by the GIS, the CCCII-based realization of the corresponding active RC BP-filter of Fig. 4.16 (b) is obtained.

The circuit besides realizing BP response at node 3 \((V_3 = V_{BP})\) additionally realizes a standard LP response at node 2 \((V_2 = V_{LP})\). These are given by:
\[
T_{lp}(s) = \frac{V_2}{V_1} = -\frac{1}{R_1 R_s C_1 C_2 D(s)} \quad (4.32)
\]

\[
T_{hp}(s) = \frac{V_3}{V_1} = -\frac{s}{R_1 C_1 D(s)} \quad (4.33)
\]

where the denominator \(D(s)\) is:

\[
D(s) = s^2 + \frac{1}{R_s C_1} + \frac{1}{R_{x3} R_s C_1 C_2} \quad (4.34)
\]

It may be noted that the passive resistor \(R_1\) in the circuit can also be replaced by CCC-II based tunable floating resistor [89], shown in Fig. 4.17 (a). The filter then becomes a CCCII-C realization with suitability to monolithic CMOS fabrication. The low pass and band pass responses using the active resistor \((R_{x3})\) remains same as given by eqns. (4.32) and (4.33), respectively, with \(R_{x3}\) replacing passive \(R_1\), where \(R_{x3} = V_T/2I_o\) in Bipolar case, and \(R_{x3} = 14.96/\sqrt{I_o}\) in MOS/CMOS case.

**HP-realization:** If the input and ground terminals of the filter are interchanged, then band pass and high pass filter responses are respectively realized at \(V_2\) and

![Fig. 4.17 (a) Tunable positive floating R (b) Tunable positive grounded R](image-url)
V3. Routine analysis of the circuit of Fig.4.16 (b) after the transformation gives the inverting band pass and non-inverting high pass responses as:

\[ T_{BP2}(s) = \frac{V_2}{V_i} = -\frac{s}{R_{x_2}C_2D(s)} \] (4.35)

\[ T_{HP2}(s) = \frac{V_3}{V_i} = \frac{s^2}{D(s)} \] (4.36)

Once again, its CCCII-C version is obtained by now replacing the grounded passive resistor \( R_1 \) by the active grounded resistor \( R_{x_3} \), shown in Fig. 4.17(b). The resulting band pass and high pass responses are again given by eqns. (4.35) and (4.36) by replacing passive \( R_1 \) by active \( R_{x_3} \).

**Filter parameters:** The biquadrate filter parameters, viz., pole frequency \( \omega_0 \) and pole- \( Q \), of the LP and BP filters, with passive resistor \( R_1 \), are given as:

\[ \omega_0 = \sqrt{\frac{1}{R_{x_1}R_{x_2}C_1C_2}}, \quad Q = R_1 \sqrt{\frac{C_1}{R_{x_1}R_{x_2}C_2}} \] (4.37)

In the LP-BP realization, the corresponding filter gains are given by eqn. (4.38 a)

\[ |H_{LP1}| = \frac{R_{x_1}}{R_1}, \quad |H_{BP1}| = 1 \] (4.38 a)

On interchanging the terminals, the HP-BP realization gives the corresponding gains:

\[ |H_{HP2}| = \frac{R_{x_2}C_1}{R_{x_2}C_2}, \quad |H_{BP2}| = 1 \] (4.38 b)

In the CCCII-C (using active R’s), the pole- \( \omega_0 \) and pole- \( Q \), are given by:

\[ \omega_0' = \sqrt{\frac{1}{R_{x_1}R_{x_2}C_1C_2}}, \quad Q' = R_{x_1} \sqrt{\frac{C_1}{R_{x_1}R_{x_2}C_2}} \] (4.39 a)
In the corresponding LP-BP realization, the filter gains are obtained as:

\[
\left| H_{L,P}\right| = \frac{R_h}{R_o}, \quad \left| H_{BP}\right| = 1 \tag{4.39 b}
\]

and in the HP-BP realization the gain expressions are:

\[
\left| H_{HP2}\right| = \frac{R_x C_1}{R_o C_2}, \quad \left| H_{HP2}\right| = 1 \tag{4.39 c}
\]

Without any loss of generality we can select in the design: for \( R_1 = R_2 = R_x \) (i.e., \( I_o = I_{o_1} \)) and \( C_1 = C_2 = C \). This simplifies the parameter expressions as:

\[
\omega_o' = \frac{1}{R_x C}, \quad Q' = \frac{R_x}{R_o} \tag{4.40 a}
\]

\[
\left| H_{L,P}\right| = \frac{R_x}{R_o}, \quad \left| H_{BP}\right| = 1 \quad \text{(for LP-BP case)} \tag{4.40 b}
\]

\[
\left| H_{HP2}\right| = \frac{R_x}{R_o}, \quad \left| H_{HP2}\right| = 1 \quad \text{(for HP-BP case)} \tag{4.40 c}
\]

It may be concluded that using the inductance simulation approach on a passive RLC prototype BP filter, a low component CCCII-based realization is obtained. It realizes standard second order LP, BP and HP responses without the requirement of component matching. The circuit has attractive advantage of electronic tunability (programmability) with bias control. The MBF can easily be converted into CCCII-C realization which is ideally suited to monolithic fabrication. The circuit has attractive sensitivity. The gain of the LP and BP filters can be tuned independently through \( R_1 \) without disturbing the pole-\( \omega_o \). In the CCCII-C case, corresponding bias control may be used in the gain adjustment. In tuning the filter, first pole-\( \omega_o \) is adjusted through \( I_{o_1}, I_{o_2} \) (\( R_{s_1}, R_{s_2} \)). The pole-Q is then set by varying \( I_{o_1} \), without disturbing \( \omega_o \).
4.5.1 Non-ideal analysis

Taking the frequency independent non-idealities into consideration, the low pass and band pass transfer functions of the circuit of Fig.4.16 (b) at V₂ and V₃, are:

\[ T_{LP}(s) = \frac{V_2}{V_1} = \frac{\alpha_2 \beta_2}{R_1 R_x C_1 C_2 D(s)} \]  \hspace{1cm} (4.41)

\[ T_{BP}(s) = \frac{V_3}{V_i} = \frac{s}{R_1 C_1 D(s)} \]  \hspace{1cm} (4.42)

With the interchanged input and ground terminals of the filter circuit of Fig.4.16 (b), the band pass and high pass transfer functions, at V₂ and V₃, are respectively given by:

\[ T_{BP}(s) = \frac{V_3}{V_i} = \frac{s \alpha_2 \beta_2}{R_1 C_2 D(s)} \]  \hspace{1cm} (4.43)

\[ T_{HP}(s) = \frac{V_3}{V_i} = \frac{s^2}{D(s)} \]  \hspace{1cm} (4.44)

where the denominator is given by

\[ D(s) = s^2 + \frac{s}{R_x C_1} + \frac{\alpha_2 \beta_1 \beta_2}{R_x R_x C_1 C_2} \]  \hspace{1cm} (4.45)

The biquadrate filter parameters are

\[ \omega_o = \sqrt{\frac{\alpha_1 \alpha_2 \beta_1 \beta_2}{R_x R_x C_1 C_2}} \] \hspace{1cm} (4.46 a)

\[ Q = R_1 \sqrt{\frac{\alpha_1 \alpha_2 \beta_1 \beta_2}{R_x R_x C_1 C_2}} \] \hspace{1cm} (4.46 a)

\[ |H_{LP}'| = \frac{R_x}{R_x \alpha_1 \beta_1}, \quad |H_{BP}'| = 1 \] (for LP-BP case) \hspace{1cm} (4.46 b)

\[ |H_{BP}'| = \frac{\alpha_2 \beta_2 R_x C_1}{R_x C_2}, \quad |H_{HP}'| = 1 \] (for HP-BP case) \hspace{1cm} (4.46 c)

At low to medium frequencies (f ≈ 10 MHz), the circuit continues to provide standard second order responses. There is slight reduction in pole \( \omega_o \), pole-Q,
and $H'_{BP2}$. The filter gain $H'_{LP1}$ is slightly increased, while the filter gains $H'_{BP1}$ and $H'_{HP2}$ remains unaffected by the non-idealities.

### 4.5.2 Sensitivity study

The active and passive sensitivities of the filter parameters, $\omega_o$ and $Q$, and filter gains, are evaluated and are given below:

$$
S_{R_a,R_b}^{o_o} = S_{C_1,C_2}^{o_o} = -\frac{1}{2}, \quad S_{R_a,R_b}^{Q} = 1, \quad S_{C_1}^{Q} = \frac{1}{2}, \quad S_{R_a,R_b}^{Q} = -\frac{1}{2}, \\
S_{C_2}^{Q} = -\frac{1}{2}, \quad S_{R_a}^{H'_{LP1}} = S_{R_a}^{H'_{HP1}} = 1, \quad S_{R_a}^{H'_{BP1}} = S_{R_a}^{H'_{BP1}} = 1,
$$

$$
S_{R_a,R_b,C_1,C_2}^{H'_{BP1}} = 0, \quad S_{R_a,R_b,C_1,C_2}^{H'_{BP1}} = 0
$$

(4.47)

The sensitivity of the filter parameters, (with non-idealities) are also evaluated and are given as:

$$
S_{\alpha,\alpha,\beta,\beta}^{o_o} = \frac{1}{2}, \quad S_{\alpha,\alpha,\beta,\beta}^{Q} = \frac{1}{2}, \quad S_{\alpha,\beta_1}^{H'_{LP1}} = -1, \quad S_{\alpha,\beta_2}^{H'_{BP1}} = 1,
$$

$$
S_{\alpha,\alpha,\beta,\beta}^{H'_{BP1}} = 0, \quad S_{\alpha,\alpha,\beta,\beta}^{H'_{BP1}} = 0
$$

(4.48)

All the sensitivities are found to be low and attractive.

### 4.5.3 Design and simulation

The performance of the multifunctional filter was verified through PSpice simulation using CCCII model of Ref [75]. The filter circuit was designed for low pass, high pass and band pass responses for a pole frequency ($f_o$) equal to 500 KHz at $Q$ of 0.707. Preselecting: $C_1 = C_2 = 40$ pF, $R_i = R_a = R_b$ is obtained as 7.96 K$\Omega$. The corresponding bias currents are, $I_o = I_{o_1} = 3.5 \mu A$. The value of $R_i$ is found to be 5.63 K$\Omega$. In the filter realization, high pass and band pass gains are inherently unity. However, the gains for low pass filter case comes out to be $H_{LP1} = 1.41$. In the CCCII-C version, $R_j = R_i = 5.63$ K$\Omega$ corresponds to $I_{o_1} = 7.06 \mu A$. The simulation results for HP and BP responses are shown in Fig. 4.18 and that of low pass
response in Fig. 4.19, along with simulated parameter values. These are found to be in conformity with the design.

The $f_o$-tunability of the band pass filter was investigated by changing $f_o$ of the filter through $R_z$, i.e., $I_o (= I_{o_1} = I_{o_2})$, at a constant $Q$ of 10. The responses
corresponding to \( I_o = 0.14 \mu A (R_s = 39.78 \text{ K}\Omega) \), 1.3 \( \mu A (R_s = 13.26 \text{ K}\Omega) \), and 14.19 \( \mu A (R_s = 3.97 \text{ K}\Omega) \), respectively, require (keeping Q constant) passive resistors \( R_1 = 397.8 \text{ K}\Omega \), 132.6 \( \text{ K}\Omega \), and 39.7 \( \text{ K}\Omega \). In the active-C realization, the corresponding values of \( I_o = 0.014 \mu A (R_s = 397.8 \text{ K}\Omega) \), 0.013 \( \mu A (R_s = 132.6 \text{ K}\Omega) \), and 0.14 \( \mu A (R_s = 39.7 \text{ K}\Omega) \) with the active resistor \( (R_s) \). The corresponding BP responses at a constant Q of 10 and variable \( f_o \) are shown in Fig. 4.20, along with the simulated results. The results show a convenient tunability of \( f_o \) with bias control.

![Simulated results](chart)

<table>
<thead>
<tr>
<th>( f_o )</th>
<th>Q</th>
<th>H_{BP}</th>
</tr>
</thead>
<tbody>
<tr>
<td>100.02KHz</td>
<td>10.2</td>
<td>10.01</td>
</tr>
<tr>
<td>300.03KHz</td>
<td>9.98</td>
<td>10.03</td>
</tr>
<tr>
<td>1.04 MHz</td>
<td>9.92</td>
<td>10.03</td>
</tr>
</tbody>
</table>

Fig.4.20 Tuning of \( f_o \) at constant Q = 10 with passive and active resistors

(i) \( f_o = 100 \text{ KHz} \) (ii) \( f_o = 300 \text{ KHz} \) (iii) \( f_o = 1 \text{ MHz} \)

Next, independent tuning of Q was demonstrated by designing the BP filter at fixed \( f_o = 500 \text{ KHz} \) and changing its Q through passive resistor \( R_1 \) and the simulated resistor \( R_s (\text{i.e., } I_o) \). The corresponding results for Q = 5, 10, and 20 are obtained with passive resistor, \( R_1 = 39.75 \text{ K}\Omega \), 79.5 \( \text{ K}\Omega \), 159 \( \text{ K}\Omega \). For the CCCII-C realization, the corresponding values of \( I_o = 0.14 \mu A (R_s = 39.75 \text{ K}\Omega) \)
KΩ), 0.04 μA (R_n = 79.5 KΩ), and 0.008 μA (R_n = 159 KΩ) used with the active resistor (R_n). The curves are shown in Fig. 4.21, along with the simulated results. The theoretical and simulated values of pole-Q exhibit convenient tuning of pole-Q, without affecting the pole frequency (ω_n).

<table>
<thead>
<tr>
<th>Theoretical Q</th>
<th>Simulated Q</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>4.35</td>
</tr>
<tr>
<td>10</td>
<td>9.56</td>
</tr>
<tr>
<td>20</td>
<td>19.25</td>
</tr>
</tbody>
</table>

Fig. 4.21 Tuning of pole Q at constant f_o = 500 KHz with passive and active resistors
(i) Q = 5 (ii) Q = 10 (iii) Q = 20

Electronically tunable ideal grounded inductor is realized employing two Current Controlled Conveyors (CCCIIs), along with a grounded capacitor. Through L-replacement scheme, a band pass filter is obtained which gives additional standard second order, low pass and high pass responses. The design of multifunctional filter is free from matching constraints and provides, independent tuning of the quality factor and pole frequency. The gain of the band pass filter and low pass filter can be tuned independently through R_i/R_n, without disturbing the pole frequency. The filter also enjoys attractive features, such as, low component count, high-Q realization, low voltage operation, low
sensitivity performance and convenient wide range tunability of important filter parameters. The CCCII-C version is suited to monolithic IC implementation.

4.6 Realization of CCCII-C Universal Biquadratic Filter

This Section presents a novel voltage-mode universal biquadratic filter having multi inputs and single output. Taking a clue from the CCII-based UBF realization with multi input and single output, the present realization is expected to give low component filter circuit with a variety of standard responses. It will be shown that the realized UBF indeed gives a canonical structure with all standard second order responses.

4.6.1 Circuit description

The proposed circuit of the universal biquadratic filter [P7] is shown in Fig. 4.22. It uses only two capacitors and two CCCIIIs in its realization. The parasitic resistance at the X-inputs of the CCCII's is, \( R^i = \frac{1.96 I_a}{I_a} \), \( i = 1, 2 \), where \( I_a \) is the bias control current. Routine analysis of the UBF gives the general output function:

\[
V_o = \frac{s^2 V_4 + s \left( \frac{1}{R_x C_2} V_3 - \frac{1}{R_x C_2} V_2 + \frac{1}{C_2 R_x} V_1 \right) + \frac{V_1}{R_x R_x R_x C_2 C_2}}{s^2 + s \frac{1}{C_2 R_x} + \frac{1}{R_x R_x C_2 C_2}}
\]  

From eqn. (4.49), various filter responses can be obtained through appropriate selection of the inputs as follows:

(i) HP-response with \( V_4 = V_{in}, V_1 = V_2 = V_3 = 0 \);
(ii) NIBP-response with \( V_3 = V_{in}, V_1 = V_2 = V_4 = 0 \);
(iii) IBP-response with \( V_2 = V_{in}, V_1 = V_3 = V_4 = 0 \);
(iv) LP-response with \( V_1 = V_2 = V_{in}, V_3 = V_4 = 0 \), and \( R_{x1} = R_{x2} \);
(v) BE-response with \( V_1 = V_2 = V_4 = V_{in}, V_3 = 0 \), and \( R_{x1} = R_{x2} \);
(vi) AP-response with \( V_1 = V_2 = V_4 = V_{in}, V_3 = 0 \), and \( R_{x1} = 2R_{x2} \);
It may be noted that for the realizations of LP, NIBP and IBP responses [case (i) to (iii)], matching constraints are not required. The constraints in the case of LP, BE and AP cases are also simple to satisfy through design, particularly in monolithic technologies, where inherently matched devices are available. From the characteristic polynomial, \( D(s) \), the pole frequency \( \omega_p \) and the pole-Q of the proposed UBP are obtained as:

\[
\omega_p = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}}, \quad Q = \frac{R_1}{\sqrt{R_2 R_1 C_1 C_2}}
\]  

(4.50)

### 4.6.2 Non-ideal analysis

Considering the non-idealities of CCCII's at low to medium frequencies \( (f \leq 10 \text{ MHz}) \), the denominator of the transfer functions in eqn. (4.49) modifies to:

\[
D'(s) = s^2 + s \frac{\alpha_1 \beta_1}{C_2 R_1} + \frac{\alpha_1 \alpha_2 \beta_1 \beta_2}{R_2 R_1 C_1 C_2}
\]  

(4.51)

Hence, the filter parameters with non-idealities are given by:
It is evident from eqn. (4.52) that the pole frequency \( \omega_o \) decreases. However, the pole-Q has negligible effect of \( \alpha \) and \( \beta \) of the CCCII.

### 4.6.3 Sensitivity study

The sensitivities of pole-\( \omega_o \) and pole-Q with respect to the active and passive components are evaluated and summarized as given below:

\[
S^\omega_{R_1, R_2, C_1, C_2} = \frac{1}{2}, \quad S^Q_{R_1, C_1} = -\frac{1}{2}, \quad S^Q_{R_1, C_2} = \frac{1}{2}
\]

\[
S^\omega_{\alpha_1, \alpha_2, \beta_1, \beta_2} = \frac{1}{2}, \quad S^Q_{\alpha_1, \alpha_2} = -\frac{1}{2}, \quad S^Q_{\alpha_1, \beta_2} = \frac{1}{2}
\]  

(4.53)

It is clear from eqns. (4.53) that all the active and passive sensitivity figures are equal to half in magnitude, which is an attractive performance feature of the UBF.

### 4.6.4 Design and simulation

The performance of the universal biquadratic filter was verified through PSpice simulation using CCCII model of [75]. Initially, low pass band pass, high pass, band reject and all pass responses of the UBF were designed for \( f_o = 500 \text{ KHz} \) at \( Q = 0.707 \). For \( I_{o_1} = I_{o_2} = I_o = 0.89 \mu \text{A} \) corresponding to \( R_s = R_t = R = 15.9 \text{ K} \Omega \), eqn. (4.51) yields \( C_1 = 28 \text{ pF} \) and \( C_2 = 14 \text{ pF} \). The simulated UBF responses are shown in Fig. 4.23. The simulated values for the band pass case are \( f_o = 500.06 \text{ KHz} \) and \( Q = 0.705 \). This shows close agreement with the theory.

The UBF was then tuned by controlling the \( I_{o_1} (R_s) \). The BP responses corresponding to \( f_o = 300 \text{ KHz} \), \( f_o = 500 \text{ KHz} \) and \( f_o = 1 \text{ MHz} \) are given in
Fig. 4.24. The simulated results show convenient tunability and close conformity with the theory.

<table>
<thead>
<tr>
<th>Simulated results</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_o$ (KHz)</td>
</tr>
<tr>
<td>500.06</td>
</tr>
</tbody>
</table>

Fig. 4.23 Frequency response of the CCCII based UBF

Fig. 4.24 Frequency tuning of non inverting BPF at constant $Q = 5$
The proposed UBF uses only two CCCIIs and two capacitors in its realization and thus has a canonical topology. The realized filter gives six standard biquadratic responses, viz., low pass (LP), high pass (HP), non-inverting band pass (NBP), inverting band pass (IBP), band elimination (BE) and all pass (AP), through appropriate selection of inputs. In an IC version, this selection may be done through a simple electronic switching arrangement [140]. The proposed UBF has advantages of low component count, wide range electronic tunability, low active and passive sensitivity figures, compatibility to monolithic implementation in CMOS IC technology and use of low supply voltage operation, over previously reported filters [48-91].

4.7 Realization of Higher Order CM Butterworth LP filter

Doubly terminated passive RLC ladder filters have the inherent advantage of low sensitivity. Higher order filters are frequently realized in the form of ladder structures [92-100]. These inherit the sensitivity characteristics of the passive RLC ladders. Consequently, many current mode ladder filters had been reported [92-100]. In [92, 94], all the circuits are obtained from the operational simulation method for realizing the transfer function, and require a large number of active and passive components. In Refs [93, 95], the current mode third order Butterworth low pass filter is realized having a large number of passive components, out of which a few resistors and capacitors are floating. In [96], linear transformation is required to realize active ladder filters having good performance, but this method requires solution of large number of mathematical equations and the design frequency is determined by passive elements. Current mode leapfrog ladder filter is realized using CDBA in [97], which has high frequency and low voltage operation, but require a large number of passive components, along with several floating resistors. In [98], active-C current mode fifth order ladder filters is realized employing seven multi output current controlled conveyors (MO-CCCII), and five capacitors. In some recent work [99], current mode third order elliptic filter is reported
employing seven multi output current controlled conveyors (MO-CCCII), and four capacitors. Recently in [100], current mode third order elliptic filter is presented using five MO-CCCIIIs and four capacitors, out of which two capacitors are floating.

It may be seen that although a wide variety of realizations of current mode ladder filters exist, they suffer from some specific drawbacks and there is need to find more attractive current mode ladder realizations. In this Section, we study the realization of a current mode ladder filter using second generation current controlled conveyors and grounded capacitors. The method is based on inductance simulation approach, in which the inductors of the prototype filter, are simulated using CCCII and capacitors and resistors are by CCCII itself. The proposed circuit is simple and easy to design, without the need of matching constraints. The circuit has the attractive features of low component count and low supply voltage operation, over the previously reported literature [92-100]. Electronic tunability and use of all grounded capacitors makes the circuit realizations attractive for IC implementation.

### 4.7.1 Realization of fifth order LP Ladder Filter

In this Section, inductance simulation approach is employed for the realization of CCC-II based current mode fifth order Butterworth low pass ladder filter derived from the doubly terminated passive RLC low pass ladder filter. The CM fifth order Butterworth low pass RLC ladder filter is shown in Fig. 4.25.

![Fig. 4.25 Prototype current mode fifth order Butterworth low pass RLC ladder filter](image)
The relations of the currents and voltages in the filter can be interrelated by:

\[ I_1 = I_S - \frac{V_1}{R_m} - I_2, \quad V_1 = Z_1 I_1 \]

\[ I_2 = Y_2 V_2, \quad V_2 = V_1 - V_3 \]

\[ I_3 = I_2 - I_4, \quad V_3 = Z_3 I_3 \]

\[ \vdots \]

and

\[ I_{n-1} = Y_{n-1} (V_{n-2} - V_n), \]

\[ V_n = Z_n (I_{n-1} - I_n) \quad (4.54) \]

Now all the floating inductances of the circuit are replaced by CCC-II based tunable floating inductor [101], shown in Fig. 4.26, and the grounded resistors are replaced by the CCC-II based grounded resistor [89] given in Fig. 4.17.

Fig. 4.26 Tunable floating inductor and its equivalent passive inductor
Using direct replacement of inductors and resistors, the resulting active
-C circuit derived from the passive RLC low pass ladder is shown in Fig. 4.27. It may be noted that the ladder now comprises of only DO-CCCII and grounded capacitors. The realized circuit comprises of minimum requirement of six DO-CCCII and five grounded capacitors, as compared to larger component count in previously reported literature [92-100]. It is also simple to design and does not have any matching constraints. The realization is also ideally suited to monolithic CMOS implementation.

4.7.2 Design and simulation
The performance of the fifth order Butterworth low pass ladder filter was verified through PSpice simulation using CCCII model of Ref [75]. The filter is first designed in the normalized form with the component relationship:

\[ R_n = R_m \quad \text{and} \quad L_n = L_m \quad \text{and} \quad C_n = C_m \]

The normalized values of the circuit components for the fifth order Butterworth low pass ladder filter [70] are: \( R_m = R_o = 1 \Omega \), \( C_1 = C_4 = 0.618 \text{ F} \), \( C_3 = 2 \text{ F} \) and \( L_2 = L_4 = 1.618 \text{ H} \). For denormalization, the frequency scaling factor \( K_f \) is equal to \( 2 \pi f_o \text{ rad/s} \), where \( f_o \) is the cutoff frequency of the low pass filter to be realized. The magnitude scaling factor \( K_m \) is selected as 1300 for obtaining convenient
component values. Then the denormalized component values for \( f_c = 10 \text{ MHz} \) are obtained as: \( R_{x_1} = R_{x_0} = 1.3 \, \text{kΩ} \), corresponding to \( I_{x_1} = I_{x_0} = 132 \, \text{μA} \). \( C_1 = C_5 = 7.5 \, \text{pF} \). For \( L_2 = L_4 = 33.47 \, \text{μH} \), selecting \( C_2 = C_4 = 7.5 \, \text{pF} \), gives \( R_{x_1} = R_{x_2} = R_{x_3} = R_{x_4} = 2.11 \, \text{kΩ} \) corresponding to \( I_{x_1} = I_{x_2} = I_{x_3} = I_{x_4} = 50.2 \, \text{μA} \).

The simulated and theoretical frequency responses are shown in Fig. 4.28, which overlaps each other over the entire range. The simulated cutoff frequency is found to be equal to 10.08 MHz and exhibits close agreement with the design value.

![Simulated and theoretical frequency responses](image)

Fig. 4.28: Frequency response of 5th order Butterworth low pass ladder filter

### 4.8 Conclusion

In this Chapter, CCCII-based novel circuits which may find ready applications in ASP are realized and studied. These incorporate electronic tunability (programmability) through bias current control of the conveyor. Most of these realizations are suitable for implementation in the contemporary CMOS technology.
A novel circuit using two CCCIIs is presented for the realization of CM analog multiplier and divider. The circuit performs ideal multiplication and division without the requirement of matching constraints. They have the attractive properties of low sensitivities, excellent high frequency performance and insensitivity to temperature variations. The use of all-active devices and electronic tunability makes them highly suitable for CMOS implementation. An ideal grounded inductance simulator (GIS) is realized using two CCCIIs alongwith, a grounded capacitor. It is free from matching constraint. It exhibits only slight L- enhancement due to device non-idealities. The circuit also enjoys attractive sensitivity properties.

A generalized scheme is given for the realization of component multipliers using a CCII and a CCCII, alongwith, two grounded impedances. The scheme is used in the realization of R and C-multipliers. A slight modification gives a CCCII-based R-multiplier. All the circuits enjoy attractive sensitivity properties and are not seriously affected by the non-idealities of conveyor. An MBF is realized using GIS considered earlier in the Chapter. The resulting CCCII-RC circuit gives LP, HP and BP responses. The circuit is modifies to realize a CCCII-C structure suitable for monolithic fabrication. The circuits enjoy low sensitivities, independent Q-tunability and are not seriously affected by the non-idealities of active device.

Next, the realization of canonical CCCII-C UBF is given. The circuit realizes all standard second order filter responses. It has low sensitivity. Also, the Q of the filter is unaffected by the device non-idealities. Finally, the realization of higher order (n = 5) CM Butterworth LP filter is given, which is obtained from the corresponding RLC LP-ladder. The circuit uses only CCCII and grounded capacitors, which make it highly suitable for CMOS implementation.

All the realizations considered in the Chapter are simulated through PSpice. Close agreement is obtained between the simulation and the design.