CHAPTER 2

LITERATURE REVIEW

The literature review focuses its attention on FIR filter, particularly to utilize low power consumption, better performance and improved efficiency. The implementation feasibility in VLSI environment is also studied and analyzed in depth.

FIR filters play a crucial role in many signal processing applications in communication systems. A wide variety of tasks such as spectral shaping, matched filtering, interference cancellation, channel equalization, etc. can be performed with these filters. Hence, various architectures and implementation methods have been proposed to improve the performance of filters in terms of speed, power and complexity.

2.1 ARCHITECTURAL APPROACH FOR FIR FILTER DESIGN

Tian-Sheuan Chang and Chein-Wei Jen (1998) presented a low power and high speed FIR filter designs by using first order difference between inputs and various orders of differences between coefficients. Further, they adopted the Distributed Arithmetic (DA) architecture to exploit the probability distribution aiming to reduce the power consumption. The design was applied to an example FIR filter to quantify the energy savings and speedup. It showed lower power consumption than the previous design with the comparable performance (Sankarayya et al 1997).
Evangelos et al (2006) developed a custom Very-Large-Scale-Integration architecture, which consists of a reconfigurable hardware substrate and a hybrid-genetic algorithm responsible for resolving the optimal configuration for the reconfigurable components of the substrate. The reconfigurable hardware was specifically tailored for the implementation of multiplierless symmetrical FIR filters based on the primitive operator technique, while the architecture of the hybrid genetic algorithm aims to improve the quality of the realized filters and speeding up the time required for their realization. Power analysis demonstrates that the filters, which are implemented by their architecture, consumed considerably less power than industrial Field Programmable Gate Arrays, targeting similar applications.

An architecture for implementing low complexity and reconfigurable FIR filters was proposed by Mahesh et al (2007). It has been applied for channelizers. Their method was based on the Binary Common Sub-expression Elimination (BCSE) algorithm. The suggested architecture guaranteed minimum number of additions at the adder level and also at the Full Adder (FA) level for realizing each adder needed to implement the coefficient multipliers. Further, they synthesized the architecture on 0.18μm CMOS technology. The synthesis results showed that the proposed reconfigurable FIR filter can operate at high speed consuming minimum area and power. The average reductions in area and power were found to be 49% and 46% respectively with an average increase in speed of operation of 35% compared to other reconfigurable FIR filter architectures in literature.

A high performance and low power FIR filter design, which was based on Computation Sharing Multiplier (CSHM) was described by Jongsun Park et al (2002). The CSHM specifically targeted the computation re-use in vector-scalar products and was effectively used in the suggested FIR filter
design. Efficient circuit level techniques namely a new carry select adder and Conditional Capture Flip-Flop (CCFF), were also used to further improve power and performance. The suggested FIR filter architecture was implemented in 0.25 μm technology. Experimental results on a 10 tap low pass CSHM FIR filter showed speed and power improvement of 19% and 17%, respectively (Potkonjak et al 1996).

In Bruce et al (2004), power optimization techniques were applied to a reconfigurable digital FIR filter used in a Universal Mobile Telephone Service (UMTS) mobile terminal. Various methods of optimization for implementation were combined to achieve low cost in terms of power consumption. The optimization methods have achieved a 78.8 % reduction in complexity for the multipliers in the FIR structure. A comparison of synthesized RTL models of the original and the optimized architectures resulted in a 27% reduction in look-up tables when targeted for the Xilinx Virtex II Pro FPGA.

Reconfigurable Multiplier Blocks (ReMB) was addressed by Süleyman Sirri Demirsoy et al (2004) to complexity reductions in multiple constant multiplications in time-multiplexed digital filters. The ReMB technique was employed in the implementation of a half-band 32-tap FIR filter on Xilinx Virtex FPGA. Reference designs had also been built by deploying standard time-multiplexed architectures and off-the-shelf Xilinx Core Generator system for the FPGA design. All designs were then compared for their area and delay figures. It was shown that the ReMB technique can significantly reduce the area for the multiplier circuitry and the coefficient store, as well as reducing the delay.
2.2 LOW POWER IMPLEMENTATIONS OF FIR FILTER

Ahmet Teyfik Erdogan et al (2002), presented three multiplication schemes for the low-power implementation of FIR filters on single multiplier Complementary Metal–Oxide–Semiconductor (CMOS) Digital Signal Processors (DSPs). The schemes achieved power reduction through the minimization of switching activity at one or both inputs of the multiplier. In addition, these schemes are characterized by their flexibility since they tradeoff implementation cost against power consumption. Results were provided for a number of example FIR filters demonstrating power savings ranging from 20% with schemes which can be implemented on existing common DSPs, and up to 51% with schemes using enhanced DSP architectures.

Erdogan et al (2004), indicated that there is a continuous drive for methodologies and approaches of low power design. This was mainly driven by the surge in portable computing. On the other hand, the design of low power systems for different portable applications was not a simple task. This was because of the number of constraints that influence the power consumption of a device. In addition to issues of performance and functionality, there was a need to satisfy strict test coverage constraints. The authors investigated the impact of DSP architectural realisation, multiplier type and the choice of number representation on the overall power consumption of DSP devices. Furthermore, the effect of DFT circuits on the overall performance was studied. A hearing aid device was considered to be an example of a system with strict power/area constraints. It was shown that the choice of multiplier architecture and number representation should be carefully considered when specific DSP architectural choices were made. The results were demonstrated with a number of specially designed DSP
architectures for the implementation of FIR filtering algorithms on hearing aid devices.

Lu et al (1997) suggested a method for the design of FIR digital filters with low power consumption. In this method, the digital filter was implemented as a cascade arrangement of low-order sections. The first section was designed through optimization so as to satisfy as far as possible, the overall required specifications. The first section was then fixed and a second section was added. It was so designed that the first two sections in cascade satisfy again as far as possible the overall required specifications. This process was repeated until a multi-section filter was obtained which would satisfy the required specifications under the most critical circumstances imposed by the application at hand. In multi-section filters of this type, the minimum number of sections required to process the current input signal can be switched in through the use of a simple adaptation mechanism and, in this way, the power consumption can be minimized. This design strategy was achieved by formulating the design of the \( k \)th section as a weighted least-squares minimization problem, assuming that an optimum \((k-1)\)-section design was available.

In Mahesh Mehendale et al (1998), the problem of reducing power was addressed to FIR filters implemented on Programmable DSP’s. They described a generic DSP architecture and identified the main sources of power dissipation during FIR filtering. They presented seven transformations to reduce power dissipated in one or more of these sources. These transformations complement each other and together operate at algorithmic, architectural, logic and layout levels of design abstraction. They showed that the power dissipation can be reduced by more than 40% using these transforms. The transformations have been encapsulated in a framework that
provides a comprehensive solution to low-power realization of FIR filters on programmable DSP’s.

Parhi (2001) reported that reduction of power consumption is significantly important for all high-performance digital VLSI systems. Several approaches for low-power implementations of building blocks for digital subscriber line (DSL) systems were reviewed. Low-power implementations of Reed–Solomon (RS) coders, Fast Fourier transforms (FFTs), FIR filters, and equalizers, and reduction of power consumption by use of dual supply voltages were addressed. It was shown that use of separate Galois Field functional units for multiply-accumulate and degree reduction can reduce the energy consumption of RS coders dramatically. A hybrid feed forward and feedback commutator scheme-based FFT was shown to require less area and full hardware utilization efficiency. Reduction of switching activity at one or both inputs of the multipliers was a key to the reduction of power consumption in FIR filters and equalizers. The switching activity was reduced by the use of transpose structure and by time-multiplexing of an unfolded filter. A well established retiming approach was generalized to find those noncritical gates which can be operated with lower supply voltages to reduce the overall system power consumption.

A hierarchical automated design flow was described by Rhett Davis (2002) for low-energy direct-mapped signal processing integrated circuits. A modular framework based on a combined dataflow graph and floor plan description drives automatic layout generation with commercial CAD tools. It was reported that automatic characterization of layout improved the system-level estimates. The simplified physical design methodologies were discussed for low supply voltages. The flow was demonstrated on a 300-k transistor test-chip, a time-division multiple-access baseband receiver, and a soft-output Viterbi decoder.
In Kyung-Saeng Kim et al (2003), a 32-tap finite impulse response (FIR) filter was described with two 16-tap macros suitable for multiple taps. The derived condition for a coded coefficient and data block showed 35% savings in power consumption and 44% improvement in occupied area compared to a typical radix-4 modified Booth algorithm. According to the condition and separated shifting-accessing clock scheme, they implemented a 32-tap FIR filter in 0.6 µm CMOS technology with three levels of metal.

Tobias Gemmeke et al (2004) reported that power dissipation along with silicon area became the key figure in chip design. They presented a design methodology reducing any combination of cost drivers subject to a specified throughput. As a basic principle, the optimization regards the existing interactions within the design space of a building block. Crucial in such optimization was the proper dimensioning of device sizes in contrast to the common use of minimal dimensions in low-power implementations. Taking the design space of an FIR filter as an example, the different steps of the design process were highlighted resulting in a low-power high-throughput filter implementation. This filter reported to have less silicon area than other state-of-the-art filter implementations, and it disrupts the average trend of power dissipation by a factor of 6.

Kuan-Hung Chen and Tzi-Dar Chiueh (2006) presented a digit-reconfigurable finite impulse response (FIR) filter architecture with a very fine granularity. It provided a more flexible yet compact and low-power solution to FIR filters with a wide range of precision and tap length compared to the previous architecture (Li et al 2002). Based on the suggested architecture, an 8-digit reconfigurable FIR filter chip was implemented in a single-poly quadruple-metal 0.35 µm CMOS technology. Measurement results showed that the fabricated chip operates up to 86 MHz when the filter draws 16.5 mW of power from a 2.5 V power supply.
Fei Xu et al (2007) suggested a new algorithm for the synthesis of low-complexity FIR filters with resource sharing. The original problem statement based on the minimization of Signed-Power-of-Two (SPT) terms had been reformulated to account for the sharable adders. The minimization of Common SPT (CSPT) terms that were considered in their proposed algorithm addresses the optimization of the reusability of adders for two major types of common sub-expressions, together with the minimization of adders that are needed for the spare SPT terms. The coefficient set was synthesized in two stages. In the first stage, CSPT terms in the vicinity of the scaled and rounded Canonical Signed Digit (CSD) coefficients were allocated to obtain a CSD coefficient set, with the total number of CSPT terms not exceeding the initial coefficient set. The balanced normalized peak ripple magnitude due to the quantization error was fulfilled in the second stage by a local search method. The algorithm used a common sub-expression based hamming weight pyramid to seek for low-cost candidate coefficients with preferential consideration of shared common sub-expressions. They reported that their algorithm was capable of synthesizing FIR filters with the least CSPT terms compared with existing filter synthesis algorithms.

Ron Ho et al (2008) presented circuits for driving long on-chip wires through a series capacitor. The capacitor improved delay through signal pre-emphasis, offered a reduced voltage swing on the wire for low energy without a second power supply, and reduced the driven load, allowing for smaller drivers. Sidewall wire parasitics were used as the series capacitor to improve process tracking, and the twisted and interleaved differential wires reduced both the coupled noise as well as Miller-doubled cross-capacitance. Multiple drivers sharing a target wire allow simple FIR filters for driver-side pre-equalization. Receivers require DC bias circuits or DC-balanced data. A test chip in a 180 nm, 1.8 V process compared capacitively-coupled long wires with optimally-repeated full-swing wires.
Zhengtao Yu and Xun Liu (2009) reported that Rotary clock is a resonant clocking technique that delivers on-chip clock signal distribution with very low power dissipation. They presented the first rotary-clock-based nontrivial digital circuit. Their design was fully digital and generated using CMOS standard cells in 0.18 μm technology. They showed that the suggested FIR filter was seamlessly integrated with the rotary clock technique. It used the spatially distributed multiple clock phases of rotary clock and achieved high power savings. Simulation results demonstrated that rotary-clock-based FIR filter can operate successfully at 610 MHz, providing a throughput of 39 Gb/s. In comparison with the conventional clock-tree-based design, their design achieved a 34.6% clocking power saving and a 12.8% overall circuit power saving. In addition, the peak current consumed by the rotary-clock-based filter is substantially lower by 40% on the average. Their study makes the crucial step toward the application of rotary clock technique to a broad range of VLSI designs.

Montek Singh et al (2010), designed a high-throughput low-latency digital FIR filter for use in Partial-Response Maximum-Likelihood (PRML) read channels of modern disk drives. The filter was a hybrid synchronous-asynchronous design. The speed-critical portion of the filter was designed as a high-performance asynchronous pipeline sandwiched between synchronous input and output portions, making it possible for the entire filter to be embedded within a clocked system. A novel feature of the filter was that the degree of pipelining was dynamically variable, depending upon the input data rate. This feature was critical in obtaining very low filter latency throughout the range of operating frequencies. The filter was a ten-tap six-bit FIR filter, fabricated in a 0.18 μm CMOS process. Resulting chips were fully functional over a wide range of supply voltages, and exhibited throughputs of over 1.3 giga-items/s and latencies of 2–5 clock cycles. Interestingly, the filter throughput was limited by the synchronous portion of the chip and the
internal asynchronous pipeline was estimated to be capable of significantly higher throughputs, around 1.8 giga-items.

Chong-Fatt Law et al (2011) suggested a set of modeling rules and a synthesis method for the design of asynchronous pipelines. To keep the circuit area and power dissipation of the asynchronous control network small, the suggested approach avoided the conventional syntax directed translation approach. Instead, it employed a data-driven design style and a coarse-grain approach to the synthesis of asynchronous control, restricting asynchronous control to the implementation of communication channels commonly found in asynchronous pipelines and operations involving these channels.

The suggested approach integrates well into conventional synchronous design flows because they are based on Verilog and System Verilog specifications, and generate register-transfer level models suitable for functional simulation and logic synthesis using existing computer-aided design tools. Using a 32-bit microprocessor, an interpolated finite-impulse-response filter bank, and a Reed–Solomon error detector as design examples, they showed that the suggested approach was competitive with other comparable reported methods.

**2.3 DESIGN OF FIR FILTER IN FPGA**

Song Qian and Sun Yi-he (2003) suggested a new systematic method to synthesize the low-complexity and low-power realization of high-order FIR filters in VLSI. First, FIR filer was represented in graph, and the coefficients were reordered to generate an optimal realization structure using minimum spanning tree algorithm. Then the common sub-expressions in the multiple constant multiplier array were extracted and reused to get further reduction in computational complexity. They achieved 36% reduction in implementation complexity without performance degradation.
In Wei Wang et al (2001), several low power techniques were proposed for the FPGA implementation of a distributed arithmetic and residue number system-based FIR filter. Two algorithms were proposed to reduce the size of the residue-to-binary converter, which was reported to be the crucial part of the system. The area, speed and power consumption of the filter were improved accordingly. Furthermore, a Look Up Table (LUT) partition technique was presented such that the most frequently accessed locations are stored in a smaller memory. The power consumption of the LUTs was reduced because the accesses to smaller LUTs dissipate less power. The implementation results showed a 20% power reduction by using the proposed methods.

Shahnam Mirzaei et al (2006) presented a method for implementing high speed FIR filters using adders and hardwired shifts. They used a modified common sub-expression elimination algorithm to reduce the number of adders. They targeted their optimizations to Xilinx Virtex II devices and compared the implementations with those produced by Xilinx CoregenTM using Distributed Arithmetic. It was reported that up to 50% reduction in the number of slices and up to 75% reduction in the number of LUTs for fully parallel implementations were achieved. Further, up to 50% reduction in the total dynamic power consumption of the filters were observed.

The basic structure and hardware characteristics of the FIR digital filter were analysed by Lin Jieshan and Huang Shizhen (2009). Further, they designed the method of the FIR filter on the basis of the FIR filter structure. They focused on the introduction of the overall framework of the FIR digital filter adopting the finite state machine as well as the principle of each module of the design. The design was implemented by the use of Verilog hardware
description language and each module was verified and simulated by Quartus 8.0 and Modelsim-Altera.

Patronis and DeBrunner (2008) identified that in FIR filter design, a sparse filter was one that has a majority of zeros for coefficients. Generally, a sparse filter was designed in order to save area and speed up computations, but while implementing a sparse filter in an FPGA, the expected area savings may not be realized. It showed that FIR filter does not generally translate directly into FPGA space(area) savings on a Virtex-4 FPGA.

Abd Samad Benkrid and Benkrid (2009), presented four novel area-efficient FPGA bit-parallel architectures of FIR filters that smartly support the technique of symmetric signal extension while processing finite length signals at their boundaries. The key to this was a clever use of variable-depth shift registers which were efficiently implemented in Xilinux FPGAs in the form of Shift Register Logic (SRL) components. Comparisons with the conventional architecture of FIR filter with symmetric boundary processing show considerable area saving especially with long-tap filters.

For instance, architecture implementation of the 8-tap low Daubechies-8 FIR filter achieves 30% reduction in the area requirement (in terms of slices) compared to the conventional architecture while maintaining the same throughput. The first architecture was highly area-efficient but requires a clock frequency doubler. Moreover, this speed penalty was cancelled in bi-phase filters which were widely used in multi-rate architectures(e.g., wavelets). Their second symmetric FIR filter architecture saves less logic than the first architecture but overcomes its speed penalty as it matches the throughput of the conventional architecture.
2.4 ALGORITHMS FOR IMPLEMENTATION OF LOW POWER FIR FILTER

Masahiro Murakawa et al (2003), developed a Large-Scale Integration (LSI) for Intermediate Frequency (IF) filters, attaining a 63% reduction in filter area, a 26% reduction in power dissipation, compared with existing commercial products using the same process technology and filter topology, and a yield rate of 97%. The developed chip was calibrated within a few seconds by a genetic algorithm - an efficient AI technique for difficult optimization problems. Their calibration method, which can be applied to a wide variety of analog circuits, leads to cost reductions and the efficient implementation of analog LSIs.

Erdogan et al (2003), presented a number of novel architectures for the implementation of low power FIR filtering cores. These architectures are directly translated from flexible algorithms which exploit data and coefficient correlation in order to minimise the effective switched capacitance on the multiplier, and data/coefficient buses. Another characteristic of these algorithms is that they can be combined to form more power-efficient algorithms which in turn can be mapped to more effective architectures. The work described the FIR filtering architectures and the arithmetic processing cores which characterize individual architectures and provides results which demonstrated up to 39% reduction in power.

A novel algorithm for designing low-power and hardware-efficient linear-phase FIR Filters was developed by Mustafa Aktan et al (2008). The algorithm finds filter coefficients with reduced number of Signed-Power-of-Two (SPT) terms given the filter frequency response characteristics. It was a branch-and-bound-based algorithm that fixes a coefficient to a certain value. The value was determined by finding the boundary values of the coefficient using linear programming. Although the worst case run time of the algorithm
is exponential, its capability to find appreciably good solutions in a reasonable amount of time makes it a desirable CAD tool for designing low-power and hardware-efficient filters. The superiority of the algorithm on existing methods in terms of SPT term count, design time, hardware complexity, and power performance was shown with several design examples. Up to 30% reduction in the number of SPT terms was achieved over un-optimized Remez coefficients, which is 20% better than compared optimization methods. The average power saving was 20% over un-optimized coefficients, which was up to 14% better than optimized coefficients obtained with existing methods.

Pramod Kumar Meher et al (2008), presented the design optimization of one and two dimensional fully pipelined computing structures for area-delay-power-efficient implementation of FIR filter by systolic decomposition of Distributed Arithmetic (DA)-based inner-product computation. The systolic decomposition scheme was found to offer a flexible choice of the address LUT for DA-based computation to decide on suitable area time tradeoff. It was observed that by using smaller address lengths for DA-based computing units, it was possible to reduce the memory size, but on the other hand that leads to an increase of adder complexity and the latency. Various key performance metrics such as number of slices, maximum usable frequency, dynamic power consumption, energy density, and energy throughput were estimated for different filter orders and address lengths. Analyses of the results obtained indicate that performance metrics of the suggested implementation was broadly in line with theoretical expectations.

A new approach was suggested by Pramod Kumar Meher (2008), for the computation of block pseudocyclic convolution using a block cyclic convolution of equal length along with some correction terms. Low-complexity algorithms were derived for efficient computation of those error terms, and the overall complexities of the proposed technique were
estimated. The proposed algorithms were used further to design high-throughput and reduced-hardware structures for cyclic convolution where the cofactors were not relatively prime.

The suggested structures for high-throughput implementation were found to offer a reduction of nearly 50%–75% of area-delay product over the existing structures for several convolution-lengths. Low-complexity structures for input/output addition units of short length convolutions were derived and used along with high-throughput modules for hardware-efficient realization of multifactor convolution, which offers nearly 25%–75% reduction of area-delay complexity over the existing structures for various non-prime-factor length convolutions.

2.5 RECONFIGURABLE MULTIPLIER ON FIR FILTER

Xinyu Xu et al (2006), suggested SDR receiver platform based on a new substrate integrated waveguide six-port structure. This SDR receiver platform operates from 22 to 26 GHz and it was designed to be robust, low cost, and suitable for different communication schemes. In this study, the receiver was demonstrated to support quadrature phase-shift keying and 16 quadrature amplitude modulation schemes. System-level simulation was made and prototype circuits were fabricated to evaluate the system performance. It was found that the combination of SDR and six-port technology can provide a great flexibility in system configuration, a significant reduction in system development cost, and also a high potential for software reuse. The suggested receiver showed a possible application of universal direct demodulator for future SDR terminals in various wireless communication systems.

Vinod and Lai (2006) presented a method to implement FIR filters for SDR receivers using minimum number of adders. They used an arithmetic scheme, known as Pseudo Floating-Point (PFP) representation to encode the
filter coefficients. By employing a span reduction technique, they showed that the filter coefficients can be coded using considerably fewer bits than conventional 24-bit and 16-bit fixed-point filters. Simulation results showed that the magnitude responses of the filters coded in PFP meet the attenuation requirements of wireless communication standard specifications. The suggested method offered average reductions of 40% in the number of adders and 80% in the number of full adders needed for the coefficient multipliers over conventional FIR filter implementation methods.

Rahim Bagheri (2006), presented an article which described a fully integrated 90 nm CMOS software-defined radio receiver operating in the 800 MHz to 5 GHz band. Unlike the classical SDR paradigm, which digitizes the whole spectrum uniformly, this receiver acts as a signal conditioner for the analog-to-digital converters, emphasizing only the wanted channel. Thus, the ADCs operate with modest resolution and sample rate, consuming low power. This approach was an attempt to have portable SDR a reality.

Abidi (2007) reported that in mobile handsets, it is enough to receive one channel with any bandwidth, situated in any band. Thus, the front-end can be tuned electronically. Taking a cue from a digital front-end, the receiver’s flexible analog baseband samples the channel of interest at zero IF, and is followed by a clock-programmable down-sampling with embedded filtering. This gave a tunable selectivity that exceeds that of RF pre-filter, and a conversion rate that was low enough for A/D conversion at only milli-watts. The front-end consists of a wideband low noise amplifier and a mixer tunable by a wideband LO. A 90-nm CMOS prototype tunes 200 kHz to 20MHz wide channels located anywhere from 800 MHz to 6 GHz.

In Rauwerda et al (2008), it was reported that mobile wireless terminals tend to become multimode wireless communication devices. Furthermore, these devices become adaptive. The heterogeneous reconfigurable
hardware provides the flexibility, performance, and efficiency to enable the implementation of these devices. The implementation of a wideband code division multiple access and an orthogonal frequency division multiplexing receiver using the same coarse-grained reconfigurable MONTIUM tile processor was discussed. Besides the baseband processing part of the receiver, the same reconfigurable processor had also been used to implement Viterbi and Turbo channel decoders.

Zhiyu Ru et al (2009), presented a SDR receiver with improved robustness to Out-of-Band Interference (OBI). Two main challenges were identified for an OBI-robust SDR receiver: out-of-band nonlinearity and harmonic mixing. Voltage gain at RF is avoided, and instead realized at baseband in combination with low-pass filtering to mitigate blockers and improve out-of-band IIP3. They reported two alternative “iterative” Harmonic-Rejection (HR) techniques to achieve high HR robust to mismatch: a) an analog two-stage polyphase HR concept, which enhances the HR to more than 60 dB; b) a digital Adaptive Interference Cancelling (AIC) technique, which can suppress one dominating harmonic by at least 80 dB. An accurate multiphase clock generator is presented for a mismatch-robust HR. A proof-of-concept receiver was implemented in 65 nm CMOS.

The article presented by Pedro Cruz et al (2010), reviews the main parts of an SDR to emphasize several possible implementations of both receivers and transmitters. They reported that many of these architectures are actually fairly old techniques that have been recently made practical due to the enormous increase in the capabilities of digital signal processors. They described solutions for testing and characterizing these types of devices as well. The SDRs typically operate in both the analog and the digital domains, thus a mixed-domain instrumentation was necessary to carry out testing.
2.6 FIR FOR DSP APPLICATIONS

Dengpan Mou et al (2003) reported that the sync processing will continue to be a mandatory block for future fully digital multimedia terminals, to offer a compatible analog video input. They concentrated on the prototypical implementation on a FPGA board and a synthesized design on a 0.35 μm CMOS technology. Compared with state of the art PLL technology, the FPGA prototype demonstrates impressively the improved picture stability with all sources, especially with noisy and unstable analog signals.

Yeung and Chan (2004) studied the design and multiplier-less realization of a new Software Radio Receiver (SRR) with reduced system delay. It employs low-delay FIR and digital all pass filters to effectively reduce the system delay of the multistage decimators in SRRs. Design results show that the system delay and implementation complexities (especially in terms of high-speed variable multipliers) of the reported architecture are considerably reduced as compared to conventional approaches.

Daylight et al (2004) indicated that the embedded systems are evolving from traditional, stand-alone devices to devices that participate in Internet activity. The days of simple, manifest embedded software [e.g. a simple FIR algorithm on a DSP] are over. The complex, non-manifest code, executed on a variety of embedded platforms in a distributed manner, characterizes the next generation embedded software. One dominant niche, which they concentrate on, was embedded, multimedia software. The need was present to map large scale, dynamic, multimedia software onto an embedded system in a systematic and highly optimized manner.

The objective of their work was to introduce high-level, systematically applicable, data structure transformations and to show in detail the practical feasibility of their optimizations on three real-life multimedia
case studies. They derived Pareto tradeoff points in terms of accesses versus memory footprint and obtain significant gains in execution time and power consumption with respect to the initial implementation choices. Their approach was a first step to systematically applying high-level data structure transformations in the context of memory-efficient and low-power multimedia systems.

A charge-domain sampling technique for realization of mixed-mode FIR filters was presented by Sami Karvonen et al (2006). The method was based on weighting signal current samples integrated into a sampling capacitor with a set of parallel digitally controlled current-mode switches, each carrying a unit current element. The fine achievable resolution and digital controllability of the filter tap coefficients allows realization of advanced programmable FIR filtering functions embedded into high-frequency signal sampling. The circuit-level simulation results of an example 50-MHz IF-sampler with a built-in 22-tap complex band-pass since FIR function in 0.35 \( \mu \)m CMOS demonstrated the feasibility of the presented method.

Pramod Kumar Meher (2010) presented that the DA-based computation was popular for its potential for efficient memory-based implementation of FIR filter where the filter outputs are computed as inner-product of input-sample vectors and filter-coefficient vector. In this work, however, they show that the LUT-multiplier-based approach, where the memory elements store all the possible values of products of the filter coefficients could be an area-efficient alternative to DA-based design of FIR filter with the same throughput of implementation. By operand and inner-product decompositions, respectively, they have designed the conventional LUT-multiplier-based and DA-based structures for FIR filter of equivalent throughput, where the LUT-multiplier-based design involves
nearly the same memory and the same number of adders, and less number of input register at the cost of slightly higher adder-widths than the other.

Moreover, they described two new approaches to LUT-based multiplication, which could be used to reduce the memory size to half of the conventional LUT-based multiplication. Further more, they presented a modified transposed form FIR filter, where a single segmented memory-core with only one pair of decoders were used to minimize the combinational area. The reported LUT-based FIR filter was found to involve nearly half the memory-space and the complexity of decoders and input-registers, at the cost of marginal increase in the width of the adders, and additional AND-OR-INVERT gates and NOR gates. They have synthesized the DA-based design and LUT-multiplier based design of 16-tap FIR filters by Synopsys Design Compiler using TSMC 90 nm library, and they have found that the reported LUT-multiplier-based design involves nearly 15% less area than the DA-based design for the same throughput and lower latency of implementation.

Seok-Jae Lee et al (2011) presented an architectural approach to the design of low power reconfigurable FIR filter. The approach was well suited when the filter order was fixed and not changed for particular applications, and efficient trade-off between power savings and filter performance can be made using the reported architecture. Generally, FIR filter has large amplitude variations in input data and coefficients. Considering the amplitude of the filter coefficients and inputs, the reported FIR filter dynamically changes the filter order. Mathematical analysis on power savings and filter performance degradation and its experimental results show that the reported approach achieves significant power savings without seriously compromising the filter performance. The power savings was up to 41.9% with minor performance
degradation and the area overhead of the reported scheme was less than 5.3% compared to the conventional approach.

Shmaliy and Ibarro-Manzano (2011) presented that the Noise Power Gain (NPG) matrix was specialized in state space for transversal FIR estimators intended for filtering, prediction, and smoothing of discrete time-variant state models with states measured. A computationally efficient iterative algorithm for NPG associated with unbiased estimation was provided. Based on a numerical example, they show that the estimates are well bounded with the Error Bound (EB) specified in the three-sigma sense by the main components of the NPG matrix and measurement noise variance. In turn, the cross-components in the NPG matrix represent interactions in the estimator channels. It was concluded that EB can serve as an efficient measure of errors in optimal and suboptimal FIR and Kalman structures. The development of multiple communication standards and services has created the need for a flexible and efficient computational platform for baseband signal processing.

In Lu et al (2011), using a set of heterogeneous Reconfigurable Execution Units (RCEUS) and a homogeneous control mechanism, the reported reconfigurable architecture achieves a large computational capability while still providing a high degree of flexibility. Software tools and a library of commonly used algorithms are also reported in this work to provide a convenient framework for hardware generation and algorithm mapping. In this way, the architecture can be specified in a high-level language and it also provides increased hardware resource usage. Finally, they evaluate the system’s performance on representative algorithms, specifically a 32-tap FIR filter and a 256-point FFT, and compare them with commercial DSP chips as well as with other reconfigurable and multi-core architectures.
Thus, the survey indicates that the conventional problems do exist in the FIR filter and modifications are required to be made to minimize the area reduction and power consumption. Issues pertaining to the FIR filter design and the attempt made towards theoretical study on architectural design of FIR filter are the key factors to pave way for the concentration of a strong modification in the conventional FIR filter design. This survey also encourages attempting the conventional problem persistent in the implementation of such filters. Further, the survey clearly indicates the feasibility of implementing the concept in FPGA environment.