

LIST OF PUBLICATIONS

1. **Hemalatha, A.** and Shanmugam, A. “Reconfigurable Multiplier on FIR Filter for SDR Receiver”, International Journal of Engineering Research and Industrial Applications, Pune, India, Vol. 4, No. 4, pp. 227-236, 2011.
2. **Hemalatha, A.** and Shanmugam, A. “Computer Aided Design for Low Power FIR Processor on System-on-chip Platform Architecture for High Performance DSP Applications”, International Journal of Computer Science and Network Security, Korea, Vol. 11, No. 7, pp. 38-42, 2011.
3. **Hemalatha, A.** and Shanmugam, A. “A Novel Shift and Add Alogorithm for Low Power and Area Efficient FIR Filter”, European Journal of Scientific Research, London, Vol. 49, No. 4, pp. 634-641, 2011.
4. **Hemalatha, A.** and Shanmugam, A. “Performance of Enhanced Transaction Level Model for Reliability Analysis of Multi-cores SoCs”, International Journal of Systemics, Cybernetics and Informatics, Hyderabad, India, JAN10-07, pp. 44-48, 2010.
5. **Hemalatha, A.** and Shanmugam, A. “Low Power System-on-chip Platform Architecture for High Performance DSP Applications”, Proceedings of the National Conference on Frontier Research Areas in Communication, Computer & Control Engineering at Kings College of Engineering, Thanjavur, India, p. 14, 2008.
6. **Hemalatha, A.** and Shanmugam, A. “A Flexible Low Power High Performance DSP IP Core for Programmable System-on-chip”, Proceedings of the National Conference on Emerging trends in Communucation at Dhanalakshmi Srinivasan Engineering College, Perambalur, India, 2008.

7. **Hemalatha, A.** and Shanmugam, A. “Improved Dynamic Power Management schemes and Reliability Modeling in Multi-core SoCs”, Proceedings of the International Conference on Advanced Communication & Informatics at Thanthai Periyar Govt. Institute of Technology, Vellore, India, pp. 89-95, 2009.
8. **Hemalatha, A.** and Shanmugam, A. “Performance Evaluation of Optimized Source Routing for Mesh Topology Type NoC Architecture”, Proceedings of the National Conference on Signal Processing, Communication and VLSI at Anna University, Coimbatore, India, 2010.